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SiGe HBT Technology

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1.1 Introduction

Advances in silicon–germanium (SiGe) heterojunction bipolar transistor (HBT) technologies resulted in an impressive increase in high-frequency performance during the last decade extending the addressed application frequencies into the mm- and sub-mm-wave bands. Today, SiGe HBTs are widely used for applications like automotive radar, high-speed wireless and optical data links, and high-precision analog circuits. BiCMOS technologies which comprise high-speed SiGe HBTs in a radio-frequency (RF) CMOS technology environment combine the excellent RF performance of SiGe HBTs with the high level of integration and the high computing power of Si CMOS. These technologies became a key enabler for demanding mm-wave systems which integrate radio front-end circuits together with digital control circuits and signal processing on a single chip. Previous development has demonstrated that SiGe HBTs continue to offer significantly higher cutoff frequencies, higher output power, and superior analog characteristics compared to CMOS transistors of the same lithography node. Thus, the integration of SiGe HBTs in a CMOS platform represents a very attractive option to boost the RF performance of a given technology node.

The state of the art of SiGe HBT technology before the start of the DOTSEVEN project in October 2012 was reviewed in [Che11]. Developments performed within the predecessor project DOTFIVE resulted in the first demonstration of SiGe HBTs with maximum oscillation frequencies, f_{MAX} , of 500 GHz together with transit frequencies, f_{T} , of 300 GHz and minimum ring oscillator gate delays of 2.0 ps [Hei10]. This was the starting point of the DOTSEVEN project addressing the challenging target for SiGe HBTs with peak f_{MAX} values of 700 GHz and minimum gate delays of

1.4 ps. Figure 1.1 summarizes published peak f_T and f_{MAX} values of selected high-speed SiGe HBT processes from the last decade. BiCMOS technologies with peak f_{MAX} values between 300 GHz and 400 GHz and peak f_T values of 230–320 GHz are in production or pre-production at several companies now. Recent research results have demonstrated that this performance can be increased much further. The values obtained within the DOTSEVEN project are indicated as red diamonds in Figure 1.1. In 2015, two separate investigations demonstrated new record values for f_{MAX} [Boe15] and f_T [Kor15]. Further technology optimization finally enabled the demonstration of the DOTSEVEN goal including the simultaneous realization of peak f_T and f_{MAX} values of 505 GHz and 720 GHz, respectively [Hei16].

The remainder of this chapter is organized as follows. Major performance factors of SiGe HBTs are reviewed in the section “HBT Performance Factors.” Fundamental dependencies of typical high-frequency figures of merit (FoMs) on device parameters are discussed here. The section “HBT Device and Process Architectures Explored in the DOTSEVEN Project” addresses device architectures for high-performance SiGe HBTs and process integration aspects. Favored process options for HBTs with selective epitaxial growth (SEG) and with non-selective epitaxial growth (NSEG) of the SiGe base layer are analyzed in detail. The focus is on the work performed in the DOTSEVEN project concerning the development of the high-performance SiGe BiCMOS technology platform B11HFC at Infineon (see the section “DPSA-SEG Device Architecture”), the investigation of an advanced HBT

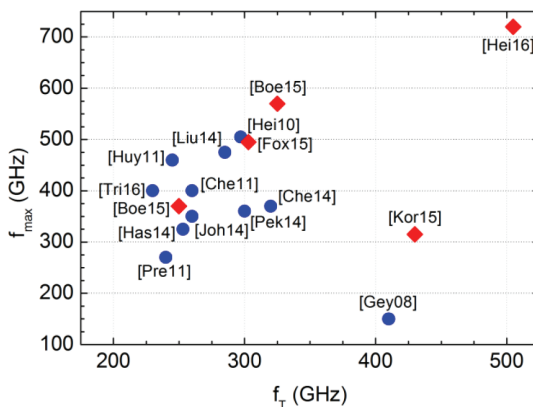


Figure 1.1 Peak f_T and f_{MAX} values of high-speed SiGe HBT technologies. Red diamonds indicate results of the DOTSEVEN project.

process with SEG of the base and epitaxial base link (EBL) regions (see the section “Approaches to Overcome Limitations of the DPSA-SEG Architecture”), and the optimization of a process with NSEG of the base (see the section “Non-selective Epitaxial Growth of the Base”), which was finally utilized by IHP to reach the DOTSEVEN goal. The section “Optimization of the Vertical Doping Profile” addresses the optimization of the vertical doping profile for f_T improvement. The final technology optimization for minimum device parasitics and balanced f_T and f_{MAX} improvement is discussed in the section “Optimization towards 700 GHz f_{MAX} .”

1.2 HBT Performance Factors

Typical FoMs characterizing a process technology in terms of high-frequency performance are the transit frequency f_T and the maximum oscillation frequency f_{MAX} . The transit frequency f_T is defined as the frequency for which the small-signal current gain $|h_{21}|$ falls to unity, i.e.,

$$|h_{21}(f)|_{f=f_T} = 1. \quad (1.1)$$

The frequency f_{MAX} is defined as the maximum frequency for which the transistor can amplify power. In this context, Mason’s unilateral power gain U is widely used, and f_{MAX} is defined by:

$$U(f)|_{f=f_{MAX}} = 1. \quad (1.2)$$

While the frequency f_{MAX} represents a speed metric for circuits such as amplifiers and oscillators, f_T gives a measure of the speed of switching circuits such as dividers. Ring-oscillator gate delays are relevant FoMs for digital high-speed circuits. Here, we use the current mode logic (CML) ring-oscillator gate delay time τ_{CML} . In addition, the base–collector breakdown voltage BV_{CEs} and the open-base emitter–collector breakdown voltage BV_{CEo} are important since they determine the maximum output power that can be provided by a transistor. Further characteristics of relevance for evaluating potential applications include the minimum noise figure, the linearity, and the gain of a transistor.

In the following, we are going to discuss the impact of different device regions and their electronic properties on RF performance. Basic device regions are indicated in the generic cross section of a high-performance SiGe HBT shown in Figure 1.2. For the analysis of the contribution of the individual device region to the delay time of the transistors

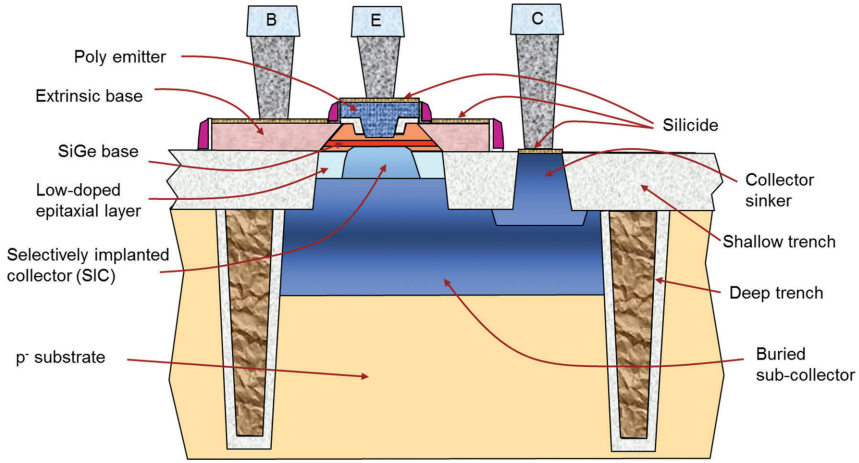


Figure 1.2 Schematic cross section of a high speed SiGe HBT.

response to an RF signal, it is helpful to relate the resistances and capacitances of the device regions to a simplified small-signal compact model.

Figure 1.3 indicates the resistances and capacitances of the individual device regions and relates them to a small signal equivalent circuit for the transistor operation in forward active mode. The model includes the resistances R_E , R_B , and R_C , of the emitter, base, and collector, respectively. The base resistance is divided into an intrinsic contribution R_{Bi} and extrinsic

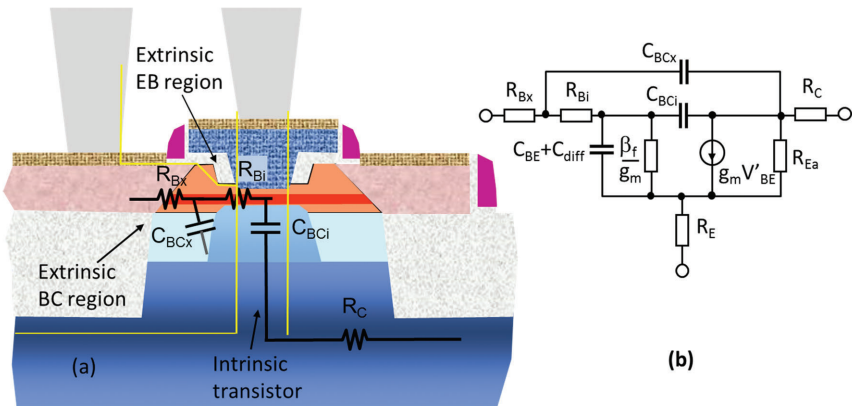


Figure 1.3 Device cross section with parasitic resistances and capacitances associated with different device regions (a) and a corresponding small signal equivalent circuit (b).

contribution R_{Bx} originating from the link region which contacts the intrinsic base. The base–collector capacitance (C_{BC}) is divided into an intrinsic part C_{BCi} and an extrinsic part C_{BCx} related to the base link region. C_{BE} includes the depletion capacitance as well as the oxide capacitance of the base–emitter junction, C_{diff} is the diffusion capacitance related to the storage of minority charges in the forward operation mode, β_f is the forward DC current gain, g_m is the transconductance, R_{Ea} is the output resistance related to the Early effect, and V'_{BE} is the intrinsic base–emitter voltage.

The frequency-dependent small signal current gain $h_{21}(f)$ of the model depicted in Figure 1.3 is approximately given by:

$$\frac{1}{h_{21}(f)} = \frac{1}{\beta_f} + j2\pi f \left(\frac{C_{diff} + C_{BE} + C_{BC}}{g_m} + (R_E + R_C) C_{BC} \right). \quad (1.3)$$

In the limit of large frequencies, h_{21} is inversely proportional to the frequency f . The corresponding unit gain transit frequency f_T is given as:

$$\frac{1}{2\pi f_T} = \frac{C_{diff} + C_{BE} + C_{BC}}{g_m} + (R_E + R_C) C_{BC}. \quad (1.4)$$

The transconductance g_m is proportional to the collector current I_C in the bias region of ideal exponential slope according to $g_m = qI_C/k_B T$, where q is the elementary charge, k_B is Boltzmann's constant, and T is the junction temperature. The diffusion capacitance C_{diff} accounts for the storage of locally compensated minority carriers during forward transistor operation. The contribution to C_{diff} can be analyzed in a charge-control model [Tau98]. This analysis relies on the fact that any variation of the bias point of the device is related to changes of the carrier densities within the device which are fed by currents into the device contacts. The corresponding forward transit time

$$\tau_F = \frac{C_{diff}}{g_m} = \tau_E + \tau_{EB} + \tau_B + \tau_{BC} \quad (1.5)$$

can be divided into contributions accounting for charge storage in the emitter, base–emitter junction, base, and base–collector junction regions, respectively. According to the charge-control model, these contributions are approximately given by:

$$\tau_E = \frac{C_E}{g_m}, \quad (1.6)$$

$$\tau_{EB} = \frac{C_N}{g_m}, \quad (1.7)$$

$$\tau_B = \frac{w_B^2}{2D_{nB}} + \frac{w_B}{v_{\text{sat}}}, \quad (1.8)$$

$$\tau_{BC} = \frac{w_{BC}}{2v_{\text{sat}}}. \quad (1.9)$$

Here, w_B is the width of the neutral base region, w_{BC} is the depletion width of the base–collector junction, D_{nB} is the electron diffusion coefficient in the base, and v_{sat} is the saturation velocity of electrons. C_E and C_N denote the parts of the diffusion capacitance related to neutral charge storage in the emitter and base–emitter junction regions, respectively. The compensated charge C_N stored in the base–emitter junction can account for a significant contribution to τ_F in particular at high current densities [Hue96]. The emitter delay time τ_E is of minor importance for typical SiGe HBTs since the amount of holes stored in the emitter is inversely proportional to the current gain. The magnitude of C_E is determined by the emitter properties. The maximum oscillation frequency of the equivalent circuit of Figure 1.3 is approximately given by:

$$f_{\text{MAX}} \cong \sqrt{\frac{f_T}{8\pi((R_{Bx} + R_{Bi})C_{Bi} + R_{Bx}C_{Bx})}}. \quad (1.10)$$

This relation is reduced to:

$$f_{\text{MAX}} \cong \sqrt{\frac{f_T}{8\pi R_B C_{BC}}}, \quad (1.11)$$

if R_B and C_{BC} are not separated into extrinsic and intrinsic contributions.

Based on the Equations (1.4) to (1.10), the following scenario can be envisioned for the enhancement of the cutoff frequencies f_T and f_{MAX} by scaling vertical and lateral device dimensions. The transit frequency f_T is predominantly determined by the vertical doping profile. Figure 1.4 illustrates qualitatively the directions of profile optimization for f_T enhancement.

Reduction of the width w_B of the boron-doped base reduces the base transit time τ_B according to Equation (1.7). A minimum width of the boron-doped region has to be ensured together with a low base sheet resistance. Today, base layers with typical sheet resistances of about 2 k Ω /sq can be grown epitaxially with widths of less than 5 nm. In addition to the deposition of a thin base, its diffusion during subsequent processes has to be kept as small as possible. A widely applied approach to minimize B diffusion is the additional doping of the SiGe layer with carbon [Lan96, Ost97, Rue99]. Moreover, the thermal budget of post-epi processing has to be kept low.

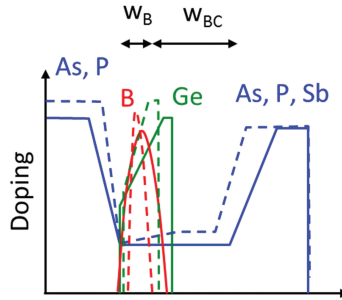


Figure 1.4 Schematic vertical doping profile of a SiGe HBT. The dashed lines indicate a scaled profile for enhanced f_T .

The challenge here is to realize simultaneously high dopant activation in heavily doped device regions and minimum diffusion broadening of the base.

Together with the base width, the width of the Ge profile is also shrunk. This allows one to increase the peak Ge concentration without exceeding the critical thickness of the SiGe layer above which the SiGe layer becomes thermodynamically unstable against the formation of dislocations. For low base transit time τ_B , it is beneficial to realize a steep gradient of the Ge concentration across the non-depleted base width w_B . The grading of the Ge profile as indicated in Figure 1.4 causes a built-in electric field due to the decrease of the band gap with increasing Ge content. This field accelerates minority electrons in the base and reduces τ_B .

Reduction of depletion width w_{BC} of the base–collector junction is a measure to reduce the base–collector transit time τ_{BC} . This reduction of τ_{BC} has to be traded off against an increased base–collector capacitance C_{BCi} and a reduced base–collector breakdown voltage due to reduced w_{BC} .

The neutral charge storage C_N in the base–emitter region can be reduced by decreasing of the base–emitter depletion width w_{EB} in conjunction with an optimized Ge-profile in the base–emitter junction region. However, reduction of w_{EB} results also in a reduction of the base–emitter breakdown voltage BV_{EB0} and in tunnel currents at low base–emitter voltages. These effects have to be traded off against the reduction of C_N .

The doping profiles of the non-depleted emitter and collector regions are optimized for low resistivity due to high concentrations of electrically active dopants. The lowest emitter resistances are typically achieved with mono-crystalline emitters. In addition to the above mentioned measures for f_T enhancement by vertical profile engineering, one also has to minimize

contributions to the base–emitter and base–collector capacitances originating from the edges of the device for realizing higher f_T values according to Equation (1.4).

For realizing high f_{MAX} values, it is crucial to minimize the base resistance and the base–collector capacitance together with high f_T values as indicated by Equation (1.9). The required reduction of these device parasitics is typically addressed by scaling lateral device dimensions and by optimizing the base-link regions. Figure 1.5 illustrates relevant lateral device dimensions and major contributions of the base-link region to R_B and C_{BC} .

Contributions to the extrinsic base resistance originate from the extension of the base layer below the base–emitter spacer, from the adjacent mono-crystalline or poly-crystalline p-doped region, the contact resistance between silicide and base poly-Si, the silicide resistance, the contact resistance between silicide and metal contact plug, as well as from the resistance of subsequent metal regions. The extrinsic base–collector capacitance includes capacitances of the mono- and poly-crystalline extrinsic base regions to the selectively implanted collector (SIC), the buried collector layer in the active region, and the buried collector below the base–collector isolation layer. Reduction of these parasitic resistances and capacitances is addressed by reducing the corresponding lateral device dimensions such as the width of the base–emitter spacer d_{SP} , the width of the emitter poly-Si w_{EP} , and the width of the active collector region w_{Col} . However, depending on the details of the device architecture, there are several tradeoffs between the different parameters. For example, the reduction of w_{Col} can lead not only to a reduction of C_{BCx} but also to an increase of R_{Bx} .

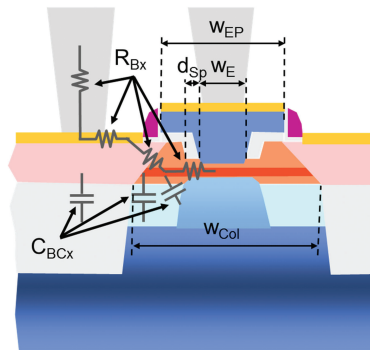


Figure 1.5 Device cross section with lateral device dimensions and major contributions of the base-link region to R_B and C_{BC} .

The intrinsic contribution to the base resistance R_{Bi} can be reduced for a given base sheet resistance R_{sbi} by narrowing the emitter window width w_E . In a typical scaling scenario, lateral scaling of w_E is accompanied by vertical scaling of the doping profile and increased current densities at peak f_T . Under these conditions, it is a major challenge to maintain low emitter and collector resistances as well as thermal resistances when the emitter width is scaled down.

Scaling of the HBT device dimensions under the boundary conditions of minimum base, emitter, and collector resistances imposes complex requirements on device architecture and fabrication process. These challenges have stimulated various innovations of the HBT fabrication process which addressed the reduction of the individual device parasitics by structural improvements as well as by improved material properties such as reduced specific and contact resistances. Approaches explored in the DOTSEVEN project will be reviewed in the following sections.

1.3 HBT Device and Process Architectures Explored in the DOTSEVEN Project

Innovations of the device architecture and of the fabrication processes have been major factors for the improvement of the RF performance of SiGe HBTs during the last decades. Fundamental requirements on the device architecture for high-speed HBTs are minimum access resistances to the intrinsic emitter, base, and collector regions together with low contributions of the extrinsic device regions to the base–collector and base–emitter capacitances. The development of device and process architectures which facilitate the simultaneous realization of low R_B and low C_{BC} has been a major challenge in this context. The realization of devices with low thermal resistances is a further requirement in order to limit self-heating.

The above-mentioned device targets have to be realized in fabrication processes which are manufacturable in high volumes with high yield. A further fundamental requirement on the HBT fabrication process is the compatibility with the addressed CMOS technology platform. The integration of SiGe HBTs and other RF-enabling passive or active devices into a BiCMOS technology platform has to be realized without degrading HBT or CMOS device characteristics or yield. The large potential of advanced CMOS processes for geometry scaling opens new options also for the HBT fabrication. However, new challenges arise for the integration of SiGe HBTs

in continuously shrinking CMOS nodes from tight constraints on the thermal budget and on device topology.

As regards the SiGe HBT device concepts, all current production-related high-speed transistors take advantage of the so-called double-poly-Si (DP) architecture. This configuration provides access from the contact region to the intrinsic base and emitter region by poly-Si layers which are dielectrically isolated against the surrounding transistor regions. It is a powerful means to keep extrinsic parasitics, such as R_{Bx} , C_{BCx} , R_E , and C_{BE} , small. It is therefore evident that the basic structure of modern SiGe HBTs is becoming more similar. Nevertheless, we are faced with quite different approaches for device manufacturing resulting in different consequences of their potential electrical performance.

A key differentiator for SiGe HBT fabrication is the way in which the SiGe base is formed. Existing SiGe HBT technologies use either selective or non-selective epitaxial growth of the base. Both approaches have been used for the development of high-performance SiGe HBT processes and found their way into industrial mass production. In the DOTFIVE project, technological solutions were developed promising further speed enhancements for HBT concepts with selective as well as with non-selective base epitaxy. Due to their specific implications on the process complexity and the self-alignment of the transistor regions, various technologies were investigated also in the DOTSEVEN project using the different base-epitaxy methods. Opportunities and challenges of the two approaches will be discussed in detail in the following subsections. This applies also to process options regarding the lateral collector isolation by deep trenches or by the standard shallow trenches of the CMOS process, the formation of the highly conductive sub-collector, and the formation of the base-emitter structure. The choice of the substrate, i.e., bulk or silicon-on-insulator (SOI), is another criterion to differentiate SiGe HBT technologies. Driven by the continuous development of SOI-based CMOS technologies several publications have been devoted to the issue of a suitable technology and device concept for high-speed SiGe HBTs on SOI wafers [Was00, Rue04, Ave05, Thi13]. Here, we will not address this architectural aspect because it was outside the focus of the DOTSEVEN project.

1.3.1 Selective Epitaxial Growth of the Base

The classical DP-self-aligned (SA) SiGe HBT technology with SEG of the base represents the most attractive process architecture from the point of view of manufacturing and degree of self-alignment. As described in the next

section, the DOTFIVE project partners Infineon and STMicroelectronics as well as FreeScale (now NXP) worked intensively on this concept in the last decade to push its performance. However, substantial improvements beyond the current level will hardly be feasible with this approach as discussed in the section “Approaches to Overcome Limitations of the DPSA-SEG Architecture.” In the DOTFIVE project, alternative SEG process flows were developed to overcome limitations of the conventional DPSA-SEG technology. It will be reported below in detail on joint activities of Infineon and IHP in the DOTSEVEN project to test one of these approaches within Infineon’s 130 nm BiCMOS platform.

1.3.1.1 DPSA-SEG device architecture

The conventional double-poly-Si self-aligned SiGe HBT technology with SEG enjoys large popularity and has been applied in production for long time by several companies [Boe04, Ave09, Joh07]. This process takes advantage from the fact that only one lithographic step is needed to completely construct the internal transistor. In principle, no further mask step is necessary to form the SIC region or the isolation between emitter and base. Usually, this process starts with the deposition of a layer stack comprising a bottom oxide, a p^+ poly-Si layer, an upper oxide, and a capping nitride. The emitter window is opened by dry etching which stops at the bottom oxide (Figure 1.6(a)). Nitride spacer formation will prevent from pulling back the upper oxide during the subsequent oxide wet etching. By this step, the intrinsic collector region is exposed and an overhang of the p^+ poly-Si is created (Figure 1.6(b)). At this point the SIC can be formed which provides a low-ohmic connection to the highly doped sub-collector. In addition, the nitride inside spacers protect against Si seeding of the p^+ poly-Si during the following base epitaxy. With this step, the link between the intrinsic base and the extrinsic part (p^+ poly-Si = base poly) is formed (Figure 1.6(c)). Whether the nitride layers are removed at a later stage or not is handled differently [Che11].

The remaining steps are very common also for other HBT processes such as technologies with non-selective base epi. Inside base–emitter spacers are formed and the in situ doped emitter layer is grown with a non-selective epitaxial step. Therefore, at least partly, a mono-crystalline emitter region can be found adjacent to the substrate surface already after deposition. The HBT flow is continued by patterning the emitter and base poly-Si layers. Finally, a short-term high-temperature treatment is needed in order to out-diffuse dopants from the highly doped emitter layer into the base cap layer before the process flow is completed by salicidation and backend fabrication (Figure 1.6(d)). The final annealing step contributes not only to improved

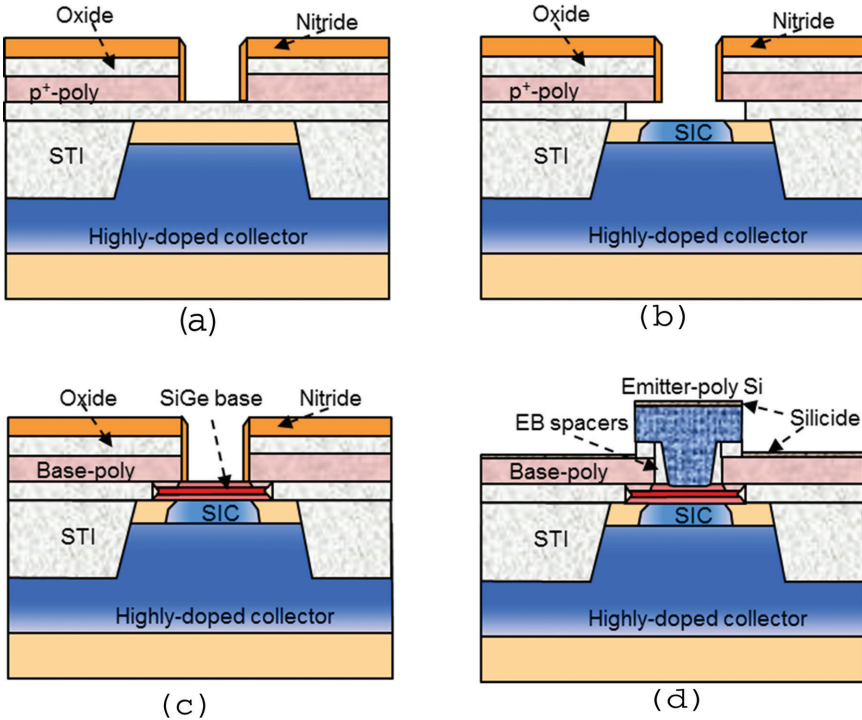


Figure 1.6 Schematic cross sections of conventional DPSA-SEG process flow.

base-current idealities but it also determines the emitter resistance. In the case of a bipolar-only technology, e.g., Infineon's B7HF200 [Boe04], the thermal budget is largely governed by the needs of the HBT. In BiCMOS processes, as a rule, the minimum requirements of the source–drain anneal determine the crucial thermal budget of the HBT assuming that a ‘source/drain-after-HBT’ integration scheme is realized.

The basic structure of the aforementioned DPSA-SEG process flow was already employed for the first demonstrations [Sat92, Mei95, Pru95]. Essentially, it has been maintained to date. In Figure 1.7, a TEM cross section of Infineon's latest SiGe HBT transistor generation is shown.

In [Che11], certain differences between the developments of different companies are pointed out. For example, Infineon utilized temporary auxiliary spacers to adjust the area of the SiC whereas the SiC was performed right after the emitter window opening at STMicroelectronics. There are also deviations in the annealing regime of the base poly. In the Infineon

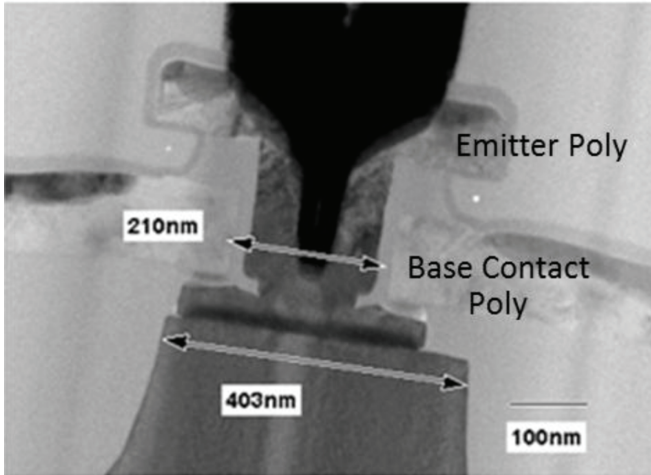


Figure 1.7 TEM cross section of a DPSA-SEG HBT of Infineon's B11HFC technology [Boe15].

flow, an extra thermal treatment after base epitaxy is introduced for out-diffusing B from the base poly toward the intrinsic base layer. Consequently, the base resistance can be reduced but the base tends to broaden causing lower f_T values. Nevertheless, variations of this annealing showed room for optimizations to increase f_{MAX} with tolerable constrains for f_T [Can12].

The collector construction used by Hitachi [Has14], Infineon [Boe15], and STMicroelectronics [Che14] includes all elements which are typical for a high-speed Si bipolar transistor: an epitaxially buried, highly doped sub-collector isolated laterally by deep trenches and a low-ohmic connection to the collector contact realized by a so-called collector sinker. In order to save fabrication efforts and to reduce complexity of the BiCMOS process, NXP (former FreeScale) developed a Sub-Isolation Buried Layer (SIBL) collector structure using only shallow trench isolation (STI) [Joh07]. A common feature of all these technologies is the shallow-trench isolation (STI) between the internal transistor region and the collector contact which enables simultaneously a low capacitive base link.

In the DOTFIVE project comprehensive efforts were made by Infineon and STMicroelectronics to improve the high-frequency behavior of the conventional DPSA-SEG technology as reported in [Che11]. Clear progress was achieved by changing the vertical profile, thermal treatments, as well as the lateral transistor dimensions. At that time, Infineon was able to increase its

initial f_T/f_{MAX} values of 190 GHz/250 GHz (B7HF200, [Boe04]) finally to 230 GHz/350 GHz while STMicroelectronics increased these FoMs from 230 GHz/280 GHz (BiMOS9MW, [Ave09]) to 260 GHz/400 GHz. Later, both companies could demonstrate this performance level in a BiCMOS environment too. The f_{MAX} results obtained in the DOTFIVE project and in the recent past for the DPSA-SEG concept [Has14, Che14, Tri16] indicate that it is difficult to reach values beyond 400 GHz. The limited possibilities to decrease R_{Bx} have been proved as the key bottleneck for advancements of the overall RF performance. Alternative concepts which were conceived to overcome this issue will be presented in the next subsection.

1.3.1.2 Approaches to overcome limitations of the DPSA-SEG architecture

If the geometry of a conventional DPSA-SEG SiGe HBT (see Figure 1.6(d)) is shrunk according to scaling scenarios for next technology nodes, as it was carried out in TCAD studies [Sch11b, Sch17], there is no serious indication for an imminent end of performance progress compared to other technology approaches. In practice, however, we are confronted with the fact that the attempts to increase f_{MAX} did not go beyond values of 400 GHz while alternative concepts indeed surpassed this level. Unfortunately, the main reason for this deficiency is closely connected with the key advantage of the conventional DPSA-SEG process, namely the straightforward manufacturing of the link between the intrinsic transistor region and the base poly-Si layer.

The vertical gap between the substrate surface and the base poly is bridged during the selective growth of the base layer (Figure 1.8(a)). Obviously, the base layer and the p+ base poly are separated after base epitaxy

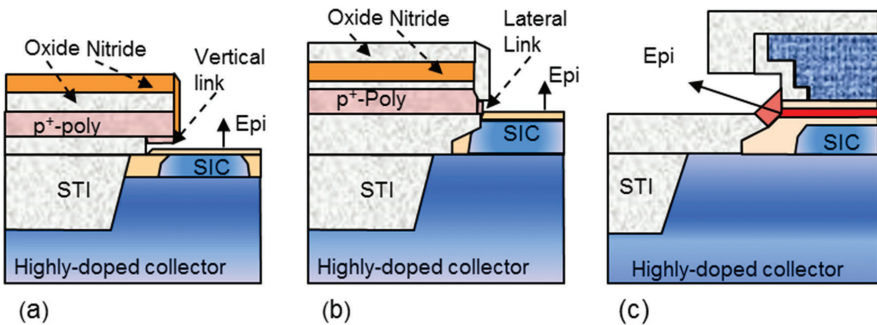


Figure 1.8 Different base link configurations of selective epitaxial growth (SEG) HBTs.

by a higher ohmic region which has to be eliminated by B in-diffusion from the base poly. Additionally, it would be beneficial if dopants could be introduced in the un-doped Si cap layer beneath the emitter–base spacers. Several attempts have been made to solve this problem. For example, borosilicate-glass EB-spacers and a dedicated anneal at 800°C for 10 min were utilized by NEC [Sat92] to overcome this issue for one of the first DPSA-SEG technology developments delivering f_T/f_{MAX} values of about 50 GHz. STMicroelectronics tested soak annealing for a few seconds at 1,010°C to 1,040°C between base and emitter deposition for an advanced DPSA-SEG version [Can12]. An improvement of the $f_T/f_{MAX}/CML$ gate delay values from 300 GHz/370 GHz/2.33 ps to 320 GHz/390 GHz/2.2 ps was shown for a split with additional annealing at 1,010°C in combination with a reduced B dose of the base layer which was applied to compensate for stronger B broadening compared to the reference process.

Other concepts tried to include the region which surrounds the base layer for a lateral connection (Figure 1.8(b)) in addition to the standard configuration with a vertical link to the base poly. Such an approach could mitigate the effect of the decreasing contact area between the intrinsic base layer and the base poly-Si with ongoing lateral scaling. For this purpose, a second poly-Si layer was inserted in the layer stack enclosing the emitter window in [Was03]. An extra selective epi step was implemented in [Fox08] for positioning of the base poly in lateral direction related to the SiGe base. A simple and meanwhile widely used measure to increase the contact area between the base poly and the base layer is, to some extent, the introduction of 45° rotated substrates. In this way, the emitter windows are aligned along the $\langle 100 \rangle$ crystal orientation and the formation of unfavorable facets during epitaxial growth of the base is minimized. However, the progress of above mentioned approaches on RF performance was limited apart from the increased process complexity or the disadvantage of a higher thermal budget. In particular, these attempts did not achieve the progress that might be theoretically possible for highly conductive mono-crystalline base-link region. In this respect, the HBT module with EBL (Figure 1.8(c)) represents an unconventional SEG approach which brought substantial progress for decreasing the specific R_{Bx} contribution without dampening the prospects for high f_T values.

A detailed description of the EBL fabrication process can be found in [Fox11]. The major steps are described below. Figure 1.9(a) shows a cross section after emitter formation. The emitter window was etched in a layer

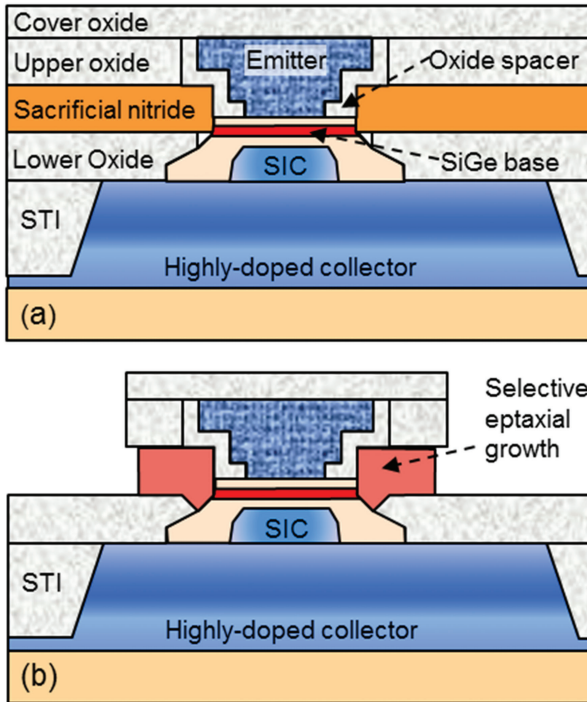


Figure 1.9 Schematic cross sections of the EBL process flow after emitter structuring (a) and after selective growth of the EBL (b).

stack consisting of a lower oxide, a sacrificial nitride, an upper oxide, and a top nitride layer that is already removed at the state of Figure 1.9(a). At this point, there are two specific features which differ from a conventional DPSA-SEG flow. First, a sacrificial nitride layer is deposited instead of the base poly-Si. Second, an overhang of the emitter poly-Si over the emitter window was created in a self-aligned manner by pulling back the upper oxide layer before EB spacer formation. Emitter poly-Si structuring is completed by chemical–mechanical polishing (CMP) similar to [Fox08]. The key idea to form the EBL is illustrated in Figure 1.9(b). After emitter CMP, the devices are covered by an oxide layer, and then the cover oxide and the upper oxide are patterned by a masked dry etching step before the sacrificial nitride is removed by wet etching. The resulting cavities are filled by SEG of B-doped Si as illustrated in Figure 1.9(b) followed by non-selective growth of B-doped Si.

In the first publication on this technology concept [Fox11] $f_T/f_{MAX}/CML$ gate delay values of 300 GHz/480 GHz/1.9 ps were presented. However, a detailed comparison of the EBL HBT performance against standard DPSA-SEG results was not in the focus of this first demonstration. This assessment has been addressed in the DOTSEVEN project. The EBL HBT was compared directly with the conventional DPSA-SEG approach based on identical collector designs, transistor layouts, and measurement conditions. For this purpose, the EBL HBT module was implemented in Infineon's 0.13 μm BiCMOS environment which includes the standard collector concept of an epitaxially buried sub-collector and deep-trench (DT) isolation combined with a mm-wave Cu back-end-of-line (BEOL). In contrast, the original EBL process comprised IHP's DT-free collector approach [Hei02] using STI-isolated, highly doped collector regions as well as an Al-based BEOL.

For this exercise, EBL HBTs and conventional DPSA-SEG HBTs were compared in two ways. First, IHP manufactured its novel device on Infineon wafers in a bipolar-only flow. The joint fabrication started at Infineon by forming the buried sub-collector, the deep trench and STI, and the MOS gates (Table 1.1). Then, the wafer processing was continued at IHP with the EBL module. The CMOS fabrication steps after the HBT module, which could deteriorate the HBT performance, were skipped in these experiments. All process steps for the bipolar devices including the final activation annealing and salicidation were done in these runs at IHP. Compared to [Fox11], the emitter–base spacer process was slightly modified to assist the formation of reduced emitter widths. To eliminate the risk of poly-Si residues, an extra mask was introduced to remove the emitter poly-Si outside of the transistor regions before emitter planarization. Otherwise, we preserved the original EBL flow including the thermal treatment and doping of the SIC, SiGe base, and emitter.

In a second cycle, the full BiCMOS flow was applied. The HBT fabrication was finished at IHP with removing the CMOS protection layer. The further processing corresponded to Infineon's 0.13- μm BiCMOS process including low-doped-drain implantation and annealing, CMOS gate spacer deposition, source/drain implantation and annealing, and salicidation. Table 1.1 shows which process modules were carried out by Infineon and which by IHP for the bipolar-only flow and for the full BiCMOS process, respectively.

Table 1.1 Process modules done by Infineon and IHP for the bipolar-only runs (left) and for the full BiCMOS process (right)

Bipolar-only		BiCMOS	
Infineon	IHP	Infineon	IHP
Buried layer, Epi		Buried layer, Epi	
Isolation		Isolation	
Wells		Wells	
Gate		Gate	
	CMOS protection		CMOS protection
	SiGe HBT		SiGe HBT
		LDD	
		MOS spacers	
		S/D	
	Final anneal	Final anneal	
	Salicide	Salicide	
	IMD	IMD	
Contact		Contact	
BEOL		BEOL	

To assist the BiCMOS integration, several adjustments of the EBL HBT module compared to the bipolar-only runs were made:

- The number of SIC implants for the high-speed HBTs and subsequently the total dose was reduced.
- The base profile thickness was slightly increased to make the profile more robust against the additional thermal budget caused by the CMOS integration.
- The emitter doping was reduced and the Si-cap thickness of the SiGe base deposition was adjusted to compensate for potentially enhanced emitter diffusion due to CMOS integration.
- The effective emitter width was slightly reduced using optimized processes for emitter window lithography and etching to support lateral scaling.
- A new laterally scaled emitter–base spacer process was introduced to reduce the base link resistance.

Figure 1.10 shows the resulting cross sections of the emitter–base complex in the bipolar-only process and the full BiCMOS runs. The effective emitter width amounts to 130 nm for the bipolar-only process and 120 nm in the BiCMOS flow.

In the following, electrical properties of the joint Infineon/IHP HBT fabrications, i.e., bipolar-only and BiCMOS EBL, are evaluated in comparison

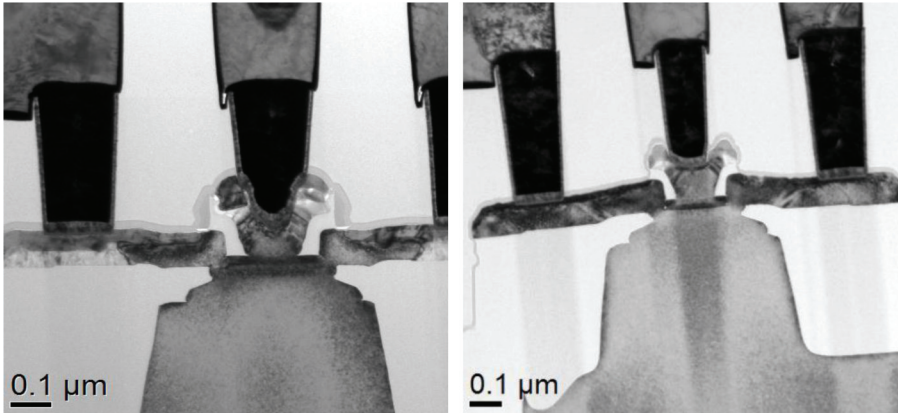


Figure 1.10 TEM cross section of IHP's EBL-HBT module on Infineon's 130 nm platform for the bipolar-only run (left) and full BiCMOS flow (right).

to those of Infineon's DOTFIVE DPSA-SEG results [Che11] and of the IHP reference [Fox11]. Static and dynamic parameters are summarized in Table 1.2.

Concerning the emitter–base (BV_{EB0}) and collector–base (BV_{CB0}) breakdown voltages, it should be noted that the collector–base and base–emitter profiles of the reference EBL HBT [Fox11], and consequently also those of the joint bipolar-only runs, are more aggressively scaled than those of the DPSA reference transistor of Infineon [Che11]. Due to the modifications listed above, the corresponding profiles of the BiCMOS version are relaxed resulting in similar values of BV_{EB0} but also of the current density at peak f_T compared to the Infineon reference.

Now, we turn to the evaluation of the high-frequency behavior. For the determination of f_T and f_{MAX} , OPEN and SHORT de-embedded s -parameters up to 50 GHz were used. f_T and f_{MAX} are extrapolated from the small-signal current gain $|h_{21}|$ and the unilateral gain U , respectively, with -20 dB decay per frequency decade. Regarding the transistor layout, the focus will be on the double-base contact (BEBC) design because it has been proved superior in terms of high-frequency performance. For the Infineon reference transistor only single-base contact (BEC) data are available [Che11]. Therefore, a BEC configuration of the joint bipolar-only preparation was included in Table 1.2 to facilitate the comparison with the conventional DPSA data. IHP's reference device consists of an 8-emitter BEC configuration with comparatively short emitter lengths optimized for the used unconventional collector construction.

Table 1.2 HBT parameters of EBL HBTs fabricated in joint Infineon/IHP flows in comparison to results of EBL [Fox11] and DPSA [Che11] reference flows

Layout	Unit	Measuring Conditions	Infineon/IHP		IHP [Fox11]	Infineon [Che11]
			[Lie16]	[Fox15]		
Technology			BEC	BEC	BEC	BEC
No. transistor			BiCMOS	Bipolar-only		
$w_E \times L_E$	μm^2		3	3	8	3
f_T	GHz	$V_{CB} = 0.5 \text{ V}$, $T = 298 \text{ K}$	0.12×2.69	0.13×2.69	0.155×1.0	0.13×2.70
f_{MAX}	GHz		240	300	305	240
$j_C(\text{peak } f_T)$	$\text{mA}/\mu\text{m}^2$		500	500	465	380
Gate delay	ps	$\Delta V = 200 \text{ mV}$	1.94	1.83	1.86	1.9
Peak β			650	1,000	450	1,300
BV_{CE0}	V	I_B reversal, $V_{BE} = 0.7 \text{ V}$	1.7	1.5	1.75	1.5
BV_{CB0}	V	$j_C = 3 \mu\text{A}/\mu\text{m}^2$	4.9	4.8	4.1	5.5
BV_{EB0}	V	$j_E = 3 \mu\text{A}/\mu\text{m}^2$	2.2	1.5	1.35	2.3
$(R_B + R_E) \times L_E$	$\Omega \times \mu\text{m}$	y_{11} circle fit @ peak f_T	n.a.	46	51	86
$R_C \times L_E$	$\Omega \times \mu\text{m}$	b forced to 1	n.a.	55	40	n.a.
R_{TH}	K/W	[Rus09]	n.a.	2,100	1,500	n.a.
C_{CB}/L_E	fF/ μm	s-parameter	1.38	1.45	1.4	1.3
C_{BE}/L_E	fF/ μm	s-parameter	1.9	2.1	1.9	2.1
C_{CS}/L_E	fF/ μm	Array	n.a.	0.9	0.6	0.9
R_{SBI}	k Ω	Tetrode	2.3	3.0	2.6	2.6

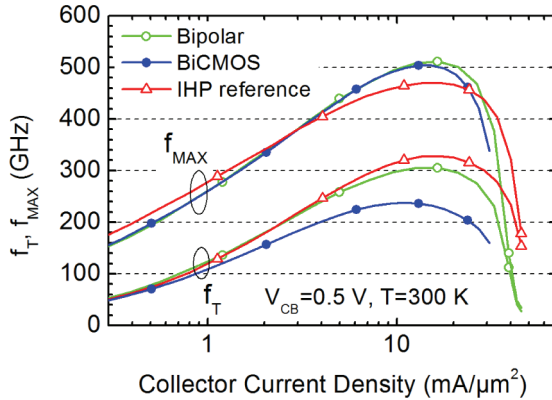


Figure 1.11 Transit frequency f_T and maximum oscillation frequency f_{MAX} vs. the collector current density j_C for Infineon/IHP EBL fabrication in a bipolar-only process and in a BiCMOS run vs. the IHP EBL reference.

Figure 1.11 shows f_T and f_{MAX} as a function of the collector-current density for transistors of the two Infineon/IHP EBL versions and of IHP's reference preparation. Looking at the Infineon/IHP bipolar-only results, the high-frequency parameters (peak f_T/f_{MAX} values of 300 GHz/500 GHz at $V_{CB} = 0.5$ V for the BEBC device, and 305 GHz/465 GHz for the BEC transistor) represent a substantial progress compared to those of the BEC Infineon device (240 GHz/380 GHz) or to results of other DPSA processes [Che14, Tri16]. In general, these figures fit well to the data of IHP's reference transistor, although the BEBC layout shows even a 55 GHz higher peak f_{MAX} whereas peak f_T is 20 GHz lower compared to the IHP reference (Table 1.2). In the case of f_{MAX} , these deviations are explained by the lower C_{CB} of Infineon's collector isolation scheme while in the case of f_T , the lower R_C and R_{TH} of the IHP transistor design have to be considered. Note that the IHP reference was re-measured at Infineon under company typical measuring conditions. The somewhat lower f_{MAX} (445 GHz [Fox15]; 480 GHz [Fox11]) is primarily attributed to the changed extrapolation frequency (20 GHz [Fox15]; 38 GHz [Fox11]).

One important factor for the enhanced RF performance of the HBTs from the joint bipolar-only process vs. that of the Infineon reference is the increase of f_T by about 25% due to an advanced vertical doping profile. Nevertheless, the main effect of the EBL process on f_{MAX} is the marked reduction of R_B relative to the Infineon reference value of a conventional DPSA-SEG process. Already for the BEC configuration of the EBL HBT, a decrease of

the length-specific input resistance ($R_B + R_E$) by 40% relative to the Infineon reference is observed. Similar relations are true also of the BEBC BiCMOS device. It should be stressed at this point again how important identical RF transistor layouts, measurement tools, and extraction procedures are for reliable evaluations. For example, ($R_B + R_E$) values given in Table 1.2 are extracted from y_{11} circle fit. This leads to 17% lower values compared to the procedure applied in [Fox 11] based on a circular fit of s_{11} .

Considering the high-frequency behavior of the HBTs, promising results were demonstrated with respect to a reduced base link resistance. However, the f_T of 240 GHz realized for the EBL module within Infineon's 130 nm BiCMOS platform is significantly below the ambitious targets for next SiGe HBT generation. Certainly, the effect of a higher thermal budget of the post-HBT BiCMOS steps at Infineon compared to those of the original IHP flow has to be considered. In addition, more aggressive EB and BC doping profiles have to be applied for further f_T enhancement.

It remains the question whether there are architecture- or flow-related reasons which make it more difficult or impossible to approach the performance values presented in the section "Optimization towards 700 GHz f_{MAX} " for the NSEG HBT also with the EBL concept. However, the finally achieved enhanced high-frequency parameters of the NSEG HBT were paid partially with increased process complexity. The search for an HBT architecture and corresponding process flow which combine best performance and reliable, cost-effective processing is in this context of continuing interest.

1.3.2 Non-selective Epitaxial Growth of the Base

Non-selective epitaxial growth of the SiGe base layer is widely used in SiGe HBT fabrication. Examples are production processes of IBM/Globalfoundries [Orn03, Pek14] and TowerJazz [Pre11] as well as several technology generations developed by IHP [Kno04, Hei07, Rue10] and by NXP and imec [Don07, Huy11]. These processes have in common a layer stack consisting of a Si buffer layer, a SiGe layer containing the boron-doped base, and a Si cap layer deposited across the whole wafer. This layer stack grows mono-crystalline in active HBT areas where the Si surface is exposed while it grows poly-crystalline in all other areas covered with oxide or nitride. This so-called differential growth mode is in contrast to the SEG where the deposition occurs only in the exposed Si regions.

An implication of the non-selective growth mode is that the poly-crystalline layer which is grown on the isolation layers adjacent to the active HBT can be used to form the extrinsic base regions. Typically this approach

is combined with an additional ion implantation into the extrinsic base regions to enhance their conductivity. This approach was applied, e.g., in the 0.25- μm BiCMOS process SG25H1 of IHP which provides peak f_T/f_{MAX} values of 180 GHz/220 GHz [Hei07]. In such an approach, the thickness of the extrinsic base is defined by the layer stack grown to form the intrinsic base. This limits the achievable sheet resistance of the extrinsic base and in particular the conductivity of the extrinsic base region below the poly-emitter overhang. That is why several approaches have been developed to enhance the conductivity of the extrinsic base region by deposition of additional Si layers. It turned out that those elevated extrinsic base regions were necessary for extending f_{MAX} of NSEG HBTs beyond 300 GHz. An NSEG process with elevated extrinsic base regions self-aligned to the emitter window is used, e.g., in IBM's 90 nm SiGe BiCMOS technology [Pek14] exhibiting peak f_T/f_{MAX} values of 300 GHz/360 GHz. In a variant of the process, the RF performance could be further improved to f_T/f_{MAX} of 285 GHz/475 GHz with the help of millisecond annealing [Liu14].

An alternative NSEG HBT process with elevated extrinsic base regions is used in IHP's 130 nm BiCMOS technology [Rue10, Rue12]. This HBT concept was the starting point for the performance optimization toward 500 GHz f_{MAX} performed in the DOTFIVE project. It turned out to be a promising concept for even further performance improvement in the DOTSEVEN project. In the following, we review the main features of the corresponding HBT process flow. The elevated extrinsic base regions are formed by an additional epitaxial step after emitter structuring as first published in [Rue03]. The implementation described below corresponds to the technology SG13G2 of IHP offering HBTs with f_T/f_{MAX} /gate-delay values of 300 GHz/450 GHz/2.0 ps.

A schematic cross section of the HBT is shown in Figure 1.12. Key device features are: (1) Elevated extrinsic base regions self-aligned to the emitter window resulting in low extrinsic base resistance R_{BX} . (2) Formation of the whole HBT structure in one active area without STI between emitter and collector contacts resulting in low collector resistance and small collector-substrate junction areas. (3) Device isolation without deep trenches resulting in reduced process complexity and improved heat dissipation.

Different stages of the HBT process are illustrated in Figure 1.13. The fabrication of the HBT module begins with the formation of the collector regions by high-dose ion implantation. The collector regions are laterally confined by shallow trench regions without introducing additional deep trenches [Hei02]. Active collector regions are defined by deposition and patterning

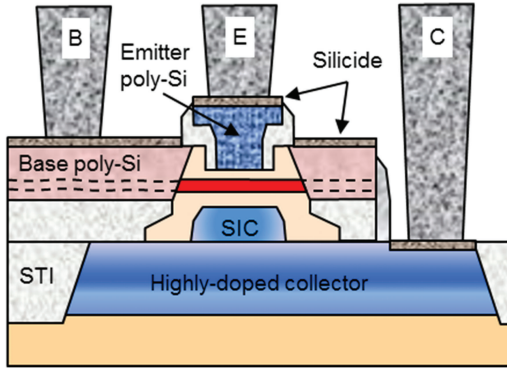


Figure 1.12 Schematic cross section of an NSEG HBT with elevated extrinsic base regions.

an oxide layer. The opened windows in this isolation oxide layer are filled by SEG of un-doped Si on the exposed collector areas. Next, selectively implanted collector (SIC) regions are formed via a patterned resist mask. A cross section of the HBT at this stage of the process is shown in Figure 1.13(a). Now, the non-selective growth of the base is performed. The layer stack consists of a Si buffer layer, the SiGe:C base layer, and a Si cap layer. It grows mono-crystalline in active collector regions and polycrystalline on top of the isolation oxide as indicated in Figure 1.13(b). After epitaxy, an oxide/nitride/oxide layer stack is deposited and emitter windows

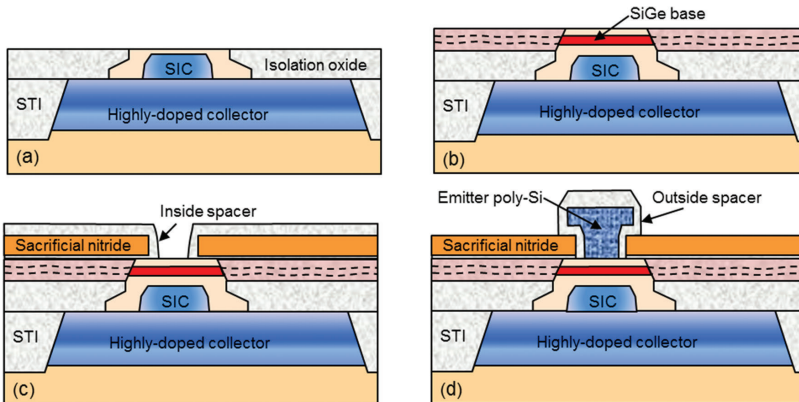


Figure 1.13 Process sequence for the NSEG HBT with elevated base regions: (a) after SIC formation, (b) after non-selective growth of the base, (c) before emitter deposition, (d) after emitter structuring.

are structured. Additional inside spacers are formed before depositing and structuring the As-doped emitter. Figure 1.13(c) shows the device cross section before emitter deposition. The emitter is capped with a dielectric layer and structured via a patterned resist mask. Outside spacers are formed on the emitter resulting in the device structure shown in Figure 1.13(d). Next, the sacrificial nitride layer is removed by wet etching followed by the selective growth of the B-doped elevated extrinsic base regions. The fabrication of the HBT module is continued with the patterning of the base poly-Si layer via a further resist mask. After the described process sequence for HBT structuring, the devices are exposed to a final rapid thermal processing (RTP) step which is used in the BiCMOS flow for the activation of source and drain regions. In the reference technology SG13G2 a spike anneal at 1,050°C is applied for this purpose. Finally, cobalt salicidation is performed on all contact areas and the aluminum metallization is processed. A schematic cross section of the final HBT structure is depicted in Figure 1.12.

The TEM cross section in Figure 1.14 shows an NSEG HBT with elevated extrinsic base regions from the SG13G2 BiCMOS process. The geometrical width of the emitter window of the final device is 120 nm. The elevated extrinsic base regions are separated from the emitter window by about 25 nm wide oxide spacers. This device construction facilitates the realization of very low extrinsic base resistances R_{Bx} due to the self-aligned positioning of the elevated extrinsic base to the emitter window and the high conductivity of the crystalline regions of the extrinsic base near the emitter. However, it has to be noted that the NSEG flow presented here exhibits a significantly lower degree of self-alignment than the DPSA-SEG and EBL process flows discussed in the section “Selective Epitaxial Growth of the Base.”

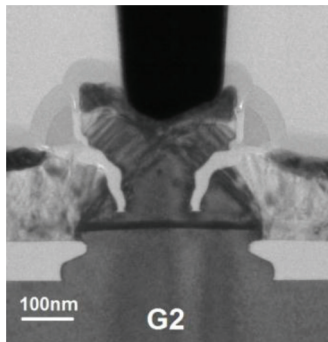


Figure 1.14 TEM cross section of an NSEG HBT of the technology SG13G2.

In particular, the collector window, the SIC implantation, the emitter window, and the emitter poly overhang are not self-aligned to each other. Their relative alignment is defined by the alignment accuracy of the respective lithographic mask steps. This sensitivity to the accuracy of the lithographic alignment can impose severe limitation for further scaling of lateral device dimensions.

Regardless of the above-mentioned limitations of the described NSEG HBT process with respect to self-alignment and scalability, it served as workhorse for optimizing the HBT performance by IHP within the projects DOTFIVE and DOTSEVEN. This arose from the greater experience and familiarity with the NSEG HBT compared to concepts with selective epitaxy discussed above. The fabrication of the NSEG HBT in the SG13G2 BiCMOS process resulted from intensive optimization of this transistor concept within the DOTFIVE project [Hei10]. This raises the question if and by what means further potential performance improvements could be achieved. According to device simulation, there are still respectable reserves for speed increase [Sch11a, Sch11b]. In particular, lateral scaling should help to increase f_{MAX} further. In addition, an appropriate vertical scaling of the doping and Ge profile is required for the desired objective of balanced high f_{T} and f_{MAX} values.

1.4 Optimization of the Vertical Doping Profile

Optimized device architectures as well as lateral and vertical scaling contributed to noticeable progress for f_{MAX} over the last years. In contrast, the potential for improving f_{T} seemed to be limited, in particular, if high f_{MAX} values have to be retained. All successful attempts to push the peak f_{T} of SiGe HBTs beyond 350 GHz delivered rather low f_{MAX} values. For example, the SiGe HBT which demonstrated the highest f_{T} until 2015 showed a peak f_{T} value of 410 GHz together with a peak f_{MAX} value of 190 GHz [Gey08].

Within the DOTSEVEN project, we considered two directions toward HBT performance optimization. First, we focused on aggressive scaling of vertical HBT doping and Ge profiles for increased f_{T} . Second, a device architecture and process flow with a balanced $f_{\text{T}}-f_{\text{MAX}}$ design at highest performance level was aimed for. In the following, we describe the main results of the experiments for f_{T} optimization.

Various vertical doping and Ge profiles were investigated in a simplified HBT flow described in [Kor15]. In these experiments, a reduced thermal budget of the HBT process was utilized for limiting dopant diffusion. Lateral device dimensions were relaxed with respect to the reference process

SG13G2 in order to reduce process complexity. Measured f_T and f_{MAX} vs. collector current density are plotted in Figure 1.15 for the optimized vertical profile. The peak f_T values could be increased to 430 GHz together with peak f_{MAX} values of 315 GHz [Kor15]. These results were achieved for an HBT with a BEC layout configuration sketched in Figure 1.16(a). This layout corresponds to the standard HBT configuration in the SG13G2 reference process. It was optimized for the special collector construction without STI between collector contact and active emitter area. For better comparability with the results of 2D device simulations presented below, we have also investigated devices with CBEBEC layout configuration sketched in Figure 1.16(b).

A further objective of these investigations in the DOTSEVEN project was the assessment of the accuracy of theoretical performance predictions from state-of-the-art device simulations based on the comparison of simulated and

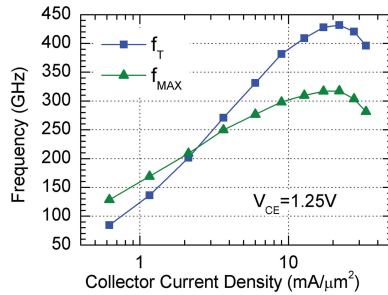


Figure 1.15 f_T and f_{MAX} vs. collector current density for an HBT with BEC layout configuration. Eight HBTs in parallel with individual emitter areas of $0.17 \times 1.01 \mu\text{m}^2$ were measured [Kor15].

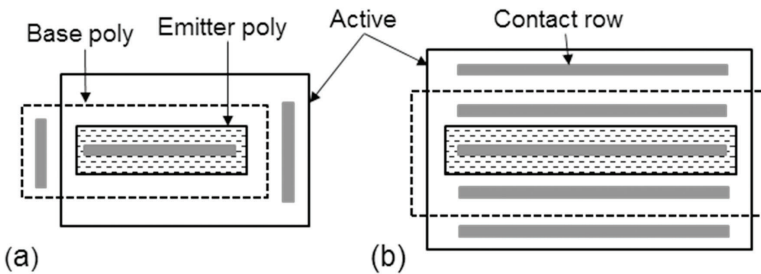


Figure 1.16 Layout configurations: (a) BEC configuration with base and collector contacts at the ends of the emitter line, (b) CBEBEC configuration with base and collector contact rows parallel to the emitter line.

measured electrical data. For this purpose, it is essential to determine doping profiles, material compositions, and device geometries of the experimental reference structures as accurately as possible. Below, we summarize the results of the experimental profile characterization.

A combination of various analytic techniques was used to characterize the vertical profiles including secondary ion mass spectroscopy (SIMS), X-ray diffraction (XRD), and energy dispersive X-ray spectroscopy (EDX). The impact of the thermal budget of the fabrication process on the B and Ge profiles of the HBT is shown in Figure 1.17(a). The major part of the observed profile broadening occurred during the final spike rapid thermal processing (RTP) with 1,030°C peak temperature. The B profile experienced only a moderate broadening due to the suppression of B diffusion by Ge and C. However, significant diffusion is observed for the Ge profile itself resulting in a reduction of the peak Ge concentration from 32 at % in the as-grown layer to 28 at % in the final structure.

The accurate determination of doping and Ge profiles in actual HBT structures represents an additional challenge. Width and doping concentrations of epitaxial layers depend in general on the size of the exposed Si area. However, SIMS measurements require dimensions which are much larger than typical active HBT areas. We have performed EDX measurements of the Ge depth profiles in typical HBT structures and in large windows of $600\ \mu\text{m} \times 400\ \mu\text{m}$ which were also used for SIMS measurements (Figure 1.17(b)). The width of the epitaxial SiGe layer was found to be 14%

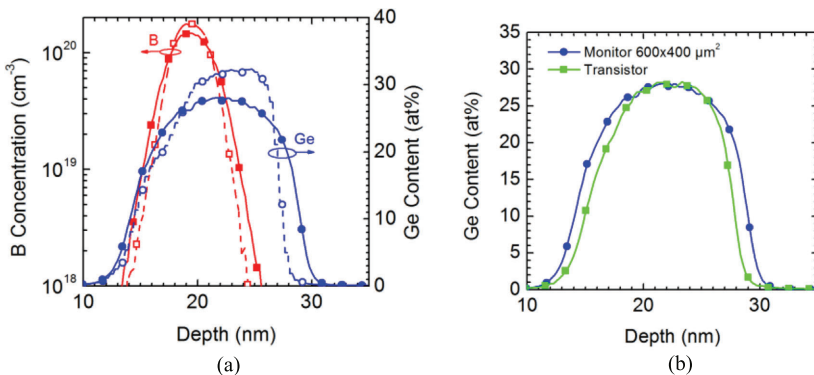


Figure 1.17 (a) Depth profiles of Ge (blue circles) and B (red squares) measured by SIMS. Open symbols are as-grown profiles. Filled symbols are profiles after the full fabrication process. (b) Ge depth profiles measured by EDX in a $600\ \mu\text{m} \times 400\ \mu\text{m}$ window (blue) and in a typical HBT structure (green).

smaller in the small HBT window while about the same peak Ge concentrations were measured in both structures. The Ge profile of the small window can be obtained from the Ge profile in the SIMS monitor by shrinking the depth scale by 14%. We assume that the same shrink of the depth scale applies to the B profile resulting in a 14% thinner profile in the small HBT window.

The measured emitter, base, and collector profiles of the final HBT structure are plotted in Figure 1.18. The theoretically proposed doping profile corresponding to generation N3 of [Sch17] was included in Figure 1.18 for comparison. This profile N3 was proposed for an HBT generation with peak f_T values of about 500 GHz. The measured and the theoretical N3 profiles show similar widths of the base and of the EB and BC junctions. The steep increase of the theoretically proposed collector profile toward 10^{20} cm^{-3} was not realized in the experiment due to limitations in the formation of low-defective high-dose SIC profiles.

The extracted doping and Ge profiles were used as input for 1D device simulations with the Boltzmann transport equation (BTE) solver [Hon09] and for 2D simulations with the hydrodynamic (HD) transport model [Kor17]. For a quantitative comparison between simulation and experiment, all relevant features of the HBT must be represented adequately by the 2D structure. To accomplish this task, the widths of the EB and BC depletion regions were adjusted to meet the measured area-specific capacitances C_{BEj} and C_{BCj} . The extent of boron diffusion from the external base as well as the lateral extent of the SIC were tailored in such a way that the measured edge capacitance C_{BEe} and C_{BCE} are reproduced [Kor17]. The 2D geometry of the simulated device was adjusted to the TEM cross section of the measured device.

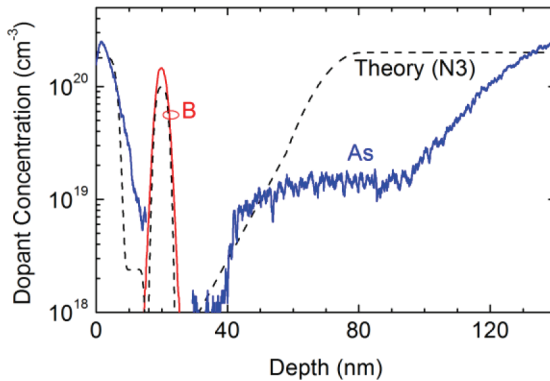


Figure 1.18 SIMS profiles measured after the final annealing step. The theoretically proposed doping profile N3 of [Sch17] is shown for comparison.

Measured and simulated transit frequencies f_T are plotted in Figure 1.19. At low and medium current densities, the simulated f_T values agree well with the measurement. However, at high I_C , the simulation markedly deviates from the measured curve. The degradation of f_T starts at lower I_C and is less abrupt in the simulation, leading to an about 11% smaller peak f_T . Further investigations are needed to clarify this deviation. Additionally, 1D HD and BTE simulations of the inner transistor were performed in [Kor17]. The simulated peak f_T of the 1D transistor is about 80% higher than the corresponding 2D value due to the absence of peripheral capacitances and resistances as well as self-heating. These simulation results indicate that a further enhancement of f_T can be expected for the given vertical profile when contributions of the device edges to the EB and BC capacitances and parasitic resistances are reduced.

1.5 Optimization towards 700 GHz f_{MAX}

In this section, we review attempts in the DOTSEVEN project to optimize the device structure and the fabrication process of the NSEG HBT for highest RF performance. The starting point for this optimization was the SG13G2 technology. The investigated process modifications addressed the reduction of device parasitics by reducing lateral device dimensions as well as by

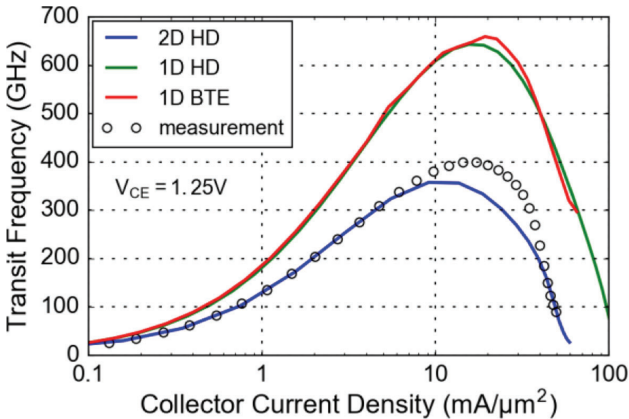


Figure 1.19 Measured and simulated f_T vs. collector current density [Kor17]. Simulations were performed with the hydrodynamic model in 2D and 1D. Results obtained from the 1D Boltzmann transport equation are shown for comparison. The measured device has an emitter area of $0.28 \mu\text{m} \times 5.0 \mu\text{m}$ and the CBEB layout corresponding to Figure 1.16(b).

improving the control of the doping profile and the conductivity of critical device regions.

The possibilities for lateral scaling of the emitter window by lithographic measures were already largely exhausted in the SG13G2 technology due to the resolution limits of the DUV tool at IHP. A further challenge for down-scaling of the emitter window width is the fabrication of conformal inside spacers in narrow emitter windows. This concerns in particular the deposition of homogenous dielectric layers with good step coverage and the reactive ion etching with minimum damage of the Si surface. Finally, we had to learn from a series of development loops that the room for a well-controlled down-scaling of the emitter width was very limited within the current process flow. Starting from a value of 120 nm in SG13G2, the emitter width was reduced to 100 nm in an intermediate process variant (split CR2). For the final device optimization, an emitter width of 105 nm was realized.

First, we discuss the process stage that was used for circuit fabrication in the DOTSEVEN project. After using the SG13G2 technology for a first circuit fabrication run, an HBT process with improved RF performance was targeted for a second circuit fabrication run (CR2). The following process changes were addressed in this split: smaller emitter–base spacers and smaller emitter window widths were formed by modifying the corresponding deposition and etching processes. An emitter deposition process with enhanced As concentration previously explored in [Hei10] was introduced. The doping concentration of the epitaxially elevated base link regions was enhanced and a new base profile was applied. In addition to these measures which are compatible with the SG13G2 BiCMOS process, we explored for further optimization of the HBT performance process changes which are in conflict with the reference BiCMOS flow. The thickness of the cobalt silicide was increased and the thickness of the silicide blocking spacer at the sidewall of the emitter poly-Si was reduced to minimize the external base resistance. The peak temperature of the final RTP step was reduced in order to minimize diffusion broadening of the base and consequently the base transit time. The HBT cross sections depicted in Figure 1.20 indicate the decreased emitter window width, the reduced widths of the base–emitter and silicide blocking spacers, and the enhanced CoSi_2 thickness of the split CR2 with respect to the reference process SG13G2 (G2).

Electrical device parameters for the investigated process variants are summarized in Table 1.3. The process developments introduced in the CR2 split resulted in significant improvements of f_T , f_{MAX} , and the CML ring oscillator gate delay compared to the reference process G2 (Table 1.3).

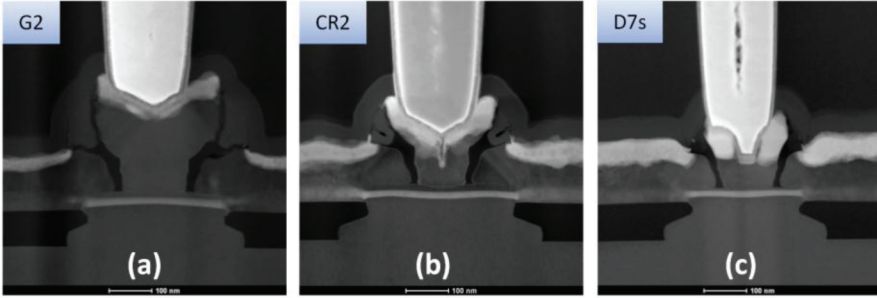


Figure 1.20 TEM cross sections of HBTs from the process splits G2 (a), CR2 (b), and D7s (c).

Table 1.3 HBT parameters of different process splits

	Unit	Measuring Condition						
			G2	CR2	G2N	G2NF	D7	D7s
No. emitters			8	8	8	8	8	8
w_E	μm		0.12	0.10	0.12	0.12	0.105	0.105
l_E	μm		1.02	1	1.02	1.02	1	1
f_T	GHz		314	351	325	331	498	505
f_{MAX}	GHz	$V_{CB} = 0.25 \text{ V}$, $T = 300 \text{ K}$	414	526	461	510	671	720
$j_C @ \text{peak } f_T$	$\text{mA}/\mu\text{m}^2$		20.3	26.3	19	20.6	31.9	34.4
C_{BC}	fF	s -parameter	14.7	15.0	14.8	14.5	15.7	15.1
C_{BE}	fF	s -parameter	20.6	19.2	21	20.8	20.3	20.4

Reduced emitter and base resistances of CR2 devices were facilitated by enhanced dopant concentration of the revised deposition processes for the emitter and the extrinsic base. For this analysis, we extracted the emitter resistance (R_E) from simple fly-back measurements [Get78]. The impact of the different process splits on base resistance (R_B) is assessed on the basis of $R_B + R_E$ values extracted from circle fits of s_{11} . The modified SiGe base epitaxy is an additional source for the improved RF parameters of the CR2 split. The increase of the Ge content enabled higher collector current densities leading to higher f_T values. A smaller base-emitter junction width and a reduced spike temperature of the final RTP created a more aggressive vertical profile compared to G2. Higher f_T values were obtained but at the cost of a decreased base-emitter breakdown voltage BV_{EB0} . The reduced base sheet resistance R_{SBI} of the split CR2 supported a further reduction of the base resistance and higher f_{MAX} values. Figure 1.21 shows a comparison of f_T and f_{MAX} as a function of collector current density for the splits G2 and CR2.

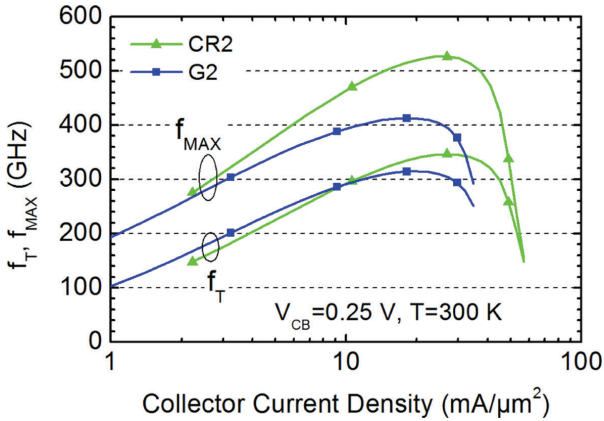


Figure 1.21 Transit frequency f_T and maximum oscillation frequency f_{MAX} vs. collector current density for devices of the split CR2 (second circuit fabrication run in DOTSEVEN) compared to the reference process G2. Device dimensions are given in Table 1.3.

Next, we investigated the potential of enhanced dopant activation by millisecond annealing and low-temperature BEOL processing for further performance improvement. Their benefit for SiGe HBTs has already been pointed out in [Liu14]. Millisecond annealing with laser or flash lamp techniques facilitates a very high level of dopant activation with almost no diffusion. In order to take full advantage of this high activation level, subsequent process steps have to be kept at sufficiently low temperatures to avoid dopant deactivation. Within the DOTSEVEN project, we exploited a non-commercial flash lamp annealing tool at the Helmholtz-Zentrum Dresden-Rossendorf, Germany. Peak temperatures beyond 1,200°C could be realized. A modified contact formation and nickel silicidation were applied to decrease the maximum temperature after flash annealing below 500°C. Cobalt silicide formation does not meet this requirement. In contrast, the nickel silicide fabrication widely used in advanced CMOS nodes does not need annealing above 500°C.

The impact of these processes on HBT performance was investigated in [Hei16] by two process splits of the G2 process. For the split G2N (Table 1.3), the original cobalt silicide process was replaced by a nickel silicide process and the temperature of the contact formation process was reduced. In addition, a flash annealing step was introduced before silicidation in the split G2NF. Figure 1.22 demonstrates the impact of these two process modifications on f_T and f_{MAX} . Markedly enhanced f_{MAX} values by 15%

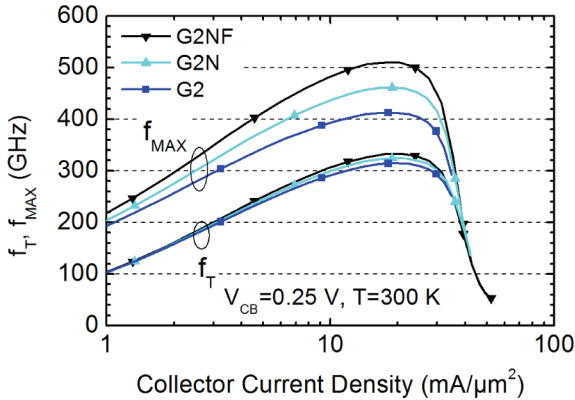


Figure 1.22 Transit frequency f_T and maximum oscillation frequency f_{MAX} vs. collector current density for devices of the split G2N (nickel silicide) and G2NF (nickel silicide and flash annealing) compared to the reference process G2 [Hei16]. Device dimensions are given in Table 1.3.

and 23% compared to G2 were obtained for the G2N and G2NF process splits, respectively. These improvements are mainly attributed to reduced base and emitter resistances due to the high level of dopant activation supported by reduced dopant deactivation during silicidation and BEOL processing and by enhanced activation due to flash annealing. Breakdown voltages and junction capacitances are hardly affected by these process modifications (see Table 1.3).

The final optimization stage performed in the DOTSEVEN project [Hein16] is represented by the split D7 in Table 1.3. The scaled device D7s corresponds to the same process flow. There, the width of the collector window is reduced by 17% and the width of the emitter poly-Si is reduced by 33% with respect to device D7 resulting in somewhat lower R_B and C_{BC} . A cross section of the final NSEG HBT is presented in Figure 1.20(c). Regarding the emitter-window and emitter-base spacer width, the situation is very similar to the interim case CR2. For this HBT, an emitter width of 105 nm was determined. The geometric dimensions of the revised versions also suggest that limits were reached for further decrease of the width of the EB spacers and of the emitter-poly overlap to the emitter window.

The D7 process split combines the above introduced process modifications of an improved EB spacer process, an extrinsic base with enhanced conductivity, nickel silicidation, and flash annealing with the following additional amendments. A further optimized SiGe base epitaxy is applied which

closely resembles the B and Ge profiles of the f_T -optimized device described in the section “Optimization of the Vertical Doping Profile.” The thicknesses of the lower doped parts of the emitter–base and base–collector junctions are reduced with respect to split CR2. The emitter utilizes the enhanced doping level but now with reduced layer thickness. Furthermore, the fabrication process for the SIC was revised. In the G2 HBT flow, the SIC was formed with the help of a patterned resist mask. In the D7 split, this process sequence was replaced by a hard mask with inside spacers. By this means, we gained additional flexibility in matching the lateral dimensions of the SIC and the emitter window. The implantation dose of the SIC was doubled in the split D7 with respect to the reference process G2.

Figure 1.23 illustrates the measurement procedure for the extraction of f_T and f_{MAX} for the device D7s. The small-signal current gain h_{21} and the unilateral gain U were derived from s -parameter measurements up to 50 GHz and plotted as a function of frequency. The f_T and f_{MAX} values are obtained from averaged values around an extrapolation frequency of 40 GHz assuming a gain decay of -20 dB per frequency decade. The quality of the measurement procedure was confirmed by independent measurements at IHP and at Infineon as described in [Hei16].

Figure 1.24 shows f_T and f_{MAX} values of the devices D7 and D7s as a function of collector current density. Data for the previous device generations G2 and CR2 are included for comparison. The optimized D7 process reveals

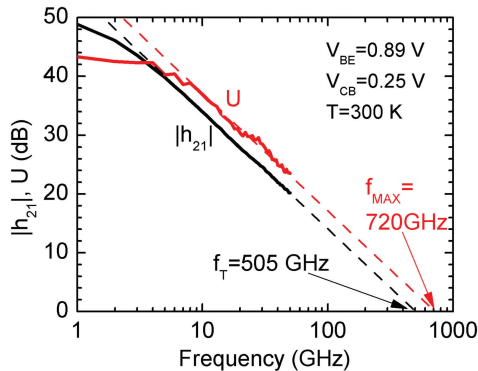


Figure 1.23 De-embedded small-signal current gain h_{21} and unilateral gain U vs. frequency of the device D7s used for extraction of transit frequency f_T and maximum oscillation frequency f_{MAX} with -20 dB decay per frequency decade [Hei16]. The emitter area is $8 \times (0.105 \times 1.0) \mu\text{m}^2$.

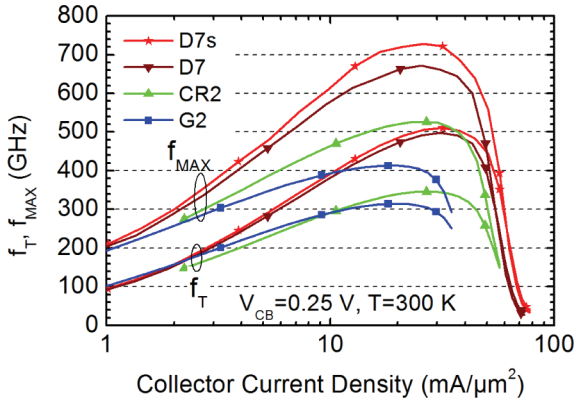


Figure 1.24 Transit frequency f_T and maximum oscillation frequency f_{MAX} vs. collector current density for two device geometries (D7 and D7s) of the latest process status of DOTSEVEN compared to the reference process G2 and the split CR2 [Hei16]. Device dimensions are given in Table 1.3.

a strong enhancement of both f_T and f_{MAX} . The obtained high f_T values are supported by reduced transit times for the aggressively scaled vertical doping profile and by strongly reduced R_E values which are accompanied by a strong enhancement of the transconductance g_m in the high current regime. Highest peak f_T/f_{MAX} values of 505 GHz/720 GHz were measured for the scaled device D7s [Hei16]. Both of these values represent the state of the art for SiGe HBTs.

CML ring oscillator gate delays are plotted in Figure 1.25 as a function of current per gate. The oscillators consist of 31 stages and a 1:16 frequency divider. Currents per stage were adjusted to a single-ended voltage swing ΔV of 300 mV at a supply voltage V_{EE} of -2.5 V. The circuits use conventional resistive loads and do not apply special circuit techniques such as inductive peaking. The data plotted in Figure 1.25 for four of the device splits discussed above demonstrate that the improvement of f_T and f_{MAX} for the devices D7 and D7s is associated with significantly reduced gate delay times. The minimum gate delay of 1.34 ps for device D7s represents the shortest gate delay that has been reported so far for a SiGe HBT technology [Hei16]. Until now, shorter gate delays have not been reported for any other integrated circuit technology.

The aggressive lateral and vertical scaling for the D7 split resulted in reduced base-emitter and base-collector breakdown voltages as indicated in Table 1.3. In addition, Figure 1.26 illustrates a degradation of the base

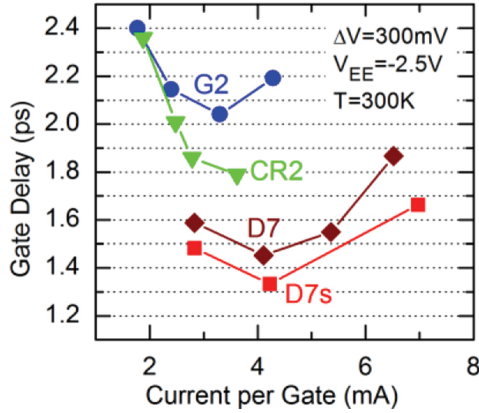


Figure 1.25 CML ring oscillator gate delays vs. current per gate for oscillators consisting of 31 stages with single-emitter HBTs for the splits G2 ($A_E = 0.12 \mu\text{m} \times 1.02 \mu\text{m}$), CR2 ($A_E = 0.1 \mu\text{m} \times 1.0 \mu\text{m}$), D7, and D7s ($A_E = 0.105 \mu\text{m} \times 1.02 \mu\text{m}$) [Hei16].

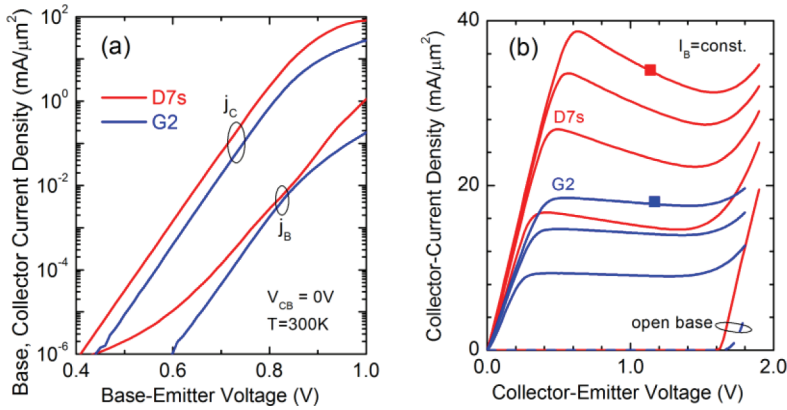


Figure 1.26 Gummel characteristics (a) and base-current forced output characteristics (b) for the splits D7s and G2. Symbols in (b) indicate the bias points for peak f_T . The emitter areas are $8 \times (0.12 \times 1.02) \mu\text{m}^2$ for G2 and $8 \times (0.105 \times 1.0) \mu\text{m}^2$ for D7s [Hei16].

current ideality factor n_{IB} and stronger self-heating for the device D7s. We suppose that a further optimization of the EB doping profile and process advancement for an improved alignment of the SIC to the collector window will weaken some of these drawbacks in future. In fact, excellent DC characteristics have already been demonstrated for devices with nearly 600 GHz f_{MAX} in [Hei16].

1.6 Summary

Due to the intensive work in the projects DOTFIVE and DOTSEVEN, a new high-speed performance level of SiGe HBTs has become a reality. Most valuable is the fact that not only f_{MAX} and the ring oscillator gate delay are improved significantly, but also a new f_{T} record is demonstrated for the same transistor. The balanced increase of f_{MAX} and f_{T} toward 700 GHz and 500 GHz, respectively, makes these devices attractive for an even wider range of RF, mm-wave and sub-mm-wave applications.

These improvements were achieved for the most part by optimization of the vertical profile, the SIC formation, and the reduction of the external resistances. A lower thermal budget in the BEOL processing or its combination with millisecond annealing can produce an extra performance increase due to an enhanced level of dopant activation. Apart from variations of the collector window or the emitter poly-Si overlap, the potential of a comprehensive lateral scaling was not exhausted. Besides adequate lithographic capabilities, this requires advanced conformal deposition and damage-less etching techniques as well as well-controlled epitaxial processes for the SiGe base in small windows.

The modifications applied here for pushing the HBT performance toward 700 GHz f_{MAX} did not consider the compatibility to any frozen CMOS or BiCMOS process. Additionally, we did not shrink back from additional processing steps as long as noticeable performance enhancement seemed possible and process safety was ensured. Consequently, it is concluded from the present results that the feasibility of the DOTSEVEN device targets is demonstrated but the challenging task to implement these capabilities in a next BiCMOS production technology has still to be done. It is an enormous challenge to integrate these HBTs in an advanced CMOS process with its tight constraints on thermal budget and device topology while reaching a similar HBT performance level and fulfilling simultaneously the industrial needs of simplicity, robustness, and high yield.

It was the intention of IHP and Infineon in the DOTSEVEN project to investigate whether the HBT module with EBL could be a promising candidate for this task. As a result, two major directions for next steps could be derived: (a) Transfer of performance enhancing modifications which were tested successfully in the NSEG concept to the SEG EBL flow and (b) revision of the flow to enable further down scaling of the emitter window and to improve process safety under a production-like BiCMOS environment.

The demonstration of a new SiGe HBT performance level should stimulate device engineers and technology developers to create further ideas for cost-effective process flows with best performance potential. In this context, technological challenges related to non-selective or selective base epitaxy and partial or full self-alignment of the HBT layers need to be reinvestigated under the process constraints of advanced CMOS technology nodes.

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