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Self-Consistent Determination of Interface and Bulk Parameters of Oxide/Si/SiGe/Si Layer Stacks by Means of Simultaneous Measurement of Gate Current and High Frequency Gate Capacitance in Non-Steady State Non-Equilibrium.

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Abstract

Heteroepitaxy of group IV materials (Si, SiGe, and Ge) has great potential for novel Si-based sensor devices. We report on a self-consistent extraction of surface and bulk MOS parameters for the optimization of the growth parameters of epitaxial Si/SiGe/Si-layer stacks used for strain sensor applications. Beside the MOS surface and bulk parameters such as interface state density $D_{it}(E_t)$ and the generation lifetime $\tau_g(x_g)$ rapid simultaneous measurements of $I_g(V_g)$ and $C_{hf}(Vg)$ in non-steady state non-equilibrium enable the extraction of the current voltage characteristic $I_{rec,gen}(\Delta\psi_s)$ of the field induced pn junction for the optimization of growth conditions of the low temperature LPCVD epitaxy process considered in this study. An appropriate choice of sample temperature and gate voltage ramp rate enables a convenient adjustment of the desired non-steady state non-equilibrium for the measurements.

I. Introduction

Strain sensors are highly demanded in social and industrial fields such as health care sensing via heartbeat, pulse, breathing and the capability of industrial robots for handling of soft materials and recognizing the state of grabbed objects with high-resolution [1,2]. In order to realize strain sensor integration into Si-based platforms with high sensing capability, the use of low-noise and high sensitivity materials is essential. Heteroepitaxy of SiGe on Si is a potential candidate for the fabrication of such layer stacks. Minimal fluctuation of device properties can be obtained by switching from polycrystalline to single crystal growth. The density of point defects and dislocations strongly affect the crystal quality of epitaxial SiGe layers. Thus, the evaluation of electrically active defects in the layer stack is essential for the optimization of the SiGe growth conditions. MOS structures with metallic, poly-silicon or mercury gate electrodes are widely used for the characterization of important process modules such as cleaning, epitaxy, oxidation, implantation and anneals. However, the successive application of the various MOS CV techniques in thermal equilibrium or steady state non-equilibrium for the determination of MOS parameters such as oxide thickness t_{ox}, flatband voltage V_{fb}, density of fixed oxide charges N_f, doping profile $N(x_d)$, density of interface states $D_{it}(E_t)$ and the generation lifetime $\tau_g(x_g)$ is extremely time consuming. In contrast, MOS CV measurements in non-steady state non-equilibrium can meet the requirements for an extensive and rapid characterization of epitaxial SiGe layer stacks. Non-steady state non-equilibrium is defined by a state between the deep depletion condition with negligibly impact of thermal generation and inversion equilibrium where all charges in the MOS system are in thermal equilibrium. Non-steady state non-equilibrium is given as long the amount of inversion charge, formed by thermal generation of minority charge carriers at the surface and in the bulk, still enables a further markable variation of the depletion depth during the measurement. By choice of an appropriate gate voltage signal and a suitable sample temperature non-steady state non-equilibrium can be conveniently adjusted in any case. Rich in structure, simultaneously recorded $I_g(V_g)$ and $C_{g,hf}(V_g)$ characteristics of MOS structures in non-steady state non-equilibrium enable a deep insight into the impact of electrically active defects. The depth of the investigated device volume is given by the reachable depletion depth during recording of a CV sweep. Fig. 1 shows a measurement example of an $Al/SiO_2/Si/SiGe/Si$ layer stack recorded at -40°C at a constant gate voltage ramp rate $R=dV_g/dt$. The pointer A marks the onset of depletion of the Silicon bulk after the Si cap and the SiGe layer were already depleted. The characteristics of the same sample measured at 27°C are depicted in Fig. 2. As can be seen, using the same measurement conditions at 27°C the sample is already in thermal equilibrium, i.e. the maximum depletion depth is dramatically reduced corresponding to a minimum inversion capacitance C_{g,hf_min} as marked by pointer C. In such a measurement mode only the interface state density $D_{it}(E_t)$ can be determined. However, the interesting defect-controlled generation and recombination processes in the entire Si/SiGe/Si layer stack cannot be evaluated in this way. Only MOS CV

sweeps recorded in non-steady state non-equilibrium enable the determination of interface and bulk parameters.

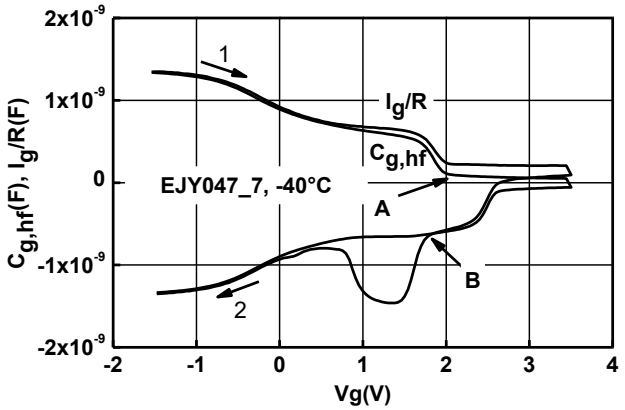

Fig. 1: $I_g(V_g)/R$ and $C_{g,hf}(V_g)$ characteristics of a $Al/SiO_2/Si/SiGe/Si$ layer stack measured in non-steady state non-equilibrium at -40°C.

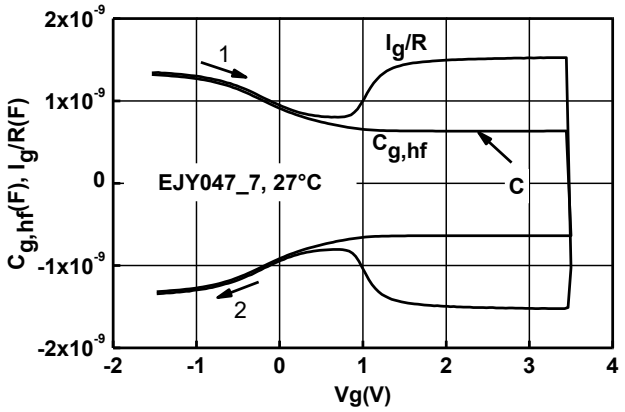

Fig. 2: $I_g(V_g)/R$ and $C_{g,hf}(V_g)$ characteristics of a $Al/SiO_2/Si/SiGe/Si$ layer stack measured in thermal equilibrium at 27°C.

Standard MOS CV equipment, available in any reasonably equipped lab, can be used for the simultaneous measurement of $I_g(V_g)$ and $C_{g,hf}(V_g)$ with high accuracy [3,4]. The gate current Ig measured at a ramp rate R=dVg/dt has two components: 1.: the displacement current through the high frequency small signal gate capacitance $C_{g,hf}$dVg/dt and 2.: additional recombination-generation currents $I_{rec,gen}$ due to charge variations at the semiconductor oxide interface dQ_{it} and in the depletion zone dQ_{inv}.

$$I_g(V_g) = C_{g,hf}(V_g)\frac{dV_g}{dt} + I_{rec,gen}\frac{(C_{ox}-C_{g,hf})}{C_{ox}} \quad (1)$$

$$I_{rec,gen} = \frac{dQ_{it}}{dt} + \frac{dQ_{inv}}{dt} \quad (2)$$

$$\psi_s(V_g) - \psi_{s,ref}(V_{g,ref}) = \int_{V_{g,ref}}^{Vg}\left(1 - \frac{I_g}{dV_g'/dt \cdot C_{ox}}\right)dV_g' \quad (3)$$

In practice two CV sweeps being successively measured. The starting voltage of the first I_g and $C_{g,hf}$ sweeps (see Fig. 1 sweeps No. 1) is in accumulation and the sample is driven from accumulation towards deep depletion. The I_g, and $C_{g,hf}$ characteristics of the second sweeps (see Fig. 1 sweeps No. 2) start in deep depletion. In order to obtain an inversion layer of minority charge carriers beneath the gate oxide before staring the second sweeps the MOS sample was driven into deep depletion and shortly illuminated. This procedure enables an effective screening against charge variations at the oxide semiconductor interface during recording the second CV sweeps. After illumination the gate voltage will be pulsed to the starting gate voltage in even deeper depletion. For the calculation of the generation active depletion depth x_g the equilibrium depletion depth x_f in strong inversion must be determined. x_f can be conveniently obtained from the second CV sweeps where I_g/R and $C_{g,hf}$ do coincide (see pointer B in Fig. 1). This intersection point marks the transition from generation to recombination, defining the origin of the MOS field induced pn junction characteristic $I_{rec,gen}(\Delta\psi_s=0)=0$. The voltage drop along the field induced pn junction is equal to the variation of surface potential $\Delta\psi_s$. $\Delta\psi_s = \psi_s - \psi_{s,ref}$ with $\psi_{s,ref} = \psi_s@ I_{rec,gen}=0$. ψ_s is calculated with Eqn. (3) which is a generalized form of the Berglund integral as used for the calculation of the $\psi_s(Vg)$ characteristic [5].

II. Experimental

Epitaxial growth of SiGe is carried out by using reduced pressure chemical vapor deposition (CVD). First, the epitaxial SiGe of 100 nm is deposited by a H2-SiH4-GeH4 gas system at 600°C as a standard condition. I order to enable a sufficient depth resolution of the MOS CV measurements applied an in-situ B doping of ~10^{17} cm^{-3} is performed by adding B2H6 during the SiGe growth. To prevent a Ge oxide formation at the interface of the MOS structure, a 15nm-thick Si cap is deposited on top of the SiGe immediately after the SiGe growth without exposing air. In order to investigate the influence of Ge concentration, Ge concentration is varied from 5% up to 30% by changing GeH4 partial pressure. To evaluate the impact of growth temperature on the crystallinity, SiGe growth temperature is varied from 550°C – 700°C. Table 1 depicts the variant matrix of 12 wafers processed in the frame of this experiment. After epitaxial growth of the Si/SiGe/Si layer stack a low temperature HDP CVD gate oxide was deposited at 320°C onto the Si cap layer. Then 500nm Al were deposited by a low energy sputter process with 1kW sputter power only. The Al MOS gates with an area of $8.2 \cdot 10^{-3}$ cm^2 were formed by a wet etch step. A 390°C, 30min H2 sinter anneal finished the sample preparation. For probing and tempering the samples standard darkened wafer prober equipment was used. The used setup for MOS CV measurements in non-steady state non-equilibrium is described extensively in [4]. For the MOS samples as listed in Table 1 the 1st and the 2nd CV sweep were measured with a linear gate voltage ramp rate R = dVg/dt = 0.08V/s. The illumination step as part of the second sweep for forming a defined inversion layer before pulsing into deep depletion was performed at Vg=1.6V. The ac small signal frequency for the capacitance measurement was 100 kHz. The ac small signal level was 30mV. All samples were measured at -20°C.

III. Results and Discussion

As expected the trap density D_{it} at the interface between the Silicon cap and the low temperature PECVD gate oxide is strongly increased in comparison to values of some 10^{10} $cm^{-2}eV^{-1}$ one usually obtains with a thermal gate oxide. The interface state density can be determined only in one half of the bandgap. Only interface states in the bandgap range with response on capture and emission of majority charge carriers can be detected. In the bandgap range without sufficient minority charge carrier response D_{it} cannot be evaluated. Fig. 3 shows the determined interface trap density curves extracted from the CV sweeps No. 1 as shown in Fig. 5, measured from accumulation towards depletion. The sample with highest Ge concentration of 30% shows the highest D_{it} midgap level of $3 \cdot 10^{11}$ $cm^{-2}eV^{-1}$. The sample with lowest Ge concentration of 5% shows the best D_{it} midgap level of around $7 \cdot 10^{10}$ $cm^{-2}eV^{-1}$.

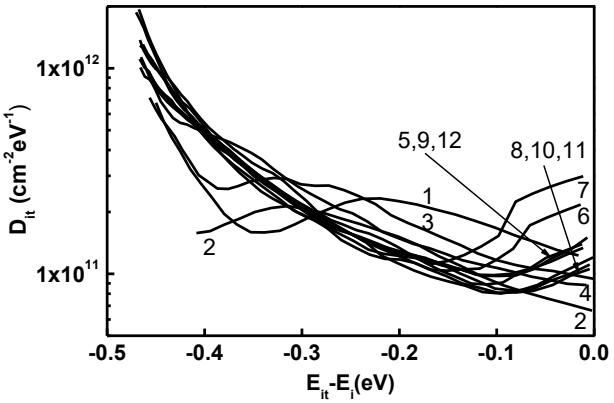

Fig. 3: Interface state density of all 12 devices under test extracted from the $I_g(V_g)/R$ and $C_{g,hf}(V_g)$ characteristics as shown in Fig. 4.

Fig. 4 shows the entire $I_{rec,gen}(\Delta\psi_s)$ characteristics of the field induced pn junction of all 12 Al/SiO_2/Si/SiGe/Si layer stack layer stacks investigated.

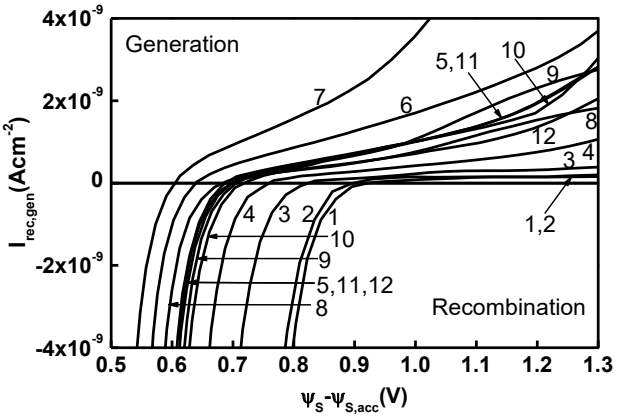

Fig. 4: Recombination Generation current vs. surface potential variation of all 12 devices under test extracted from the $I_g(V_g)/R$ and $C_{g,hf}(V_g)$ characteristics as shown in Fig. 5.

$I_{rec,gen}(\Delta\psi_s)$ is extracted from the MOS CV sweeps No. 2. Starting in deep depletion with predominant generation of electron hole pairs the samples were driven towards accumulation. As long generation predominates the field induced pn junction is reverse biased. After onset of recombination the field induced pn junction gets forward biased. Maximum recombination occurs in a depth where the concentration of electrons coming from the surface and holes coming from the bulk are equal. The $I_{rec,gen}(\Delta\psi_s)$ characteristics were extracted from the measured $I_g(V_g)$ and $C_{g,hf}(V_g)$ characteristics (CV sweeps No. 2 in Fig. 5) using Eqn. 1,2 and 3 with $\psi_{s,ref} = \psi_{s,acc}$. Note that for a better distinction $I_{rec,gen}$ is represented here versus $\Delta\psi_s = \psi_s - \psi_{s,acc}$ which is the variation of the surface potential with reference to a value in strong accumulation. That's why all curves do not coincide at $I_{rec,gen}=0$ which marks the transition from generation to recombination. As an electrical criterion for evaluation of the several technological variants it is useful to consider the slope of each $I_{rec,gen}(\psi_s - \psi_{s,acc})$ characteristic. According the SRH theory applied to the calculation of the forward and reverse characteristics of solid state pn junctions the lowest slope denotes the lowest level of electrically active defects. The small forward bias of the field induced pn junction < 100mV ensures that the condition for low level minority charge carrier injection are fulfilled at the evaluation of recombination. The samples with 25% and 30% Ge show the highest defect level. Up to 10% Ge the defect level is very low and comparable with the Si reference sample. Even the lowest deposition temperature of 550°C still enables outstanding crystal quality of 100nm thick epitaxial SiGe layers.

IV. Summary

MOS C-V measurements in non-steady state non-equilibrium have proven as very useful for the optimization of epitaxial growth conditions of Si/SiGe/Si layer stacks. It can be assumed that this technique can be advantageously applied also for the evaluation of the crystal quality of many other types of epitaxially growth layer stacks.

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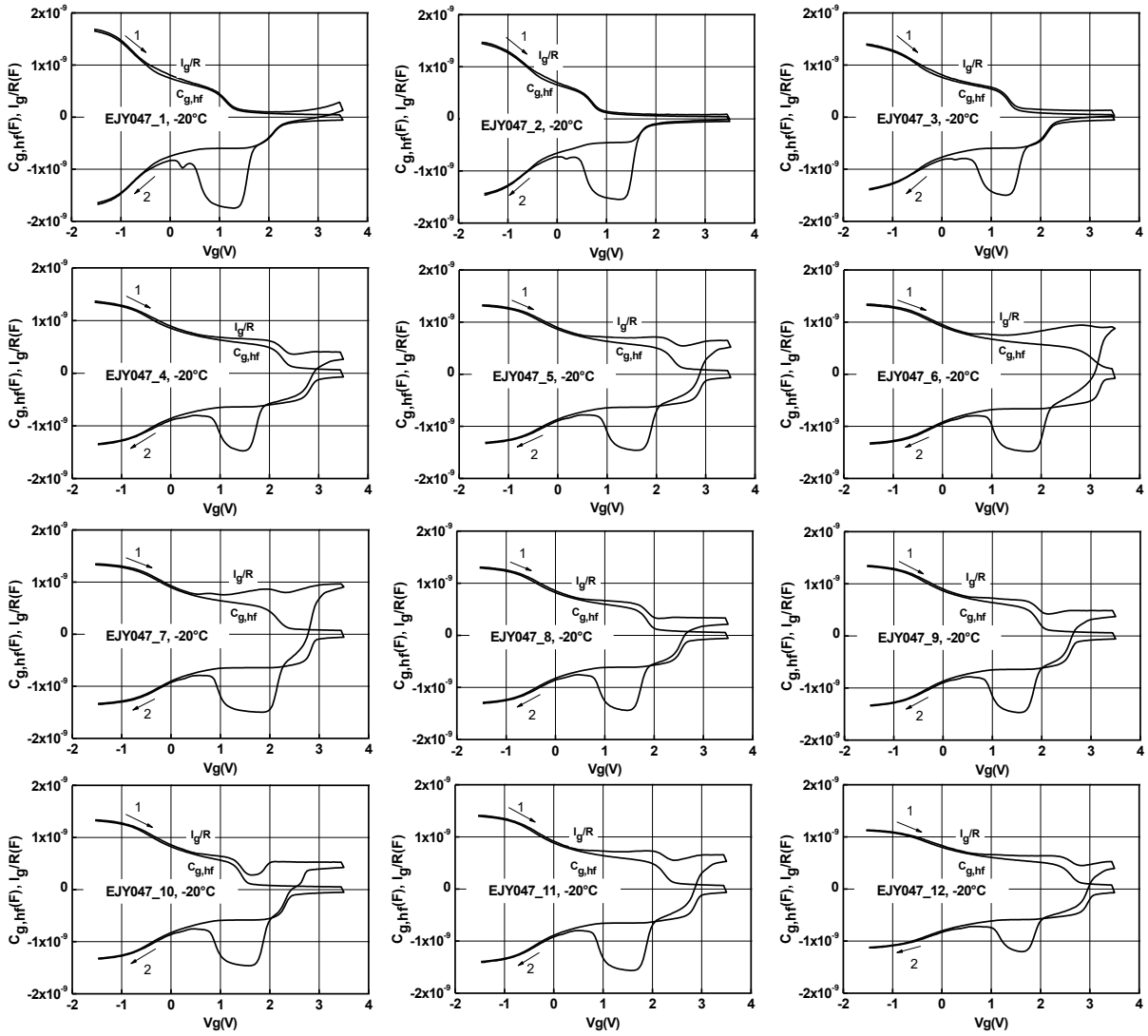

Fig. 5: Ig(Vg)/R and Cg,hf(Vg) characteristics of investigated Al/SiO2/Si/SiGe/Si layer stacks measured in non-steady state non-equilibrium at -20°C based on the experiment matrix as shown in Table 1.

Wafer ID	SiGe Thicness (nm)	Ge (%)	SiGe Temp (°C)	Si cap Thickness (nm)	B conc (cm^{-3})	HDP CVD Oxide Thickness (nm)
EJY047_1	100	0	700	10	10^{17}	15
EJY047_2	100	5	600	10	10^{17}	15
EJY047_3	100	10	600	10	10^{17}	15
EJY047_4	100	15	600	10	10^{17}	15
EJY047_5	100	20	600	10	10^{17}	15
EJY047_6	100	25	600	10	10^{17}	15
EJY047_7	100	30	600	10	10^{17}	15
EJY047_8	100	20	550	10	10^{17}	15
EJY047_9	100	20	650	10	10^{17}	15
EJY047_10	100	20	700	10	10^{17}	15
EJY047_11	100	20	600	10	10^{17}	20
EJY047_12	100	20	600	10	10^{17}	25

Table 1: Epitaxy growth conditions and oxide thickness for the 12 MOS samples EJY047_1 … EJY047_12 investigated in the experiment.