Design, fabrication, and characterization of integrated optical through-silicon waveguides for 3D photonic interconnections

Francesco Villasmunta*[a,c], Patrick Steglich[a,b], Claus Villringer[a], Sigurd Schrader[a], Harald Schenk[c,d], Andreas Mai[a,b], Martin Regehly[a]

[a]Technical University of Applied Sciences Wildau, Hochschulring 1, 15745 Wildau, Germany; [b]IHP – Leibnitz-Institut für innovative Mikroelektronik, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany; [c]Brandenburg University of Technology (BTU) Cottbus-Senftenberg, Platz der Deutschen Einheit 1, 03046 Cottbus, Germany; [d]Fraunhofer IPMS, Maria-Reiche-Strasse 2, 01109 Dresden, Germany

ABSTRACT

In the context of an ever-growing volume of data generated by established and emerging technologies, such as 5G, the Internet of Things, artificial intelligence, machine learning, blockchain, and virtual reality, faster communication speed is demanded by data centers and high-performance computing. Transceiver requirements surged from 100 to 400 Gb/s and beyond. In this scenario, photonics aims to enable Tb/s optical communication at energies below 1 pJ/bit. Targeting higher communication rates while maintaining a low power budget can significantly benefit from 3D photonic chip architectures. This paper presents the simulation-based design, fabrication, and characterization of a monolithically integrated optical through-silicon waveguide that facilitates the connection between different surfaces of a silicon chip. Deep reactive ion etching was employed in both the Bosch and Cryogenic variants to evaluate the effect of sidewall roughness on propagation losses. The mechanical stability of the waveguide was ensured by interrupting the annular trench with a bridging structure. The high-refractive-index contrast to air provides tight light confinement for a core size of up to 50 µm and multimode operation at 1550 nm. The morphology was characterized using scanning electron microscopy (SEM), and optical transmission characterization was performed using relative power loss measurements. A tunable laser source was butt-coupled to a waveguide to analyze light transmission efficiency. Preliminary measurements using single-mode fiber show that the transmitted values exceeded 99% for all structures.

Keywords: Multimode photonics, Cryogenic etching, ICP-DRIE, Optical interconnects, Silicon photonics, 3D chip stacking

1. INTRODUCTION

In recent years, the development and mass adoption of data-hungry technologies have progressed significantly. Today, it is easy to think about large language models (LLM) relying on Machine Learning (ML) and more widely on Artificial Intelligence (AI). They must process and analyze large volumes of data at a very quick rate to provide real-time or low-latency answers or decisions. Together with other established and emerging technologies, such as 5G, Internet of Things, blockchain, and virtual reality, they contribute to the demand for faster communication speed. In this scenario, transceiver requirements surged from 100 to 400 Gb/s and beyond[1]. The major impact of this demand is on data centers and high-performance computing units. Although the computing power of a single die is still able to keep pace and improve over the years, the interconnects are holding back, approaching the limit of their scalability, and effectively acting as I/O bottleneck[2]. Consequently, the performance of the entire system is limited by the speed at which data can be transmitted between chiplets. A further, not less important, aspect that is affected by electrical interconnections is the power consumption. In fact, the energy required to handle such information has reached environmentally significant levels[3]. Most of the energy is dissipated, not in logical operations, but to transport information[4]. It is estimated that approximately 20% of the power is overall lost in connection paths longer than 1 mm.

*francesco.villasmunta@th-wildau.de

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Photonics aims to enable Tb/s optical communication at energies below 1 pJ/bit[5]. In addition, optical clock distribution can benefit from this technology[6]. Targeting higher communication rates while maintaining a low power budget can benefit significantly from 3D photonic chip architectures[3]. In this context, an integrated optical waveguide, as a communication channel seamlessly integrated within a silicon chip, is required to facilitate connections between different surfaces. Such an element simplifies the coupling of internal and external light sources with photonic integrated circuits, enabling the adoption of stacked 3D photonic chip architectures for efficient interchip data exchange.

In this manuscript, we introduce vertical optical interconnects realized by the deep reactive-ion etching (DRIE) of a silicon substrate, a well-established process widely employed in the complementary metal-oxide-semiconductor (CMOS) industry. This manufacturing technique allows for direct integration of the waveguide component into the production of large-scale 200- or 300-mm wafers. The interconnects are composed of monolithically integrated waveguides in silicon, defined here as optical through-silicon waveguides (OTSWs). A trench is etched partially around the core of the waveguide, insulating it from the surrounding material to create the necessary refractive-index contrast. The mechanical stability of the waveguide is ensured by one or more monolithic silicon slabs acting as bridges between the core of the waveguide and the surrounding substrate. Here, we demonstrate the fabrication of the structures using both industrially established Bosch etching and cryogenic etching methods. A particular focus should be dedicated to the effect of the sidewall profile, which mainly distinguishes the two methods in terms of propagation losses. However, because of the different propagation axial lengths of the waveguides, it was not possible to decouple these two effects. In fact, optical characterization focuses on the comparison of the transmission performance with respect to the fiber-to-fiber coupling. The measurements also included a study of alignment tolerance. The variety of integration possibilities with other photonic components, such as grating couplers and planar silicon waveguides, and hetero-integration with optoelectronic elements such as vertical cavity surface-emitting lasers (VCSELs) and photodetectors, makes this passive element highly versatile and offers flexibility in the continuously expanding photonic ecosystem, including multimode photonics[7–9]. Moreover, in combination with through-silicon via (TSVs) technology, the integrated optical waveguide enables the possibility of stacking electro-optical chips on top of each other, allowing for the creation of highly efficient optical networks in a compact and tightly integrated package (Figure 1).

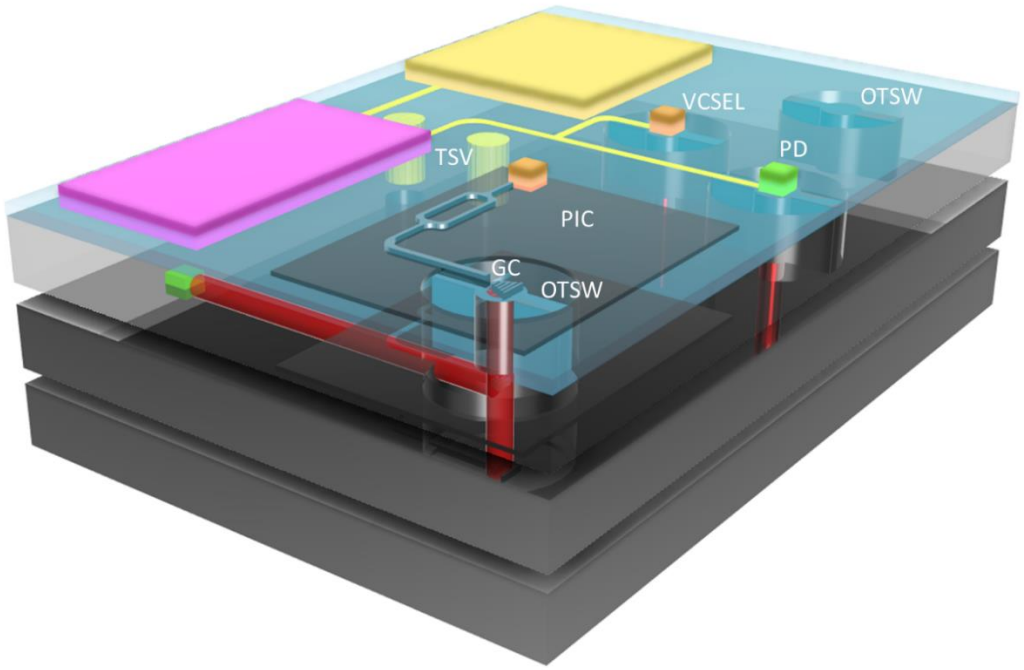

Figure 1. Graphical depiction of a three-dimensional stacked chip integration, showcasing the incorporation of diverse functions, including 3D electrical interconnects (TSV), photonic interconnects (OTSW), and various sources (VCSELs, grating couplers (GC)) and receivers (PD). A grating coupler can be designed to enable the redirection of light within a planar silicon waveguide to the vertical dimension without the need for tilting the Optical Through-Silicon Waveguide (OTSW).

2. SIMULATION AND DESIGN

Designing a monolithically integrated silicon waveguide in the vertical direction has advantages and disadvantages compared with the realization of a planar silicon waveguide. Despite being both fabricated using DRIE, the constraints imposed by this process are completely different. While planar silicon waveguides require a shallow etching process with a depth of only a few hundred nanometers, OTSWs must cross the bulk of the entire wafer, ranging from approximately 100 to 700 µm. Anisotropic plasma dry etching processes, such as Bosch[10] and Cryogenic[10–12], are often characterized by their strengths and weaknesses, but they share the same basic compromise between a high quality morphology and a fast etch rate[10]. Common morphological defects that are often observed in very deep-etched structures include mask undercut, bowing, notching, and scalloping[13]. Additionally, the sidewalls of these structures can be tapered, resulting in different cross-sectional sizes from top to bottom. These characteristics represent the main constraints imposed by DRIE and affect the minimum cross-sectional dimensions of the vertical waveguides, which are currently considered to be approximately 20 µm, given a tapering angle of approximately 1° for a 150 µm thick wafer. Fortunately, another typical limitation encountered by DRIE, known as aspect ratio-dependent etching (ARDE)[13], does not hinder the fabrication of OTSWs because it is not a relatively small waveguide that needs to be etched, but a through-silicon via (TSV) trench around it. Another constraint that is released in comparison with planar waveguides is the freedom of the waveguide cross-sectional shape design, which only requires mechanical stability. Therefore, the core shape can be tailored to satisfy several requirements such as polarization dependence, mode field size matching, and alignment tolerances. To address the physical stability of the structures a silicon slab, defined as "bridge", is left to partially interrupt the annular trench around the waveguide and bind it to the surrounding substrate (Figure 2). Naturally, if air is chosen as a cladding for high-refractive-index contrast, light propagation is supported by multiple modes, given the relatively large waveguide dimensions. Nonetheless, if required, cladding material can be deposited on the waveguide sidewalls by PECVD, or SiO_2 can be thermally grown. In practice, given the strong input contrast to air, the effective light input angle will exceed the critical angle to provide an estimated 1,3 Tbit/s single channel data rate in on–off keying modulation. In principle, single-mode propagation can be achieved if a material with a very weak refractive index contrast, such as polySi:P, is employed as the cladding.

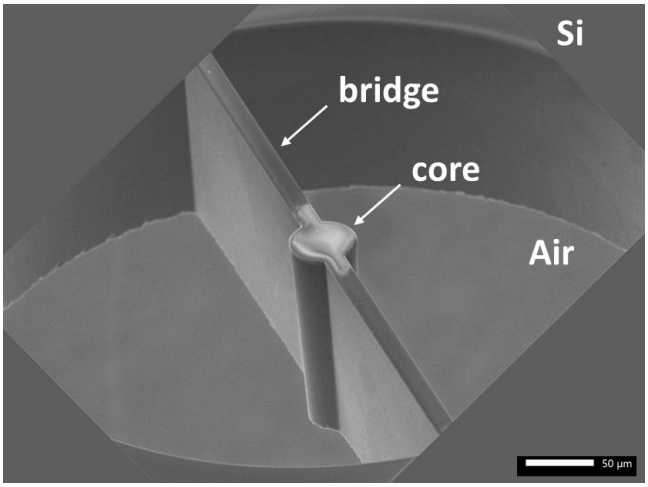

Figure 2. Scanning electron microscope image of a deep reactive ion-etched optical through-silicon waveguide. At the waveguide's top, a SiO_2 layer serves as a lithographic mask. The monolithic waveguide's core is linked to the substrate through two silicon slabs. The etched trench forms an air gap, contributing to the required refractive index contrast.

The necessity of a bridge results in a waveguide that is not completely surrounded by a material with a lower refractive index. To avoid excessive losses, an optimal bridge-to-core size ratio can be assessed using finite-difference frequency-domain (FDFD) electromagnetic wave simulations. As reported in a previous publication[14], for the structure depicted in Figure 3, the optimal bridge-to-core size ratio is comprised between 0.4 and 0.6. At this ratio, while the fundamental mode is confined within the waveguide core, higher-order modes start to leak into the bridges, exhibiting a behavior similar to that of the rib waveguides.

Based on these considerations, multiple parameters had to be established in the design of the waveguides, such as the core shape and diameter, bridge shape and width, shape and size of the open trench area, and waveguide array distributions in the test fields, for effective morphological and optical characterization. Four different structures were selected for mask lithography in this first iteration of the design process. Structure 1 (Figure 3a) has a circular core with diameter d_c = 50 µm and a single bridge of width w_b = 16 µm. Structure 2 (Figure 3b) has a circular core with the same diameter d_c = 50 µm and a double bridge of width w_b = 16 µm. Structure 3 (Figure 3c) is similar to structure two, but the size of the core is d_c = 28 µm and the bridge width is w_b = 14 µm. The trench size is w_t = 250 µm for all structures. Structure 4 (Figure 3d) is shaped like a rib waveguide, but with the internal angles following the crystallographic directions of the vertical planes {111} lying below the <112> directions on the surface of a Si{110} wafer[15]. The core and bridge dimensions were chosen according to the conditions demonstrated by *Huang et al.[16]* for single mode light propagation at 1550 nm, with a core size d_c = 50 µm and a bridge size w_b = 32 µm. The recurrent 50 µm core size was chosen to provide mode field size matching with a multimode optical fiber to ensure high coupling efficiency[17, 18]. In the case of a SiO_2 hard mask, its thickness can be tuned to provide impedance matching at λ=1550 nm and minimize back-reflections. Electromagnetic simulations of the fundamental mode confinement of the four structures are shown in Figure 3a-d.

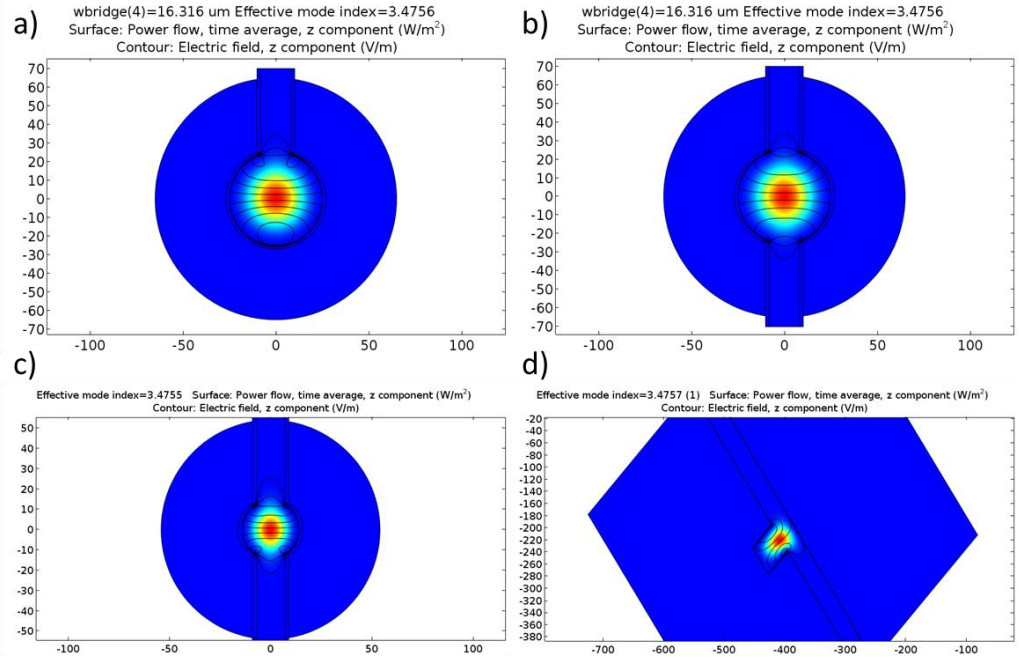

Figure 3. Finite Difference Time Domain (FDTD) simulations illustrate fundamental mode light confinement in distinct Optical Through-Silicon Waveguide (OTSW) designs: a) Circular core (d_c = 50 µm), single bridge (w_b = 16 µm); b) Circular core (d_c = 50 µm), double bridge (w_b = 16 µm); c) Core size (d_c) 28 µm, bridge width (w_b) 14 µm, trench size (w_t) 250 µm for all; d) Rib waveguide shape with internal angles following crystallographic directions on Si{110} wafer surface ({111} below <112>). Core (d_c) and bridge (w_b) dimensions tailored for single-mode light at 1550 nm (d_c = 50 µm, w_b = 32 µm).

3. MATERIALS AND METHODS

3.1 Bosch and Cryogenic DRIE

OTSWs can be integrated on SOI photonics platforms by performing localized backside etching, where the waveguide lands either on an optoelectronic component such as a VCSEL or a photodetector, or a passive component such as an integrated grating coupler that can steer the incoming radiation into a planar silicon nanowaveguide[19, 20]. However, for the initial purpose of characterizing only the waveguides, a pure silicon wafer patterned with a 4 µm SiO_2 mask was chosen. Considering studies on the effects of sidewall roughness on optical propagation losses[21–24], two different DRIE etching processes for waveguide fabrication have been adopted: multiplexed Bosch process and continuous cryogenic etching process. Bosch etching is a well-consolidated and robust etching process that represents the industry standard. However,

it is affected by sidewall roughness and periodic scalloping, which can induce diffraction patterns in the wavefront (Figure 4). Cryogenic etching is more condition-sensitive, but very promising for this application because it produces smooth sidewalls. Consequently, lower losses and better signal quality are expected, which in turn can help maintain a low total power budget, thus improving energy efficiency.

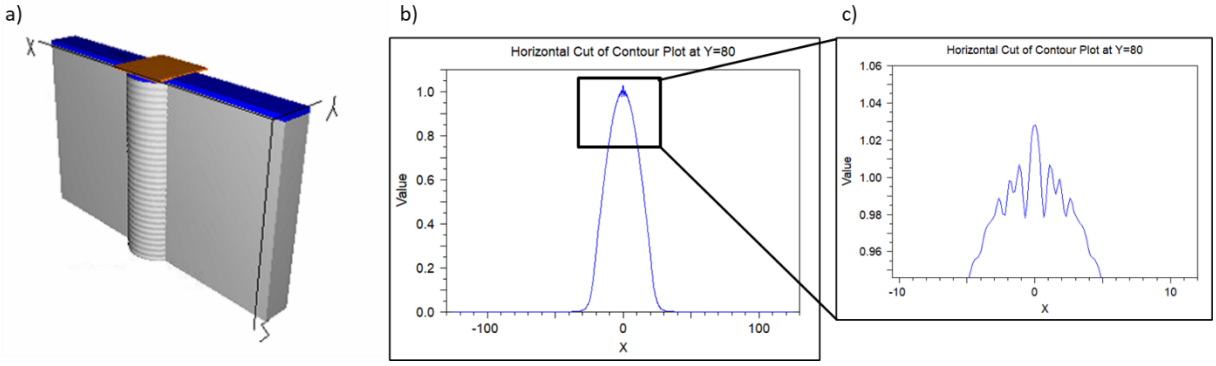

Figure 4. Beam propagation method simulation of an OTSW with the characteristics of Structure 1 (d_c = 50 µm, w_b = 16 µm). In a) is represented the 3D simulation geometry. The orange square represents the source of a gaussian beam with a diameter of 50 µm. The blue layer is a 4 µm SiO_2 mask. The sidewalls of the waveguide are scalloped with a period of 600 nm, such as by the Bosch etching fabrication process; in b) the electric field profile after a propagation distance of 150 µm; and c) a close-up of the wavefront with a diffraction pattern induced by the sidewall's scallops.

Mask lithography and Bosch etching were performed at the Leibniz Institute for High Performance Microelectronics (IHP), Germany. The 200 mm wafers were first etched to a depth of 250 µm and then thinned to a final thickness of 150 µm, thereby revealing the OTSWs. Consequently, scuff marks from the grinding process remained on the exposed facets of the waveguides (Figure 6). The etching was done for 295 loops in a SPTS Rapier etching chamber. The mask was 4 µm PECVD-based SiO_2.

Cryogenic etching was performed at the University of Applied Science in Wildau, Germany. A commercially available inductively coupled plasma (ICP) etching system from Sentech Instruments GmbH was used for the experiments. The system was connected to a 120 L dewar, which was filled with the liquid nitrogen necessary to perform the test runs. In this case, the masked wafers were first thinned to 100 µm and 150 µm, and then diced into approximately 3 × 2 cm^2 large single dies. During each run, a die was loaded on a 100 mm carrier wafer, and a thin layer of Fomblin® oil was spread at the interface to ensure thermal contact between the sample and carrier. This oil is resistant to chemical etching and stable over a wide range of process temperatures. The carrier wafer and sample were then placed on a stainless-steel wafer holder with a bottom cavity that provided thermal exchange with liquid nitrogen by means of backside He flow. Prior to each set of runs, the reactor was cleaned with a mixture of O_2, SF_6, and Ar and then conditioned with a sacrificial wafer under conditions similar to the actual etching process. These steps and test runs were monitored using a plasma optical emission spectroscopy (OES) system adapted to the process chambers, which was necessary to safeguard the reproducibility of the method.

The morphological characterization of the structures was performed using optical and scanning electron microscopy (SEM). When possible, the samples were broken to observe the cross section of the chip. Atomic force microscopy (AFM) measurements of sidewall roughness are desired but are not yet available.

4. RESULTS AND DISCUSSION

4.1 Bosch etching

In the case of the OTSWs fabricated by Bosch etching, Figure 6e shows that in the adopted process flow, a single bridge cannot provide the necessary stability to survive the thinning process. However, the double-bridged stabilization system was sufficiently robust to withstand this process. For this reason, only Structures 2, 3, and 4 (Figure 6f-h) from this process can be characterized in a wafer that is 150 µm thick.

Structure 2 (Figure 6f) showed a very good morphology, characterized by a regular scalloping of approximately 600 nm from top to bottom. No other prominent defects were observed. The waveguide's core sidewalls however are tapered at an angle $\vartheta = 2{,}35°$ and therefore the bottom facet of the waveguide has an ellipsoidal section with a short axis of $d_o = 37{,}7$ µm. The bridge width is reduced to $w_o = 7$ µm. As anticipated in the previous section, scuffs from the grinding process were observed at the output facet surface of the waveguide.

Structure 3 (Figure 6g), similar to Structure 2, showed a tapered core profile at an angle $\vartheta = 2°$. The short ellipsoidal axis of the output facet is $d_o = 17{,}5$ µm in this case and the bridge width has a value of $w_o = 6$ µm and therefore a tapering angle of $\vartheta = 1{,}33°$. This result indicates that the slab and circular section of the waveguide have different tapering angles.

Structure 4 (Figure 6h), unlike patterns 1,2 and 3, all characterized by a circularly shaped core, showed no tapering angle, and the output facet sizes of the core and bridge are constant from side to side.

4.2 Cryogenic etching

On the other hand, cryogenic etching is a highly parameter-sensitive process that relies on the delicate balance between etching and passivation mechanisms occurring at the same time[11]. When one condition dominates the other, the process is unbalanced toward either an over- or under-passivation regime. Both have detrimental effects on the morphological quality of fabricated structures. In these experiments, such effects are often observed during the process development and optimization. In the first case, the formation of silicon micrograss at the bottom of the trenches was observed and was associated with a decrease in the etch rate, as is well known from previous studies[12]. In the second case, isotropic etching and catastrophic effects were observed in the underpassivated samples. Unfortunately, these effects develop with longer processing times; therefore, finding a good starting set of parameters by factorial design of experiment[25] is not enough and requires further optimization, for example, by ramping certain parameters such as the substrate temperature or the amount of O_2 in the gas mixture, which have the highest impact on the passivation mechanism[12]. A robust set of initial parameters was found for processes up to 18 min in duration with an etch rate of approximately 1,5 µm/min, therefore it reached a depth of approximately 27 µm and showed excellent morphological characteristics with steep and smooth vertical sidewalls (Figure 5). As expected, an overpassivating regime was observed when running for longer durations with this particular set of parameters. This regime was characterized by the formation of silicon micrograss and a cessation of the etching process. The successful fabrication of a 100 µm thick sample was achieved using a different set of parameters. However, the resulting waveguides exhibited some defects, including mask undercut and an inhomogeneous sidewall profile. Nonetheless, these structures are sufficiently different from those etched by the Bosch process, particularly in the absence of periodic sidewall scalloping. The fabrication of 150 µm thick samples has not yet been successfully completed as of the current time.

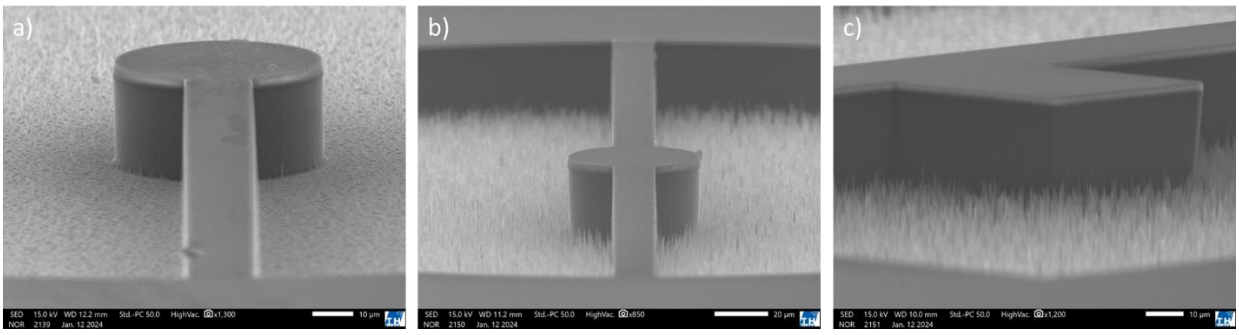

Figure 5. Scanning electron microscope images of the cryogenically etched a) Structure 1; b) Structure 2; and c) Structure 4. For etch depths up to approximately 30 µm, the current process provides excellent morphological quality of the sidewalls with a smooth and steep profile and consistent reproducibility. At the bottom of the trenches the initial stages of black silicon/micrograss formation are visible.

Given the inverse process flow between thinning and etching with respect to the Bosch-etched structures, Structure 1 was successfully fabricated in this case. The sidewalls of the waveguides were not perfectly smooth but did not present any periodic pattern. To compare the nanometric roughness, atomic force microscope measurements are required and are

planned to be performed. All waveguides fabricated with this process showed no signs of scalloping, but the sidewalls were not as smooth as the process could convey.

Structure 1 (Figure 6a) was etched with a tapering angle of $\vartheta = 3{,}4°$. As a result, the diameter of the bottom facet is $d_o = 38$ µm, which is close to that of Structure 2 (Figure 6f) etched by the Bosch process. However, the thicknesses of the two samples were different (100 µm for cryogenic and 150 µm for Bosch); therefore, the tapering angle was steeper in the case of the cryogenically etched structures. The resulting bottom bridge width is $w_o = 13{,}6$ µm and the sidewalls are almost vertical with a tapering angle $\vartheta = 0{,}7°$.

Structure 2 (Figure 6b) was characterized by the same irregular sidewalls. In this case the tapering angle was $\vartheta = 5{,}7°$ with a bottom diameter of the waveguide $d_o = 30$ µm. The bridge width at the bottom was $w_o = 8{,}9$ µm, corresponding to a tapering angle $\vartheta = 2°$.

Structure 3 (Figure 6c), because of the relatively high tapering angle, did not preserve the designed shape from top to bottom, and a relatively strong lateral etching caused degradation of the bottom tip of the waveguide. Therefore, they cannot be optically characterized.

Structure 4 (Figure 6d), unlike that etched by Bosch, presented a tapered profile. The lateral size of the bottom facet is $d_o = 37$ µm corresponding to a tapering angle $\vartheta = 3{,}7°$. The bottom bridge width is $w_o = 21{,}2$ µm resulting from a tapering angle of $\vartheta = 3{,}1°$.

In general, a significant morphological variation in the tapering angles is observed for different structures on the same sample and between the bridge and core.

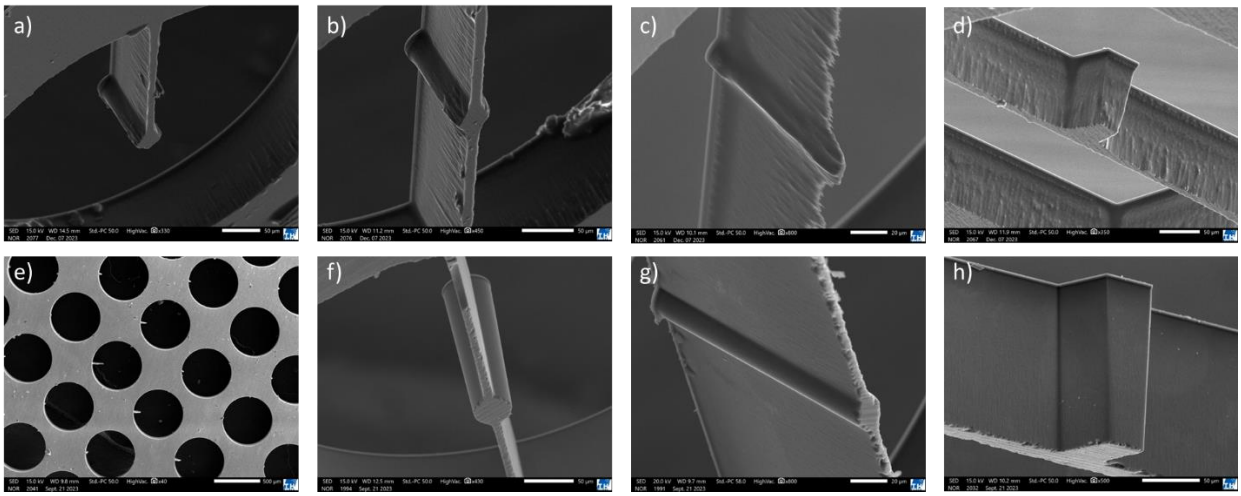

Figure 6. a-d) Scanning electron microscope images depict 100 µm deep Optical Through-Silicon Waveguides (OTSWs) etched via cryogenic DRIE. e-h) Corresponding images showcase Bosch-etched waveguides. The sidewall morphology in a, b, and d is qualitatively acceptable but not perfect. Structure c experienced strong lateral etching and was unsuitable for optical characterization. Structure e (with single bridge) did not withstand the grinding process. In contrast, structures f, g, and h were successfully fabricated with a depth of 150 µm, exhibiting a regular sidewall profile.

4.3 Optical characterization

Accurate measurement of OTSW properties, such as transmission losses, polarization dependence, and alignment tolerances, in experimental optical structures is fundamental for determining their performance and the consequent impact of this photonic element on the power budget between a source and a detector. To evaluate these quantities, one end of a bare optical fiber connected to a laser source must be precisely aligned on one side with the core of the through-silicon waveguide. On the other end, another optical fiber must collect the outcoming light and carry it to a photodetector, where the transmitted intensity can be measured as voltage. This voltage can then be compared with the reference voltage measured by directly injecting the beam from the source fiber into the receiving fiber. By comparing the results obtained by measuring differently shaped and fabricated through-silicon waveguides, better-performing waveguides can be identified, and the design of the structures and fabrication methods can be modified to improve component design and

functionality. Such measurements require a highly accurate optical characterization system, as described in the following paragraph. A schematic of the optical characterization setup is shown in Figure 7.

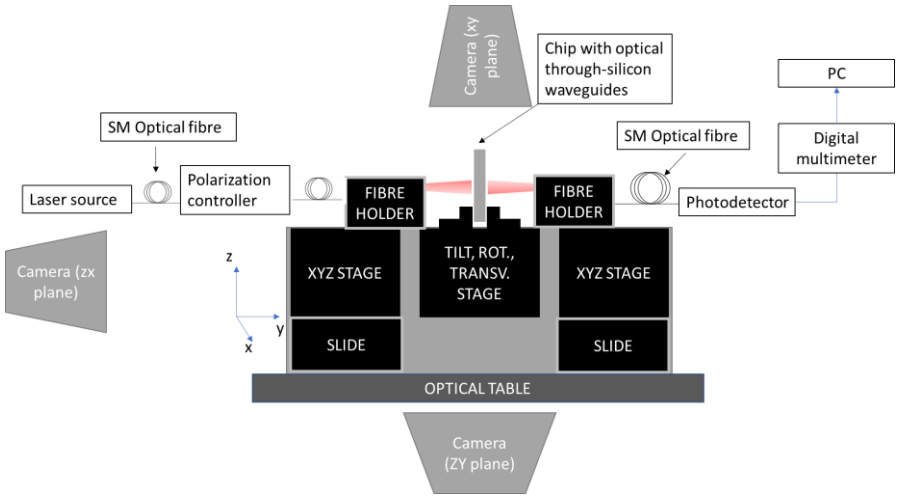

Figure 7. Schematic illustration of the optical characterization setup. The alignment of the source and receiver fibers is facilitated by an XYZ translational stage with a displacement resolution of 20 nm. In these initial experiments, two single-mode optical fibers were employed. The laser source operates at 1550 nm with a power output of 10 mW. The coupled light produces a voltage output on the receiving end. Three machine vision cameras support the manual alignment procedure.

In the current setup the FC/APC connector of a single mode (SMF-28) optical fibre is connected to one of the laser sources available in our lab, such as the Yenista T-100S benchtop external cavity laser (ECL) or the APEX AP3350A tunable laser source (TLS) and tuned at $\lambda = 1550\ nm$ and 10 mW of power. The other end of the fiber was stripped from the jacket and left bare. Exposing the waveguide cladding simplifies the tedious alignment procedure. Another single-mode (SMF-28) optical fiber, which acts as a receiver, is connected at one end to the photodetector DET08CFC/M from Thorlabs Inc., which is linked to a KeySight 34461A digital multimeter and measurement PC. To treat the noise affecting some measurements, Python code was employed to average a large number of measurements and calculate the standard deviation. The other end of the fiber was stripped and bare. The fiber-to-chip alignment procedures were assisted by three machine-vision cameras equipped with 10x magnification objectives (Figure 8b). The bare ends of the two fibers were supported by fiber holders mounted on the flexure stages of the MDE881 professional waveguide alignment workstation from Elliot Scientific Limited (Figure 8a). The flexure stages provide travel in the x-, y-, and z-directions with a full displacement range of 2 mm in each direction and an adjustment resolution of 20 nm. The central stage includes tilt, rotation, and transverse motion stages. Travel in the transverse direction can be visually controlled using a small digital readout screen. The sample holder was mounted on the top.

Transmission measurements were performed by acquiring the average value of 100 measurements to minimize the influence of the detector noise on the measured value. Despite the current lack of knowledge regarding the exact polarization direction of the incident light with respect to the bridge axis, a linearly polarized state of light is rotated before every measurement until the transmission readout value is maximized. These measurements were repeated five times after realignment of the fibers to the same structure. This procedure was repeated for five random structures from the same field. The alignment tolerance measurements were performed in a similar manner. The spatial coordinate variation was always perpendicular to the bridge axis. The measurement procedure relies on highly accurate nanodisplacement of the receiver flexure stage. After maximizing the output power, the stage was displaced in both directions in steps of 20 or 40 nm, and the average voltage was read out.

Unfortunately, at this time conventional methods for the characterization of propagation losses, such as cut-back[26] or Fabry-Perot[27] could not yet be applied.

These measurements represent a preliminary series of tests that will be repeated and refined using different combinations of single-mode and multimode optical fibers.

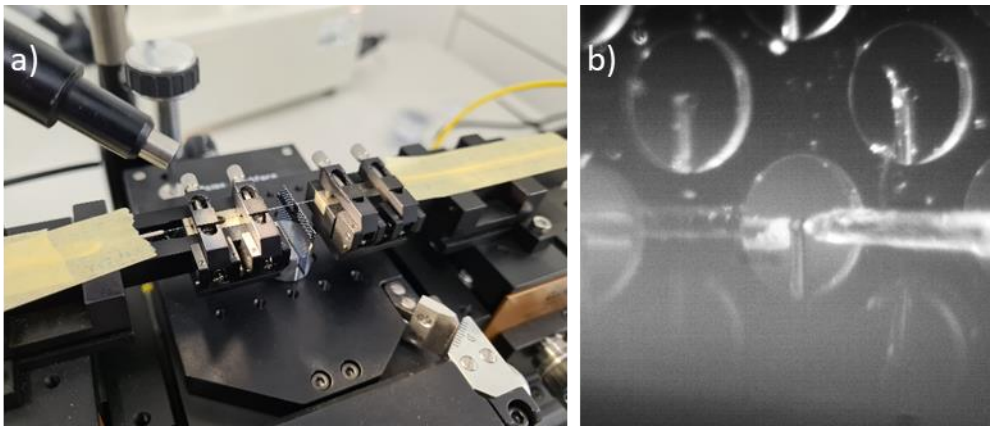

Figure 8. Picture a) provides a close-up view of the fiber-to-waveguide alignment setup. In b), the alignment of sender and receiver fibers with the integrated waveguides is achieved through a macro camera system for enhanced precision.

To optically characterize the waveguides and their performance, we compare in Figure 9 the results of the maximized transmission measurements for each structure obtained using the method reported in the previous section. We can observe that over several tests, fiber-to-fiber coupling comes with the higher uncertainty, spanning from a minimum readout value of V_o = 11,52 V to a maximum of 11,64 V. This large standard deviation is also associated with the smallest measured 3 dB width alignment tolerance (FWHM), which is as small as approximately 300 nm, as shown in Figure 10. A direct performance comparison between the structures etched by the cryogenic and Bosch processes in this case is not possible because the effects of the waveguide's length and sidewall profile cannot be decoupled. Nonetheless, it is possible to compare the fiber-waveguide-fiber (FWF) coupling for samples from the same process and them to the fiber-to-fiber coupling (F2F). Structures 1 and 2 obtained by cryogenic etching had similar maximum coupling efficiencies and did not present any significant losses in comparison to the F2F coupling. However, S1 shows a slightly larger alignment tolerance than S2, with measured values of 563 nm and 429 nm, respectively. The alignment tolerance with respect to the F2F coupling was almost 100% higher in the first case and 150% in the second case. Structure 2, etched by Bosch in this test, reported the lowest coupling efficiency, although the measured value was 98,48% of that measured for F2F and within its standard deviation. The alignment tolerance of these structures was approximately 525 nm. Structure 3, etched by Bosch, showed a slightly higher coupling efficiency than structure 2, but an alignment tolerance as low as 253 nm, which is also the lowest measured and approximately 84% of the F2F one. Among all the measurements, the design of structure 4 from both Bosch and cryogenic etching showed the highest measured voltage in the photodetector. The alignment tolerances with respect to the spatial axis transversal to the bridge direction are 404 and 550 nm, respectively, and are therefore sensibly higher than that of the simple F2F coupling. In general, these results match and confirm the confinement properties predicted by the simulation analysis. In addition, with the current setup and preliminary results, the size and sidewall quality do not seem to provide a striking difference in the measured performance, with the light always being confined and losses lower than 1,2%. This can be explained by the fact that in these tests, two single-mode fibers were coupled from both ends of the waveguide. The situation can differ significantly when a multimode fiber or another larger source is coupled into the waveguide, and mode field size matching and adiabatic tapering for mode field size conversion start playing a significant role.

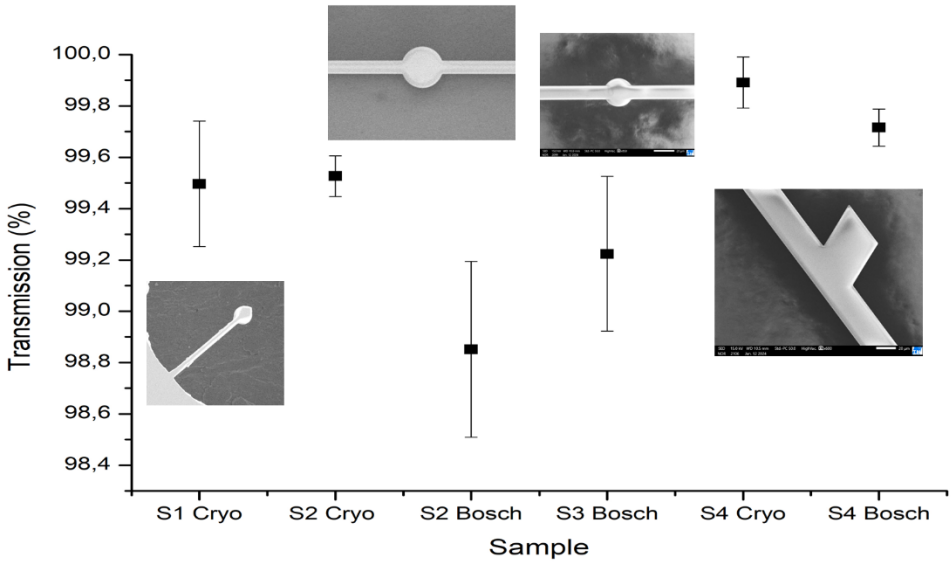

Figure 9. This graph illustrates the average measured values for fiber-to-waveguide optical transmission. Structures 1 and 2, etched by cryogenic DRIE, exhibit a transmission higher than 99.4%. Structures 2 and 3, fabricated by Bosch DRIE, demonstrate a transmission ranging between 98.8% and 99.2%. Remarkably, Structures 4, in both cryogenic and Bosch cases, showcase the highest measured transmission values.

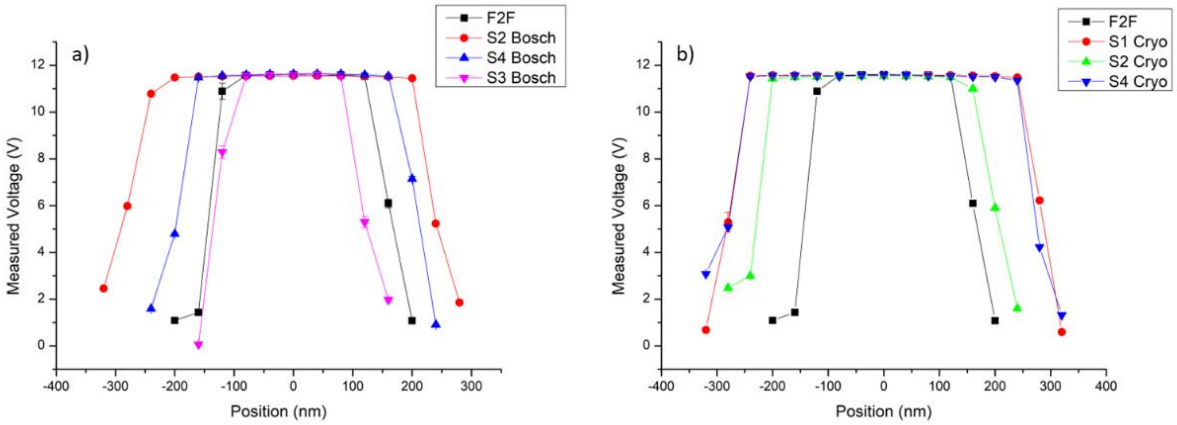

Figure 10. a) Graph depicting alignment tolerances for waveguides fabricated via the Bosch process, compared to fiber-to-fiber alignment. b) Similar representation for structures cryogenically etched. Notably, Structure 3, etched by Bosch, exhibits the lowest alignment tolerance, while Structures 2 (Bosch) and Structures 1 and 4 (cryogenic etching) demonstrate larger tolerances which are almost twice as much as the fiber-to-fiber coupling.

5. CONCLUSION

In this paper we presented the successful design and fabrication of optical through-silicon waveguides for chip-to-chip communication. The fabrication was successfully completed with both cryogenic and Bosch etching methods with a final wafer thickness of 150 µm and 100 µm, respectively. Waveguides etched using the Bosch method exhibit characteristic sidewall scalloping periodicity, whereas cryogenically etched waveguides, while not perfectly regular, display smooth sidewalls. A direct comparison of the effects of sidewall roughness and periodicity on light propagation was hindered by the differing lengths and tapering angles of structures obtained via the two methods. Nevertheless, simulations indicate that all fabricated structures effectively confine and transmit light when coupled to single-mode waveguides from both sides, utilizing 1550nm laser light at a power of 10 mW. The measured transmission exceeds 99% in preliminary experiments, despite mask back-reflections and scuffing on the waveguide bottoms resulting from the thinning process.

Additionally, it was observed that the 3 dB alignment tolerance between two fibers increases twofold when an optical through-silicon waveguide is interposed. Future steps involve conducting measurements with various fiber types to simulate diverse sources and detectors. Moreover, the accurate determination of the sidewalls roughness and periodicity is necessary to determine which of the process suits best for the fabrication of these components in different integrations scenarios.

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REFERENCES

[1] P. Dong et al., "Silicon Photonics for 800G and Beyond [invited]," in Optical Fiber Communication Conference (OFC) 2022, San Diego, California, M4H.1.
[2] C. Sun et al., "Single-chip microprocessor that communicates directly using light," Nature, vol. 528, no. 7583, pp. 534–538, 2015, doi: 10.1038/nature16454.
[3] D. A. B. Miller, "Attojoule Optoelectronics for Low-Energy Information Processing and Communications," J. Lightwave Technol., vol. 35, no. 3, pp. 346–396, 2017, doi: 10.1109/JLT.2017.2647779.
[4] C. A. Thraskias et al., "Survey of Photonic and Plasmonic Interconnect Technologies for Intra-Datacenter and High-Performance Computing Communications," IEEE Communications Surveys & Tutorials, vol. 20, no. 4, pp. 2758–2783, 2018, doi: 10.1109/COMST.2018.2839672.
[5] S. Bernabé et al., "Silicon photonics for terabit/s communication in data centers and exascale computers," Solid-State Electronics, vol. 179, p. 107928, 2021, doi: 10.1016/j.sse.2020.107928.
[6] D. Miller, "Rationale and challenges for optical interconnects to electronic chips," Proceedings of the IEEE, vol. 88, no. 6, pp. 728–749, 2000, doi: 10.1109/5.867687.
[7] Q. Zhang et al., "Multimode Optical Interconnects on Silicon Interposer Enable Confidential Hardware-to-Hardware Communication," Sensors (Basel, Switzerland), vol. 23, no. 13, 2023, doi: 10.3390/s23136076.
[8] D. Dai, w. zhao, J. Guo, and D. Liu, "Multimode silicon photonic devices," in Integrated Optics: Devices, Materials, and Technologies XXV, Online Only, United States, Mar. 2021 - Mar. 2021, p. 20. [Online]. Available: https://www.spiedigitallibrary.org/conference-proceedings-of-spie/11689/2577026/Multimode-silicon-photonic-devices/10.1117/12.2577026.full
[9] C. Li, D. Liu, and D. Dai, "Multimode silicon photonics," Nanophotonics, vol. 8, no. 2, pp. 227–247, 2019, doi: 10.1515/nanoph-2018-0161.
[10] M. Huff, "Recent Advances in Reactive Ion Etching and Applications of High-Aspect-Ratio Microfabrication," Micromachines, vol. 12, no. 8, 2021, doi: 10.3390/mi12080991.
[11] R. Dussart, T. Tillocher, P. Lefaucheux, and M. Boufnichel, "Plasma cryogenic etching of silicon: from the early days to today's advanced technologies," J. Phys. D: Appl. Phys., vol. 47, no. 12, p. 123001, 2014, doi: 10.1088/0022-3727/47/12/123001.
[12] M. J. de Boer et al., "Guidelines for etching silicon MEMS structures using fluorine high-density plasmas at cryogenic temperatures," J. Microelectromech. Syst., vol. 11, no. 4, pp. 385–401, 2002, doi: 10.1109/JMEMS.2002.800928.
[13] F. Laermer, S. Franssila, L. Sainiemi, and K. Kolari, "Deep reactive ion etching," in Handbook of Silicon Based MEMS Materials and Technologies: Elsevier, 2020, pp. 417–446.
[14] F. Villasmunta, P. Steglich, S. Schrader, H. Schenk, and A. Mai, "Numerical Simulation of Optical Through-Silicon Waveguide for 3D Photonic Interconnections," in 2021 International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD), Turin, Italy, 2021, pp. 115–116.
[15] P. Pal and S. S. Singh, "A New Model for the Etching Characteristics of Corners Formed by Si{111} Planes on Si{110} Wafer Surface," ENG, vol. 05, no. 11, pp. 1–8, 2013, doi: 10.4236/eng.2013.511A001.

[16] H. Huang, K. Liu, B. Qi, and V. J. Sorger, "Re-Analysis of Single-Mode Conditions for Silicon Rib Waveguides at 1550 nm Wavelength," J. Lightwave Technol., vol. 34, no. 16, pp. 3811–3817, 2016, doi: 10.1109/JLT.2016.2579163.
[17] R. Yu, C. Wang, F. Benabid, K. S. Chiang, and L. Xiao, "Robust Mode Matching between Structurally Dissimilar Optical Fiber Waveguides," ACS Photonics, vol. 8, no. 3, pp. 857–863, 2021, doi: 10.1021/acsphotonics.0c01859.
[18] K. Vanmol et al., "Mode-field matching design, 3D fabrication and characterization of down-tapers on single-mode optical fiber tips for coupling to photonic integrated circuits," in 3D Printed Optics and Additive Photonic Manufacturing II, Online Only, France, Apr. 2020 - Apr. 2020, p. 9. [Online]. Available: https://www.spiedigitallibrary.org/conference-proceedings-of-spie/11349/2555770/Mode-field-matching-design-3D-fabrication-and-characterization-of-down/10.1117/12.2555770.full
[19] J. Zhang, C. Zhang, G. Liang, and Y. Yang, "Simulation research of high-efficiency unidirectional vertical coupling grating couplers for optical through-silicon vias in 3D optoelectronic integrated circuits," Optics Communications, vol. 479, p. 126408, 2021, doi: 10.1016/j.optcom.2020.126408.
[20] N. Mangal, J. Missinne, J. van Campenhout, B. Snyder, and G. van Steenberge, "Ball Lens Embedded Through-Package Via To Enable Backside Coupling Between Silicon Photonics Interposer and Board-Level Interconnects," J. Lightwave Technol., vol. 38, no. 8, pp. 2360–2369, 2020, doi: 10.1109/JLT.2020.2966446.
[21] C. Bellegarde et al., "Improvement of sidewall roughness of sub-micron silicon-on-insulator waveguides for low-loss on-chip links," in 2017, p. 1010816. Accessed: Jul. 27 2020. [Online]. Available: http://proceedings.spiedigitallibrary.org/proceeding.aspx?doi=10.1117/12.2250344
[22] Kuan Pei Yap et al., "Correlation of Scattering Loss, Sidewall Roughness and Waveguide Width in Silicon-on-Insulator (SOI) Ridge Waveguides," Journal of Lightwave Technology, vol. 27, no. 18, pp. 3999–4008, 2009, doi: 10.1109/JLT.2009.2021562.
[23] T. Barwicz and H. A. Haus, "Three-dimensional analysis of scattering losses due to sidewall roughness in microphotonic waveguides," Journal of Lightwave Technology, vol. 23, no. 9, pp. 2719–2732, 2005, doi: 10.1109/JLT.2005.850816.
[24] F. Grillot, L. Vivien, S. Laval, D. Pascal, and E. Cassan, "Size Influence on the Propagation Loss Induced by Sidewall Roughness in Ultrasmall SOI Waveguides," IEEE Photonics Technology Letters, vol. 16, no. 7, pp. 1661–1663, 2004, doi: 10.1109/LPT.2004.828497.
[25] D. C. Montgomery, Design and analysis of experiments. Hoboken NJ: John Wiley & Sons Inc, 2017.
[26] C. Qiu et al., "Fabrication, Characterization and Loss Analysis of Silicon Nanowaveguides," J. Lightwave Technol., vol. 32, no. 13, pp. 2303–2307, 2014, doi: 10.1109/JLT.2014.2309122.
[27] L. Pavesi, Ed., Optical Interconnects: The Silicon Approach. Berlin, Heidelberg: Springer-Verlag Berlin Heidelberg, 2006.