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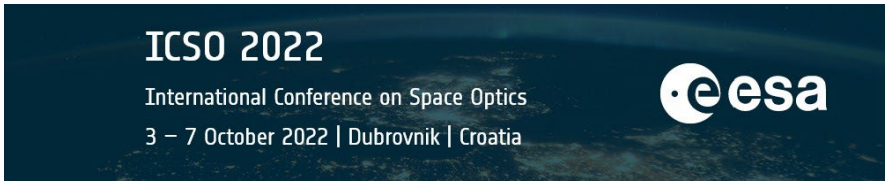

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High-speed optical transceiver integrated chipset and module for on-board VCSEL-based satellite optical interconnects

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ABSTRACT

We present the fabrication and testing of a prototype high-speed, quad-channel mid-board optics transceiver chipset and module applicable to VCSEL-based intra-satellite optical interconnects. The optical transceiver (OTRx) chipset comprises a VCSEL driver and a TIA integrated circuit (IC) both manufactured in IHP 130 nm SiGe BiCMOS process. The 4-channel OTRx module operates at 850 nm wavelength. It features low power consumption, a small form factor and it is pluggable on the host board through a micro edge card (MEC) connector. We present first functional test results in loop-back configuration at data rates up to 15 Gb/s per channel. The work is performed within the framework of H2020-SPACE-SIPHODIAS project.

Keywords: optical intra-satellite links, optical interconnects, VCSEL transceivers, Very High Throughput Satellites

1. INTRODUCTION

New generation advanced On-Board Processors (OBPs) rely on optical interconnects (OI) to transmit data quickly and efficiently within the telecom satellite. The migration toward OI is primarily motivated by the significant reduction of the mass and volume offered by fiber optics compared to electrical harnesses. The latter has reached space standardization through the ESCC3409/001 standard [1], which specifies SpaceFibre wireline links operating at 10 Gb/s data rates through 2.5 mm-diameter microwave cables weighing 17 grams / meter and exhibiting 2.2 dB / m loss. On the other hand, OI have already reached TRL 9 and thanks to the use of lightweight ribbon fiber optic cables and ruggedized dense multi-ferule connectors [2], they offer >90% savings in mass and volume consumption with respect to coaxial cables, whereas being capable to support higher data rates. OI have recently made their debut in commercial missions through the launch of Eutelsat KONNECT VHTS, which hosts Thales Alenia Space DTP5G OBP [3] – a processor with digital optical links operating at 10 Gb/s data lanes for board-to-board interconnections. To further promote the deployment of intra-satellite OI, ESA released the ECSS-E-ST-50-11C standard [4] which specifies SpaceFibre optical links operating at data signaling rates in the range of 6.25 to 10 Gb/s, with a system requirements roadmap extending beyond 25 Gb/s.

The critical component in on-board OI is the OTRx, which adopts the mid-board optics approach to accommodate a ruggedized system design, a small form factor and enhanced signal integrity. The majority of hi-rel OTRx, which are built to such system form and function make use of COTS electronic circuitry, which is evaluated under radiation constraints and they are mounted on the host board through BGA soldering or LGA interposers. To enhance reliability and accommodate a straightforward system assembly and integration, radiation-hardened (RH) electronic ICs and mounting methods which avoid solder or interposer-attach are often preferable.

In this paper we present the fabrication and testing of a prototype high-speed mid-board optics transceiver chipset and module applicable to VCSEL-based intra-satellite optical interconnects. The electronic integrated circuitry comprises of quad-channel VCSEL driver and transimpedance amplifier (TIA), both manufactured in IHP's 130 nm SiGe BiCMOS rad-hard process flavor (SG13RH). We also demonstrate the flip-chip assembly and packaging of the electronic chipset with COTS multimode (MM) VCSEL/PD opto-parts in a 4-channel mid-board OTRx module prototype. The OTRx module weighs 6.4 grams and occupies ~670 mm^2 of PCB area. We report eye diagram performance at data rates up to

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15 Gb/s with Non-Return-to-Zero (NRZ) On-Off-Keying modulation (OOK). The work is performed in the frames of H2020-SPACE-SIPHODIAS [5] project, which is funded by the European Union's Horizon 2020 research and innovation programme under Grant Agreement No 870522.

2. TRANSCEIVER CHIPSET

In this section we report the fabrication and characterization of the first-generation transceiver chipset, consisting of the quad channel VCSEL driver and TIA circuits. Both circuits accommodate flip-chip assembly within the OTRx module [6]. Figure **1** shows the microphotograph of the VCSEL Driver IC fabricated in IHP SG13RH technology along with a block diagram detailing the various features of the circuit. The four high-speed channels are visible on the left of the die, where the differential inputs (top) and single-ended outputs (bottom) are visible. The digital programming interface and biasing circuits are located on the right of the chip, covered by the metal fillers. Powered separately from the driver core, the rad-hard 8x8-bit register SPI slave core implements programming the three-stage driver. The driver can provide a programmable output current up to 11 mA. A coarse/fine control scheme over the output bias and modulation current is implemented to accommodate the required mode of operation for the VCSEL. The chip is powered by a single supply of 3.3 V and it features a 50-Ohm termination input.

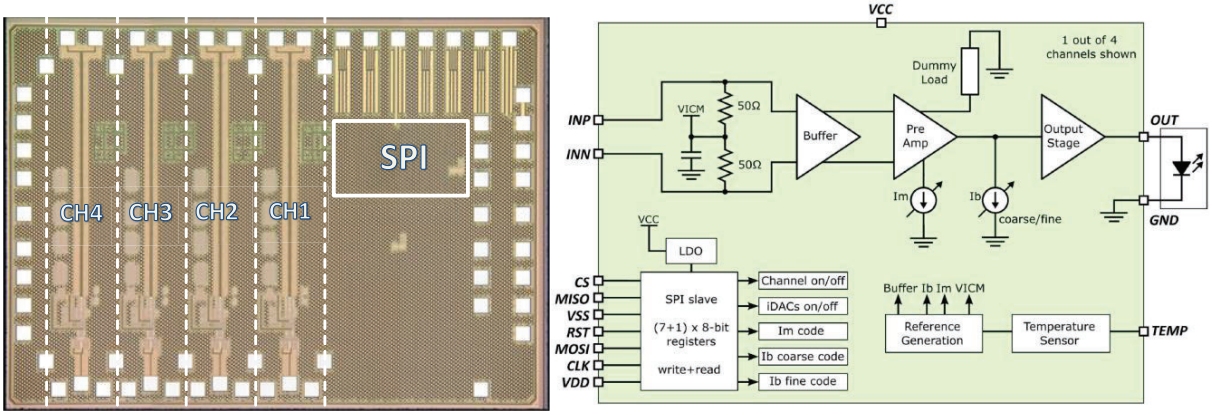

Figure 1. Driver IC microphotograph (left) and corresponding circuit block diagram for a single channel (right).

Figure 2 shows the microphotograph of the TIA photodiode receiver chip fabricated in the same process and uses a similar inventory of circuit blocks: Digital-to-Analog Converters (DAC), low-drop out regulators (LDO), bandgap references and SPI core for establishing biasing, programmability, and temperature sensing. The chip features 50-Ohm output and can be powered by supplies ranging from 2.5-3.3 V. Each TIA channel receives four controlled currents generated by a four-channel DAC, allowing noise tuning, transimpedance, and output swing adjustments. Each DAC having a separated bias reference network for enhanced reliability.

Each circuit occupies 2.6 mm^2 of silicon area. Besides components hardened by technology, radiation-hardened-by-design (RHBD) techniques were used, including enclosed layout transistors (ELTs) and custom designed RH flip-flops.

A series of electrical tests was performed on the chips to ensure functional operation prior to assembly of the OTRx module. The tests were performed after mounting the chips on custom designed PCBs built for this purpose. Biasing and control were interfaced through wire bonding from the PCBs, while high-speed signal interfacing was carried-out using a probing setup. Direct electrical characterization was possible with the use of PRBS input and oscilloscope as seen in the testbench shown in Figure 3.

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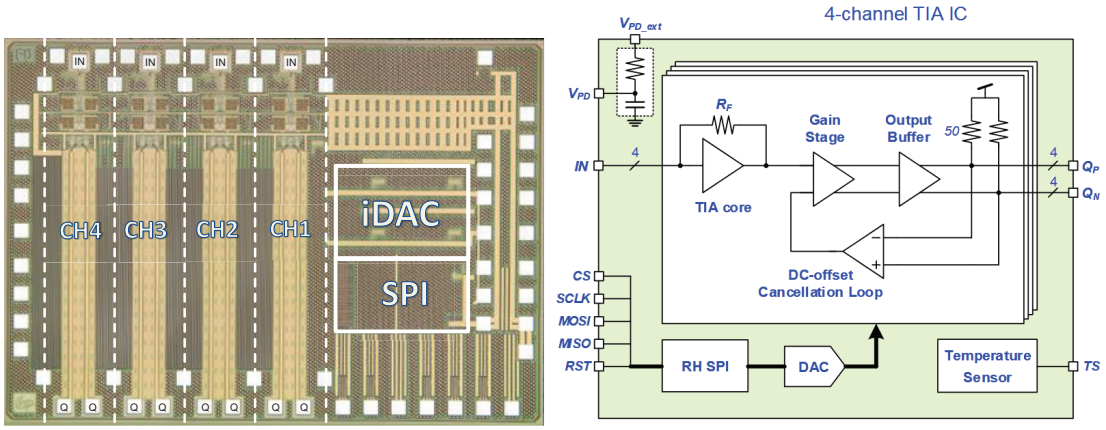

Figure 2. TIA photodiode receiver microphotograph (left) and block diagram (right).

Specifically, for the VCSEL driver, a dummy-load was implemented to emulate the biasing condition expected by the VCSEL component, which permitted to assess the output current capability. An example of the driver's fine output current setting is shown in Figure 4.

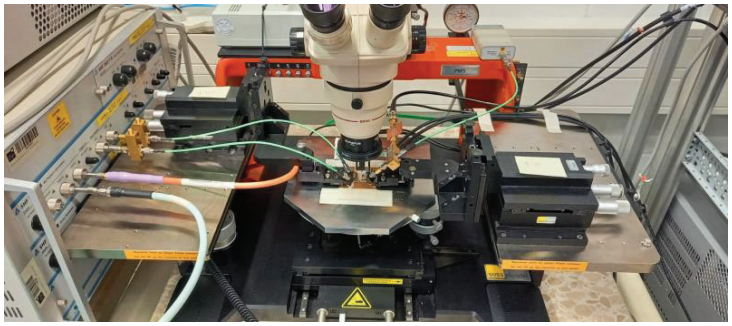

Figure 3. Measurement setup with PRBS source for the input signal and VCSEL equivalent circuit in the output acting as the load probed by a high-speed oscilloscope for eye diagram analysis.

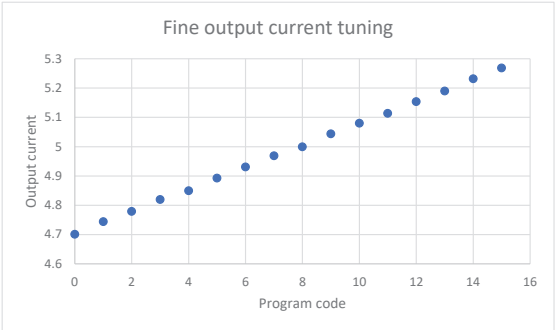

Figure 4. VCSEL driver fine output current controllability around a nominal VCSEL biasing current of 5 mA

The chipset features an aggregate power consumption of 160 mW per channel which accounts for 70 mW dissipated by the VCSEL driver and 90 mW by the TIA circuit.

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3. TRANCEIVER MODULE

3.1 Module overview

The OTRx was designed for mid-board optics assembly, according to the module design reported in [6]. The optical I/O consists of four transmit and four receive channels. They correspond to the respective quad VCSEL and PD arrays operating at 850 nm wavelength and they are interfaced through a standard MT connector with ribbon fiber array. The opto-parts along with the rad-hard Driver and TIA electronic ICs are flip-chip mounted onto a transparent carrier. The latter is also mounted on top of a PCB interposer, which implements the electrical interface. The module electrical I/O comprises 4 transmit and 4 receive differential pairs and pluggability to the host board is supported through a mini edge card connector.

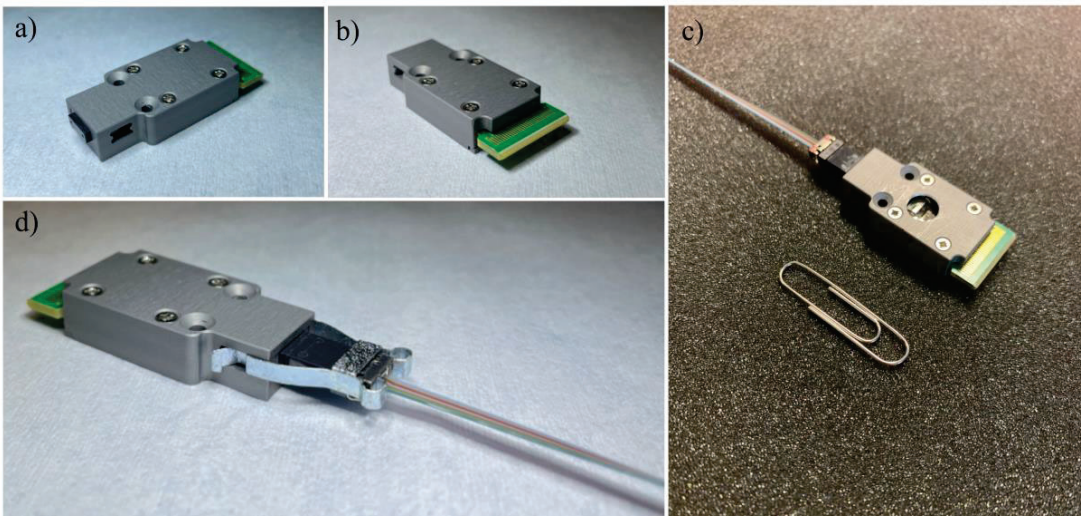

Figure 5. Packaged OTRx prototype module

Figure 5 a) and b) show the module front and rear view with the extruded MT ferule and PCB for optical and electrical connectivity respectively. Figure 5 c) shows the OTRx, with an MT ribbon fiber pigtail fitted, next to a paper clip for footprint comparison. Figure 5 d) shows the module with the pigtail fitted and a mechanical clip which secures the pigtail to the module package. The module weighs 6.4 grams (ex the pigtail) and occupies ~670 mm^2 on a form factor of 39.4 x 17 x 7.2 mm (L x W x H). The environmental and mechanical parameters of the module are summarized in Table 1. The OTRx operates on a single 3.3 V supply voltage and on a typical differential input voltage swing of 200 mVp-p and differential output voltage swing of 400 mVp-p.

Table 1. OTRx module environmental and mechanical parameters.

Parameter	Symbol	Target		Unit
Operating temperature	T_{op}	-40	+85	°C
Storage temperature	T_{stg}	-40	+100	°C
Electrical interface	-	MEC-5 connector		
Optical input interface	-	MT ferule		
Package size*	LxWxH	39.4 x 17 x 7.2		mm
Mass*	-	6.4		g
Power (Driver + TIA)	P_{dis}	160		mW/ch

*excluding fiber pigtail and MEC-5 connector

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3.2 Module testing

The OTRx module was tested in an optical loop-back configuration as shown in the schematic of Figure 6 a). A signal generator (Anritsu MG3697C) was used to provide the reference frequency to a PRBS generator (SHF 12105A). The PRBS generator provided the high-speed differential signal which was connected to the Device-Under-Test. The OTRx optical output was connected to a fan-out which provided access to individual Tx and Rx MM fibers terminated to FC/APC connectors. A Tx-Rx pair was directly connected through an FC/APC adaptor to form the optical loop back. The Rx differential signal output was connected to a pair of electrical channels of a Digital Sampling Oscilloscope (DSO - KEYSIGHT DCA-X 86100D) to capture the electrical eye diagrams.

Figure 6 b) shows the testbed and Figures 6 c) and d) illustrate the Device-Under-Test (DUT) configuration. The evaluation board hosts a MEC connector used to mount the OTRx, two multi-coaxial connector assemblies for RF connectivity and an embedded SPI module for digital control through a USB interface. The evaluation board was powered through a single 12 V supply voltage provided by an SMU (KEYSIGHT B2912A).

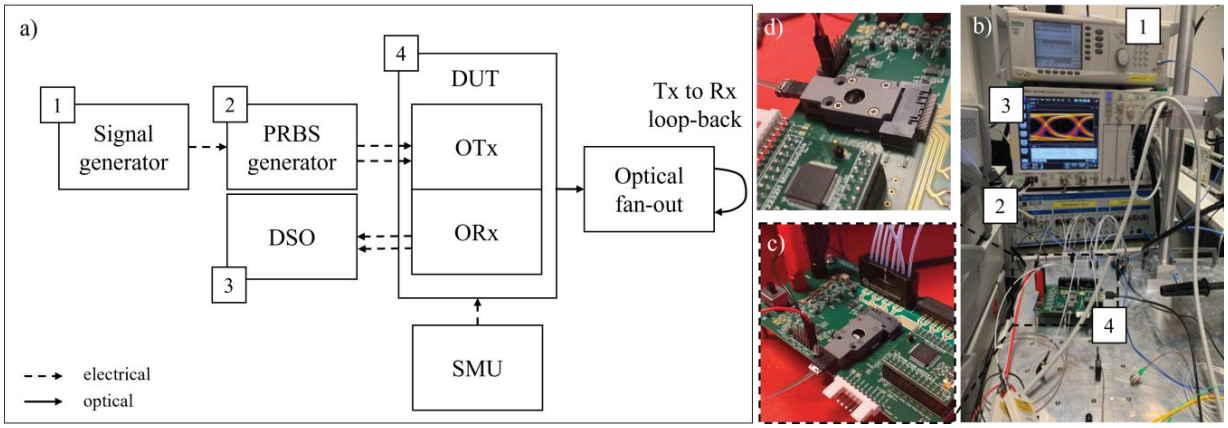

Figure 6. a) Test set-up schematic, b) testbed implementation, c) and d) DUT detail.

DUT evaluation was performed using a PRBS9 NRZ-OOK pattern at data rates up to 15 Gb/s. Figure 7 shows the eye diagrams recorded by the DSO at the Rx output at 6.25 Gb/s (left), 10 Gb/s (middle) and 15 Gb/s (right). The top and bottom rows show the captured eye diagrams at 2 UI and 4 UI time base. Open eye diagrams were captured, with bandwidth limitation and inter-symbol interference (ISI) effects starting to appear at 15 Gb/s data rates.

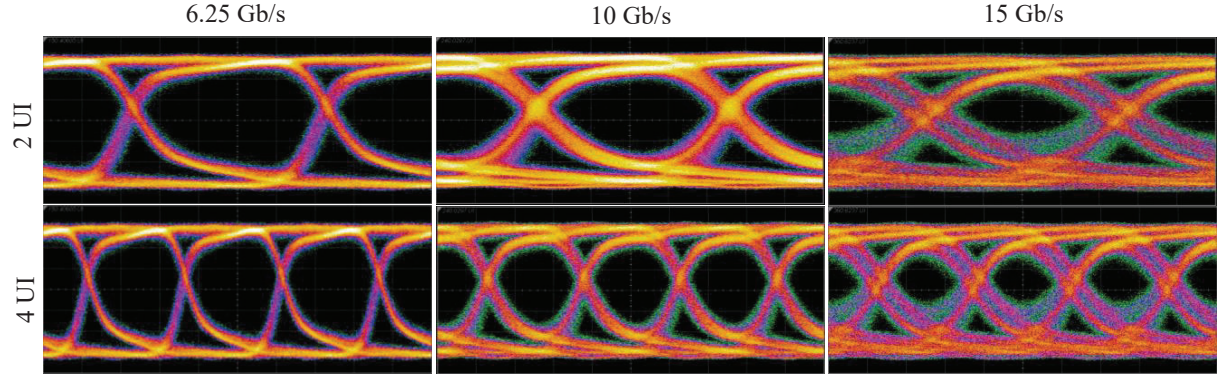

Figure 7. Captured eye diagrams at the Rx output at data rates of: (left) 6.25 Gb/s, (middle) 10 Gb/s and (right) 15 Gb/s. Time base is: (top-row) 2UI and (bottom row) 4UI.

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4. CONCLUSION

We have presented the progress of H2020-SPACE-SIPHODIAS project in the development of a new generation mid-board optics OTRx for optical intra-satellite interconnects. We have presented the fabricated VCSEL driver and TIA chipset in a 130 nm SiGe BiCMOS process as well as the assembly, integration and preliminary testing of the quad-channel, 850 nm OTRx module. Preliminary testing in loop-back configuration has validated the functional integrity of the device up to 15 Gb/s data rate per fiber. Work is underway to perform environmental evaluation as well as the assembly, integration and testing of a second generation OTRx with enhanced bandwidth performance.

5. ACKNOWLEDGEMENT

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