High Frequency Properties of an Integrated PJFET for Sensor Applications

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Abstract:

High frequency properties of a P-channel JFET modularly integrated in a 130 nm SiGe:C BiCMOS technology offering bipolar transistors with f_T / f_{max} of 300 GHz / 500 GHz are presented. The measured cut-off frequencies f_T / f_{max} of 3.5 GHz / 11 GHz are comparable with published values form physically faster N-channel JFET. Furthermore, the influence of de-embedding is demonstrated and the calculation of f_T based on |h21| and gm is compared.

Keywords: modularly integrated PJFET, cutoff frequencies (fT / fmax), open / short de-embedding

Introduction

Low noise transistors are essential in the first stage of read-out circuitries in sensor applications e.g. biomedical systems [1] or Radiation Detector in high energy physics [2]. Junction field effect transistor (JFET) transistors have like bipolar transistors very low 1/f noise characteristics but offer high input impedance, which is required for sensor read out circuitries.

In this work a short channel PJFET (p-channel JFET) with split channel region was modularly integrated in IHP's 130 nm SiGe:C BiCMOS (Silicon Germanium Carbon bipolar complementary metal oxide semiconductor) technology [3].

In Figure 1, the schematic cross-section (a) and the top view (b) of a quarter PJFET is depicted. The drawn gate and channel length are 0.31 μ m and 3.15 μ m respectively. An average channel width of 30 μ m of the presented transistor can be assumed. Since the measured test structure consists 4 devices (Figure 2), the total channel width is approximately 120 μ m.

The measured cut-off frequencies (f_T / f_{max}) of the presented PJFET are comparable to the performance of a physically faster NJFET with f_T = 2.5 GHz (estimated) published in [4] and measured f_T / f_{max} = 3.5 GHz / 23 GHz [5].

Radio frequency characterization

The radio frequency (RF) characterization up to 30 GHz was performed on-wafer using a semiautomated wafer prober equipped with two RFprobes for contacting the gate (G), source (S) and drain (D) electrode and two DC probes for biasing the bulk silicon (PSUB) and the back gate (BG) (shown in Figure 2).



Figure 1: Cross section (a) and quarter layout (b) of the presented short channel PJFET

The RF setup including network analyzer (Agilent 8364A), RF-cables and RF-probes was calibrated using an impedance standard substrate (ISS) and applying the Short-Open-Load-Thru (SOLT) method [6]. For extracting the scattering (S) parameters of the device under test (DUT) surrounded by the backend metal stack including comparatively large bond pads (see Figure 2) various methods can be found in literature. Here, the open / short (OS) de-embedding method [7] is applied. Therefore, scattering-parameters of an additional open and short structure are required.



Figure 2: The parasitic influence of the pads is de-embedded to extract the properties of the PJFET.

Source measurement units (SMU - HP4142B) are used to provide bias voltages and measure the currents. The maximum cutoff frequency was achieved with the following bias conditions $V_G = -0.2 \text{ V}$; $V_D = -3.3 \text{ V}$; $V_{BG} = 1 \text{ V}$; $V_{PSUB} = -3.3 \text{ V}$.

In Figure 3, the measured frequency dependent small signal parameter |h21| and Mason's unilateral power gain (U) are depicted. U is calculated using Eq. 1-3. The intercept points where |h21|=1 is defined as transit frequency (f_T) and U=1 is defined as f_{Max}.

$$nom = |Y21 - Y12|^2 \tag{1.}$$

 $det = 4(\Re e(Y11)\Re e(Y22) - \Re e(Y12)\Re e(Y21))$ (2.)

$$U = \frac{nom}{\det}$$
(3.)



Figure 3: Measured cut-off frequencies $f_T = f(|h21|)$ and $f_{max} = f(U)$ at ambient temperature. For comparison, Open / Short (OS) or no de-embedding is depicted.

In Figure 3 the transit frequency f_T is calculated using |h21|. Another possibility to calculate f_T based on the transconductance (gm) using the drain-source capacitance (c_{DS}) and the gate-source capacitance (c_{GS}) extracted from S-parameter measurements and converted to Y-parameters. Using equations 4-7 f_T is calculated versus operating frequency.

$$c_{GD} = \frac{-\Im \mathfrak{m}(Y12)}{2\pi f \left(1 + \frac{\Re e(Y12)}{\Im \mathfrak{m}(Y12)}\right)^2} \approx \frac{-\Im \mathfrak{m} \left(\frac{1}{1/1 - Y12}\right)}{2\pi f}$$
(4.)

$$c_{GS} = \frac{-1}{\Im m(1/(Y11+Y12))2\pi f}$$
(5.)

$$gm = \frac{-1 \cdot \frac{|T_{21} - T_{12}|}{|Y_{11} + Y_{12}|}}{\Im(1/Y_{11} + Y_{12})} \approx |Y_{21} - Y_{12}|$$
(6.)

$$f_{T_gm} = \frac{gm}{2\pi(c_{GS} + c_{GD})}$$
(7.)

For comparison of f_T based on |h21| and gm are plotted versus operating frequency in Figure 4. The difference between the two characteristics is not significant. Nevertheless, $f_T(|h21|)$ is not as constant as $f_T(gm)$.



Figure 4: Comparison of open / short de-embedded f_T = f(gm) and $f_T = f(|h21|)$ versus measurement frequency

Conclusion

The measured and open / short de-embedded cut-off frequencies f_T / f_{max} of the modularly integrated PJFET are 3.5 GHz / 11 GHz. Thus, comparable to the RF-performance of the physically faster NJFET. $f_T(|h21|)$ and $f_T(gm)$ show similar values while $f_T(|h21|)$ has a stronger frequency dependence.

References

- M. Safavi-Naeini et al., "Evaluation of Silicon Detectors With Integrated JFET for Biomedical Applications," *IEEE Trans. Nucl. Sci.*, pp. 1051-1055, June 2009.
- [2] G.-F. Dalla Betta et al., "Low Noise Junction Field Effect Transistors in a Silicon Radiation Detector Technology," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 5, pp. 3004-3012, 2006.
- [3] H. Rücker, B. Heinemann and A. Fox, "Half-Terahertz SiGe BiCMOS technology," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pp. 133-136, 16-18 Jan. 2012.
- [4] L. Sturm-Rogon, K. Neumeier and C. Kutter, "Low-Noise Si-JFETs Enhanced by Split-Channel Concept," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4789-4793, Nov 2020.
- [5] Y. Shi et al., "A cost-competitive high performance Junction-FET (JFET) in CMOS process for RF & analog applications," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 237-240, May 2010.
- [6] A. Fraser, R. Gleason and E. Strid, "GHz onsilicon-wafer probing calibration methods," *IEEE Proc. of the BCTM*, pp. 154-157, Sep. 1988.
- [7] M. Koolen, J. Geelen and M. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," *IEEE Proc. of the BCTM*, pp. 188-191, Sep. 1991.