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High Crystallinity Ge Growth on Si (111) and Si (110) by Using Reduced Pressure Chemical Vapor Deposition

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A method for high quality epitaxial growth of Ge on Si (111) and Si (110) is investigated by reduced pressure chemical vapor deposition. Two step Ge epitaxy (low temperature Ge seed and high temperature main Ge growth) with several cycles of annealing by interrupting the Ge growth (cyclic annealing) is performed. In the case of Ge seed layer growth below 350 °C for (111) and 400 °C for (110) orientation, huge surface roughening due to too high dislocation density is observed after the following annealing step. For both crystal orientations, a high crystallinity Ge seed layer is realized by combination of 450 °C growth with 800 °C annealing. Once the high-quality Ge seed layer is deposited, high crystal quality Ge can be grown at 600 °C on the seed layer for both crystal orientations. For the 5 μm thick Ge layer deposited with the cyclic annealing process at 800 °C, a Si diffusion length of ~400 nm from the interface, RMS roughness below 0.5 nm and threading dislocation density of 5×10^6 cm^{-2} are achieved for both (111) and (110) substrates.

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Heteroepitaxial growth of Ge on Si has great interest for various optoelectronic applications such as Ge photodiodes[1–5] and also for virtual substrate for GeSn,[6,7] SiGeSn[8,9] and also for III-V materials.[10] One of the key parameters to realize high quality heteroepitaxy is to manage strain due to the lattice mismatch between Si substrate and the deposited epitaxial layers. In the case of Ge growth on Si, the lattice mismatch is 4.2%.[11] In the initial stage of the Ge growth on Si, the heteroepitaxial strain induces local elastic deformation at the heterointerface, resulting in island growth by Stransky-Krastanov mechanism. The island growth formation can be avoided by lowering the initial growth temperature of Ge, however, after exceeding a critical thickness, of only a few nm in the Ge/Si case, it is not possible to avoid plastic relaxation induced by misfit dislocations (MD) and threading dislocations (TD).[12] High density of MDs and the TDs causes a degradation of crystallinity of Ge.

Recently, the process development of heteroepitaxial Ge growth on Si (001) is widely investigated by using chemical vapor deposition (CVD) and high-quality Ge (001) growth techniques such as thermal cycling,[13–15] graded buffer[11,12] are reported. In previous works, we have reported about the cyclic annealing process, which contains several cycles of annealing by interrupting the Ge deposition steps.[16–18] By these Ge growth techniques, high quality Ge growth with TDD of below 1×10^7 cm^{-2} is realized on Si (001) surface. Moreover, other crystal orientation such as the Ge (111) surface is also interesting because of higher carrier mobility.[19] Furthermore, Ge (110) is the preferred orientation of virtual substrates (VS) for epitaxial graphene growth.[20] In the case of Ge deposition on Si (111) and Si (110) substrates, it seems that the process conditions used for Ge growth on Si (001) are not suitable to realize high crystallinity and a smooth surface.[21] In this paper, we investigate a method of high quality and smooth Ge layer growth on Si (111) and Si (110), which is nearly the same level as the Ge growth on Si (001) by cyclic annealing process.

Experimental

Epitaxial growth of Ge on Si (111) and Si (110) is carried out using a reduced pressure (RP) CVD system. Non-structured on-oriented Si (111) and Si (110) standard test wafers were used as substrates. After standard Radio Corporation of America clean followed by diluted HF dip, the wafer is loaded into the RPCVD reactor and baked at 1000 °C in RP under H_2 environment to remove residual oxide. After that, the wafer is cooled down to 600 °C in H_2. Then, the carrier gas is switched to N_2 and further cooled down to 300 °C–500 °C to form a hydrogen-free Si surface. After stabilizing the temperature, a 100 nm thick Ge layer is deposited as a seed layer using GeH_4 with N_2 carrier gas. In order to investigate the influence of annealing on the crystallinity of the Ge seed layer, an annealing at 600 °C to 800 °C is performed in H_2 for selected wafers. Furthermore, the wafer is cooled down to 450 °C–700 °C in H_2 and 400 nm to 5 μm thick Ge is deposited using a H_2-GeH_4 gas mixture as a main part of Ge growth. For TD density (TDD) reduction, cyclic annealing in H_2 is performed at 800 °C for several minutes at total Ge thickness of 0.4 μm or 0.5 μm and 1 μm, as well as every following 1 μm deposition step.

Atomic-force microscopy (AFM) is used for surface roughness analysis. Spectroscopic ellipsometry and scanning electron microscopy (SEM) are employed for Ge thickness measurement. Scanning transmission electron microscopy (STEM) and X-ray diffraction (XRD) are used for structural characterization of the Ge layer. Secondary ion mass spectroscopy (SIMS) is utilized to evaluate the diffusion length of Si into Ge. Etch pit count by Secco defect etching combined with angle view SEM or optical microscope are used for TDD evaluation. By our Secco etching technique, good agreement of the etch pit density and TDD measured by plan-view TEM is obtained.[16]

Results and Discussion

Ge seed layer growth.—In Figs. 1a, 1b, the root mean square (RMS) surface roughness of 100 nm thick Ge (111) and Ge (110) seed layers before / after postannealing is summarized. Ranges of the growth temperature and postannealing temperature are 300 °C–550 °C and 600 °C–800 °C, respectively. In the case of the Ge growth on the Si (111) surface at 300 °C, a RMS roughness of 6.3 nm is observed at as-deposited condition. The RMS roughness is not affected by postannealing at 600 °C, but significantly increased after postannealing at 700 °C. In the case of the Ge growth at 350 °C, the strong roughening starts not for postannealing at 700 °C, but at 800 °C. By depositing at 400 °C or higher temperature, no increase of RMS roughness is observed after postannealing. Similar behavior is observed for the Ge growth on Si (110) surface. In the case of Si (110) substrate, strong increase of the surface roughness is observed after postannealing at 800 °C when the Ge layer growth temperature

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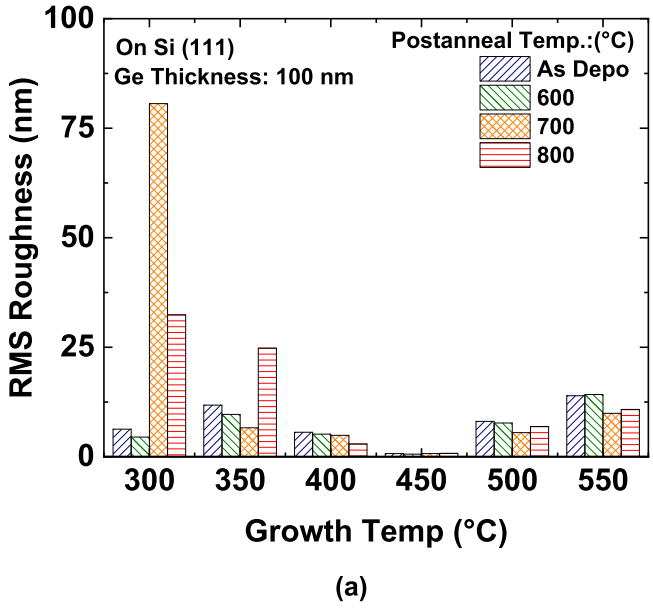
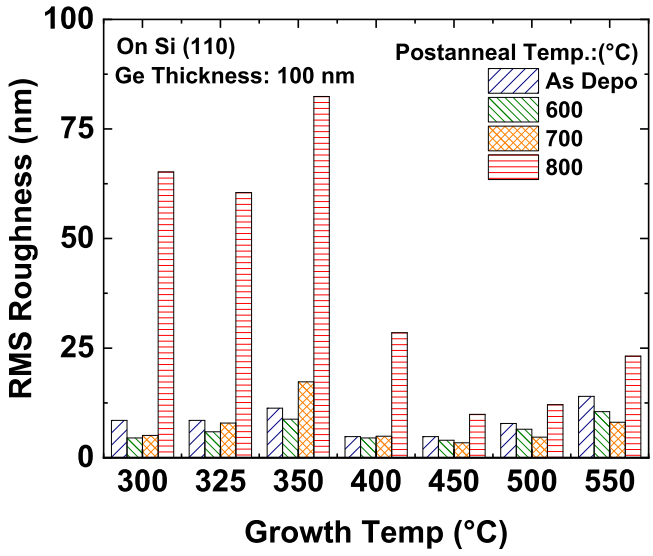


(a)



(b)

Figure 1. RMS roughnesses of 100 nm thick seed Ge layers deposited on (a) Si (111) and (b) Si (110) at different growth temperatures. The RMS roughnesses of as deposited and postannealed Ge surfaces at 600 °C, 700 °C and 800 °C are summarized.

is below 350 °C. The surface roughening by postannealing becomes moderate for the Ge grown at 400 °C. For both crystal orientations, the lowest RMS roughness is obtained by depositing at 450 °C. The increased surface roughness at 500 °C and 550 °C is caused by a Stransky-Krastanov growth mechanism caused by the increased surface mobility of adsorbed Ge atoms at high temperature. The maintained RMS roughness even after postannealing at 800 °C may indicate good crystal quality even at as-deposited condition.

In order to confirm the influence of the growth temperature on the crystallinity, cross section STEM images of the 100 nm thick Ge (111) and Ge (110) seed layers deposited at 300 °C and 450 °C are shown in Figs. 2a–2d. By depositing Ge at 300 °C (Figs. 2a, 2b), a very high density of stacking faults (SF) on {111} planes and high surface roughness are observed. Near the interface between the Ge layer and Si substrate, a higher density of SF is observed for both crystal orientations. In contrast, by depositing at 450 °C (Figs. 2c, 2d), the SF density in the Ge layer is reduced compared to that grown at 300 °C for both crystal orientations. In the case of the Ge seed layer growth at 450 °C, the dislocation density is relatively low already at as deposited condition, therefore it seems that further reduction of the dislocation density is realized by migration of Ge atoms and dislocation networks to reduce non-uniform local strain around the dislocations. However, in the case of growth at 300 °C, the crystallinity cannot be improved by the postannealing, because the too-high density of dislocations and SFs may cause irregular migration of the Ge atoms and the dislocation networks. As a result, surface roughening occurs after the postannealing for the Ge layers deposited at 300 °C. It is possible to conclude that under our process conditions, optimal growth temperature for the Ge seed layer is 450 °C followed by annealing at 800°C for both (111) and (110) crystal orientations.

Second part of Ge growth.—The RMS roughness of 500 nm thick Ge (111) and 400 nm thick Ge (110) surfaces before and after postannealing at 800 °C are summarized in Figs. 3a, 3b. The growth temperature is varied from 300 °C to 650 °C. For all cases, a 100 nm

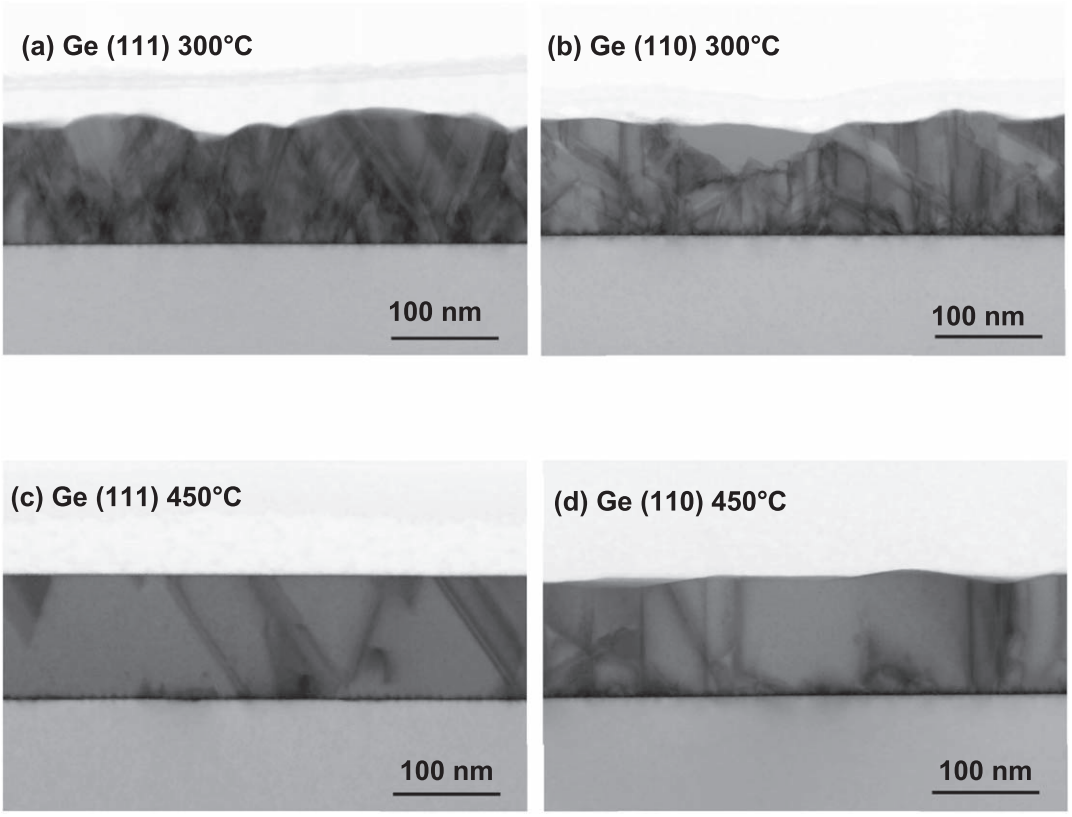
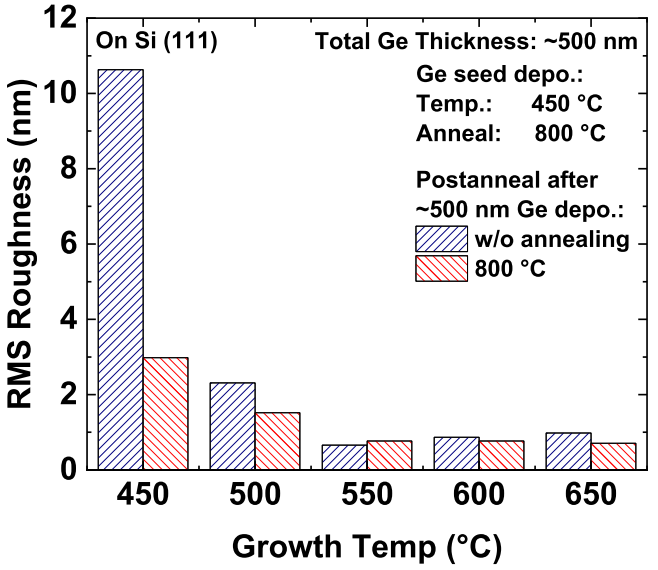


Figure 2. Cross section bright field STEM images of 100 nm thick Ge seed layers. All layers are as deposited condition. Growth temperatures of (a), (b) are 300 °C, and (c), (d) are 450 °C, respectively. Crystal orientations of (a), (c) are (111) and (b), (d) are (110), respectively.

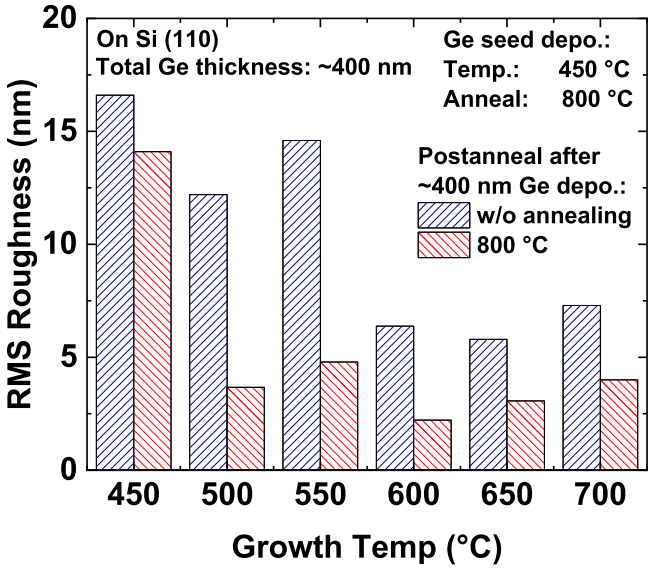
thick Ge seed layer is deposited at 450 °C with 800 °C annealing. Additionally, in Figs. 4a–4h, AFM images of Ge (111) and Ge (110) surfaces deposited by process conditions summarized in Table I are shown. In the case of Ge growth at 450 °C on the Ge (111) seed layer, a high surface roughness (RMS roughness of 10.63 nm (Fig. 3a) due to triangle island formation (Fig. 4a is observed. The triangle pyramid formation may be caused by non-uniform strain distribution of the Ge seed layer due to the presence of defects and insufficient growth temperature to allow for Ge migration. With an increase of the Ge growth temperature, the surface morphology of the as-deposited Ge (111) surface becomes smoother and below 1 nm of RMS roughness is obtained above 550 °C (Fig. 3a). Above 550 °C, no improvement of the surface roughness is observed for the Ge (111) surface. As shown in Fig. 4c, a very smooth Ge (111) surface, with a RMS roughness of 0.87 nm, is realized at 600 °C. On this surface, atomic terraces with a height of ∼0.3 nm is observed. By postannealing this sample at 800°C, the RMS roughness is not significantly improved, however a smoother shape of the atomic terraces is observed (Fig. 4e), which may be indicating improved TDD. On the other hand, in the case of (110) crystal orientation (Fig. 3b), a high surface RMS roughness of ∼18.63 nm due to pit formation is observed at 450 °C, as shown in Fig. 4b. The high density of the pits formation in similar shape is also observed for the Ge (110) layers deposited at 500 °C and 550 °C. If the Ge layers are deposited at temperatures higher than 600 °C, reduced pit formation is observed, as shown in Fig. 4d. The surface roughness of the Ge (110) deposited between 600 °C and 700 °C is between ∼6.4 nm to ∼7.3 nm. The higher surface roughness compared to the Ge (111) surface may be due to the presence of perpendicular SFs oriented towards the growth front, as shown in cross section STEM images in Figs. 2b, 2d. By introducing postannealing at 800 °C, the Ge surface morphologies are changed for all deposition temperatures. The RMS roughness is improved by the postannealing except for the Ge sample deposited at 450 °C. In the case of the Ge layer grown at 450 °C, its crystallinity seems not high enough, resulting in irregular migration of Ge atoms and dislocation networks. The lowest RMS roughness of 2.22 nm for the Ge (110) surface is realized by depositing at 600 °C followed by postannealing at 800 °C. Even though the same process condition is used for the second Ge part, huge surface roughening is observed if the Ge seed layer is deposited at 300 °C without annealing (i.e. Ge growth on a seed layer with high dislocation density) (Figs. 4g, 4h). High crystallinity Ge seed layer must be prepared for depositing high quality Ge.

Figure 5a shows the RMS roughness of Ge (111) and Ge (110) as function of Ge thickness. A 100 nm Ge seed layer is deposited at 450 °C with 800 °C annealing for all cases and following the second part of the thick Ge growth is performed at 600 °C with cyclic annealing at 800 °C. In the case of the Ge (111), a surface RMS roughness below 1 nm is observed already even after the first 100 nm thick Ge seed layer deposition (also shown in Fig. 1a). The surface roughness is slightly decreased with increasing thickness, and after 5 μm deposition, an RMS roughness of 0.51 nm is obtained. On the surface of the 5 μm thick Ge (111) layer, triangular cross hatch structures along the ⟨110⟩ directions are observed, as shown in Fig. 5b. Terraces of ∼0.3 nm step height, which is close to the bilayer height of Ge (111) surfaces (0.337 nm), are clearly visible. On the other hand, in the case of the Ge (110) surface, the RMS roughness of the 100 nm thick Ge seed layer is 9.91 nm. With increasing the Ge thickness, the surface roughness is decreased and a RMS roughness of 0.35 nm is realized for 5 μm thick Ge. Atomic terraces with a height of 0.2 nm, which is almost the same height as a monolayer height of Ge (110), are clearly seen. The presence of the smooth atomic terraces on the surface of the Ge (111) and Ge (110) is indicating high crystal quality for both crystal orientations. The surface roughnesses of 5 μm thick Ge (111) and Ge (110) are comparable level as 5 μm Ge grown on Si (001).[16]

Figure 6 shows a SIMS depth profile near the interfaces of the Si (111) and Si (110) substrates and the 5 μm thick Ge. Because of



(a)



(b)

Figure 3. RMS roughness of (a) Ge layers deposited on (a) 100 nm thick Ge (111) seed layer and (b) Ge (110) seed layers. RMS roughness of Ge surfaces of as deposited and after postannealing at 800°C are plotted. Ge thicknesses shown in (a) and (b) are 500 nm and 400 nm, respectively. For both crystal orientations, the 100 nm thick Ge seed layers are deposited at 450 °C in N_2 carrier gas followed by 800 °C annealing in H_2. H_2-GeH_4 gas system is used for the second part of the Ge growth.

several cycles of annealing at 800 °C, Si diffuses into the Ge layer for both orientations. The diffusion lengths of both layers are ~400 nm, which is also similar to our previous results of Ge growth on Si (001).[16,17]

Figure 7 shows TDD as function of Ge thickness for deposited on Si (111) and Si (110) surfaces. In the case of 500 nm thick Ge deposition using the cyclic annealing process at 800 °C, TDDs of $\sim 3.7 \times 10^8\,cm^{-2}$ are obtained for both crystal orientations. With increasing Ge thickness, a reduction of the TDD is observed. No clear difference of the TDD is observed between (111) and (110) orientation, even though surface morphologies are different as shown in Figs. 5a–5c. Compared to the Ge growth on the Si (001)

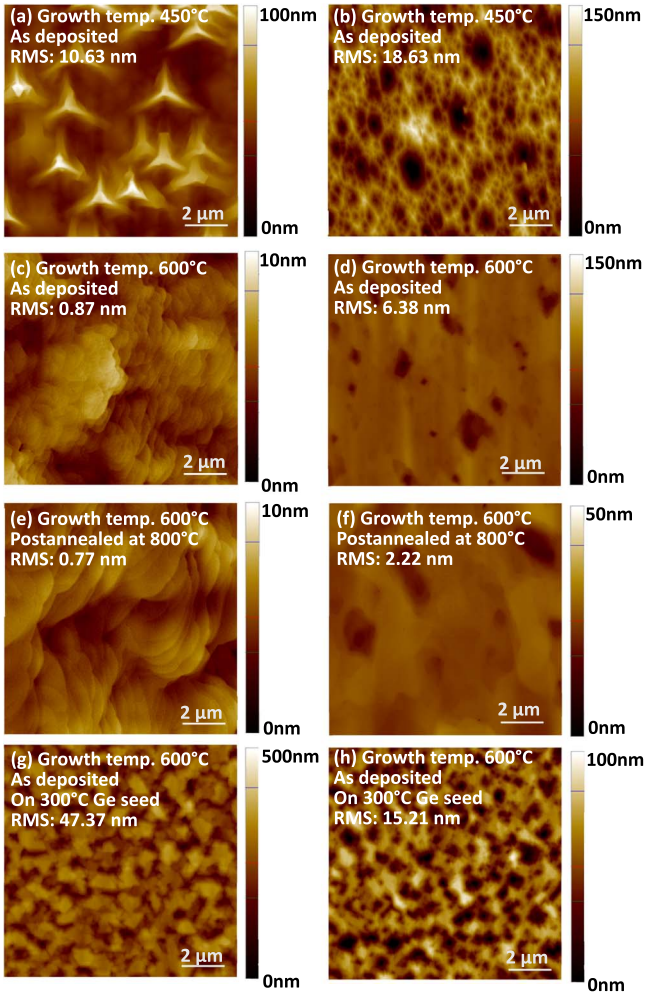


Figure 4. AFM surface images of (a, c, e, g) 500 nm thick Ge (111) and (b), (e), (d), (f) 400 nm thick Ge (110). For both crystal orientations, 100 nm thick Ge seed layers are deposited at (a)–(f) 450 °C followed by annealing at 800 °C, and at (g), (h) 300 °C without annealing. Growth temperatures of the main part of the Ge layer are (a), (b) 450 °C and (c)–(h) 600 °C. (a)–(d), (g), (h) shows the as-deposited surface and (e), (f) shows the Ge surface after postannealing at 800 °C. Process conditions of these wafers are summarized also in Table I.

surface, reduction of the TDD by increasing the Ge thickness is slightly lower, but the TDD is decreased to $\sim 4.9 \times 10^6\,cm^{-2}$ by 5 μm thick Ge deposition for both (111) and (110) orientations. Low TDDs, which is nearly comparable level as the 5 μm thick Ge (001) of $\sim 1 \times 10^6\,cm^{-2}$, are realized.

Cross section STEM images of the 5 μm thick Ge (111) and Ge (110) are shown in Figs. 8a, 8b. For both crystal orientations, most of the TDs are located near the interface between Ge and Si substrate. Above ~1.5 μm from the Si interface, almost no TDs are observed by STEM analysis, which may indicate a low TDD also in the deeper part of the Ge layer. The TD reduction occurs by migration of TD networks. The driving force of the migration is the reduction of local strain fluctuation to reduce strain energy. By the cyclic annealing process, a reduction of TDD at the surface of the deposited layer is expected. Therefore, the crystallinity of Ge deposited on the annealed surface should be improved compared to that for simple continuous deposition. By subsequent annealing, reduction of TDD occurs not only in the newly deposited Ge part, but also in the deeper region by migration of TD networks. By the cyclic annealing process, more efficient TD reduction occurs due to presence of the part with improved crystallinity on the top of the Ge layer. The high crystallinity layer enables the TD migration by reduction of strains around the defects which are located at distant

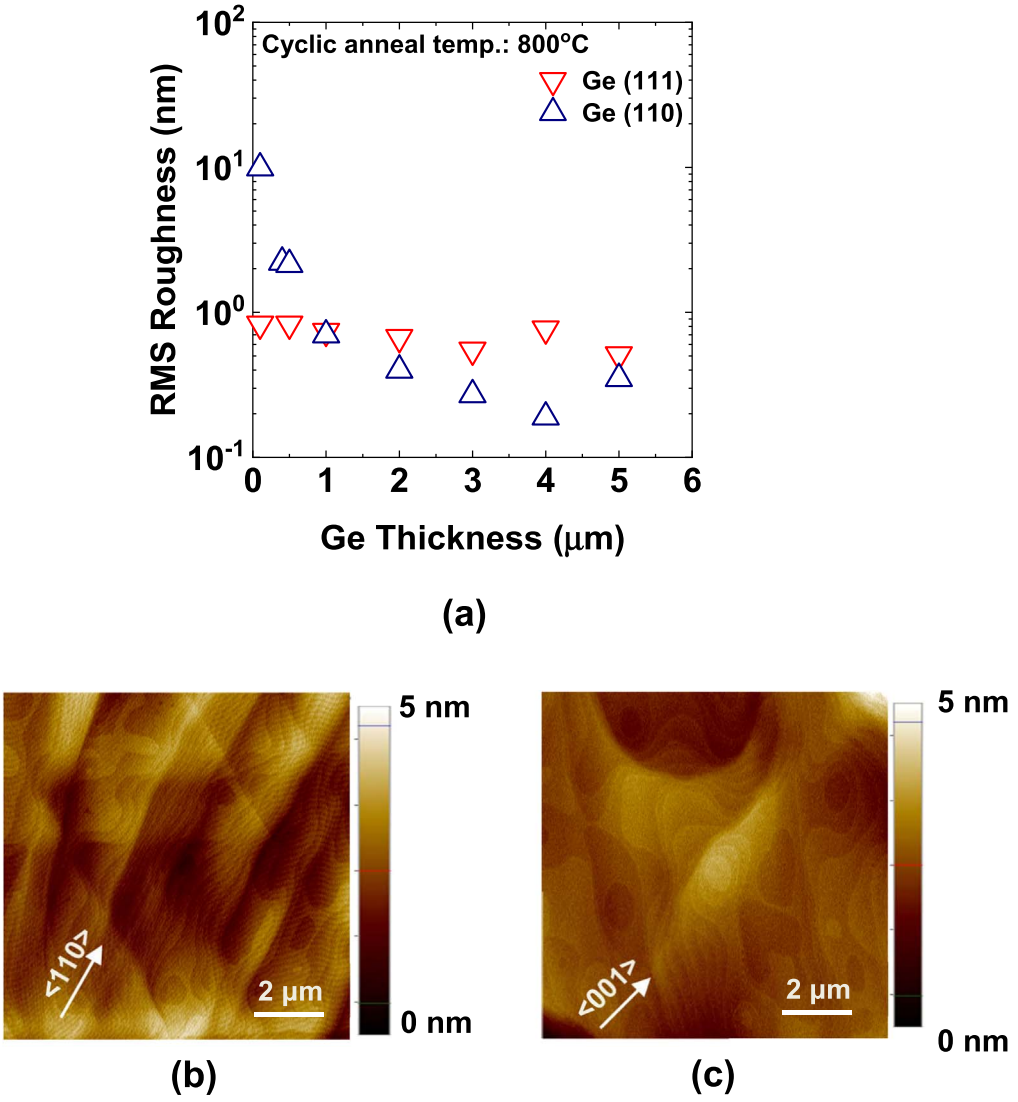


Figure 5. (a) RMS roughness of Ge (111) and Ge (110) as function of Ge thickness, using cyclic annealing at 800 °C. For both crystal orientations, the Ge seed layers are deposited at 450 °C followed by 800 °C annealing. (b) and (c) shows AFM images of 5 μm thick Ge (111) and Ge (100) surfaces using the cyclic annealing process.

Table 1. Summary of samples shown in Fig. 4 (a-h). Crystal orientation of substrate, growth condition of Ge seed layer, growth temperature of second part of Ge and postannealing temperature are summarized.

#	Substrate Orientation	Ge seed layer		2nd part of Ge layer	
		Growth temp. (°C)	Annealing temp. (°C)	Growth temp. (°C)	Postannealing temp. (°C)
(a)	(111)	450	800	450	As deposited
(b)	(110)				
(c)	(111)				
(d)	(110)				
(e)	(111)			600	800
(f)	(110)				
(g)	(111)	300	Without annealing		As deposited
(h)	(110)				

places. Near the interface, it is known that there is a high TDD region which might cause degradation of device performance. However, by depositing thick Ge layer with the cyclic annealing process, it is possible to realize improved TDD level even near the interface region compared to that of thin Ge layer using conventional growth technique with same annealing temperature.

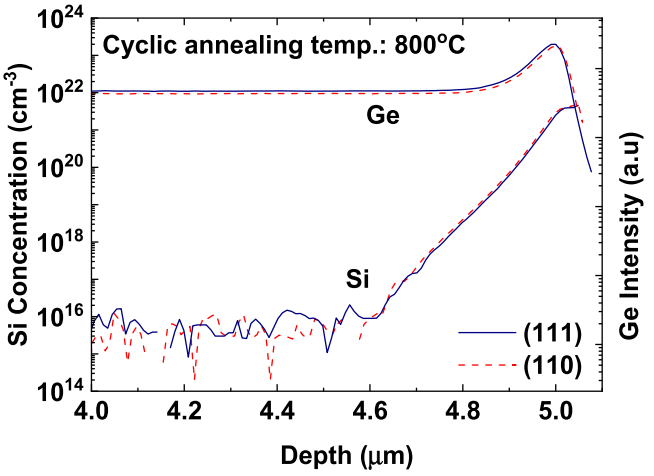


Figure 6. SIMS depth profile of Ge and Si near the interface of 5 μm thick Ge (111) and Ge (110) deposited by cyclic annealing process. Temperatures of the Ge seed layer deposition, main part of the Ge growth, and cyclic annealing are 450 °C, 600 °C and 800 °C. Si implanted Ge is used as a calibration sample.

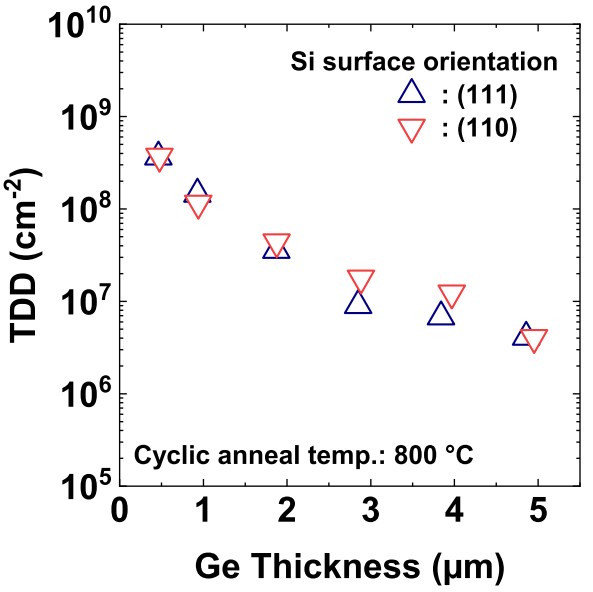


Figure 7. TDD as function of Ge thickness deposited on Si (111) and Si (110) using the cyclic annealing process. The cyclic annealing temperature is 800 °C for both crystal orientations.

Images of the XRD RSMs around the specular Ge (111) and Ge (220) Bragg diffraction of the 5 μm thick Ge layers are shown in Figs. 9a, 9b. The normalized Ge peak intensities of a 500 nm and a 5 μm Ge (111) and Ge (220) layer along the direction of the in-plane scattering vector Q_x are shown in Figs. 9c, 9d. In Figs. 9a, 9b, sharp streaks toward the out-of-plane direction Q_z are observed for both crystal orientations. The sharp streaks are the crystal truncation rods of the high quality Ge layers, which are due to the scattering from its sharp and smooth surface.[22] In Figs. 9c, 9d, with increasing Ge

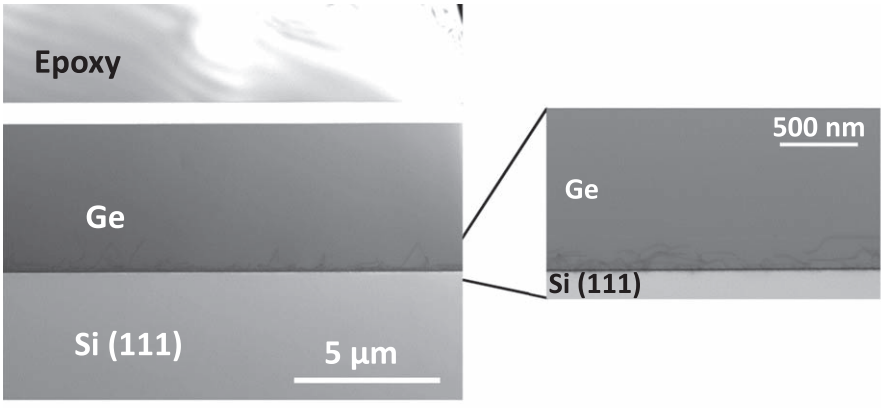


Figure 8. Cross section bright field STEM images of 5 μm thick (a) Ge (111) and (b) Ge (110) layers with cyclic annealing process at 800 °C. Higher magnification images near the interface between Si and Ge are also shown.

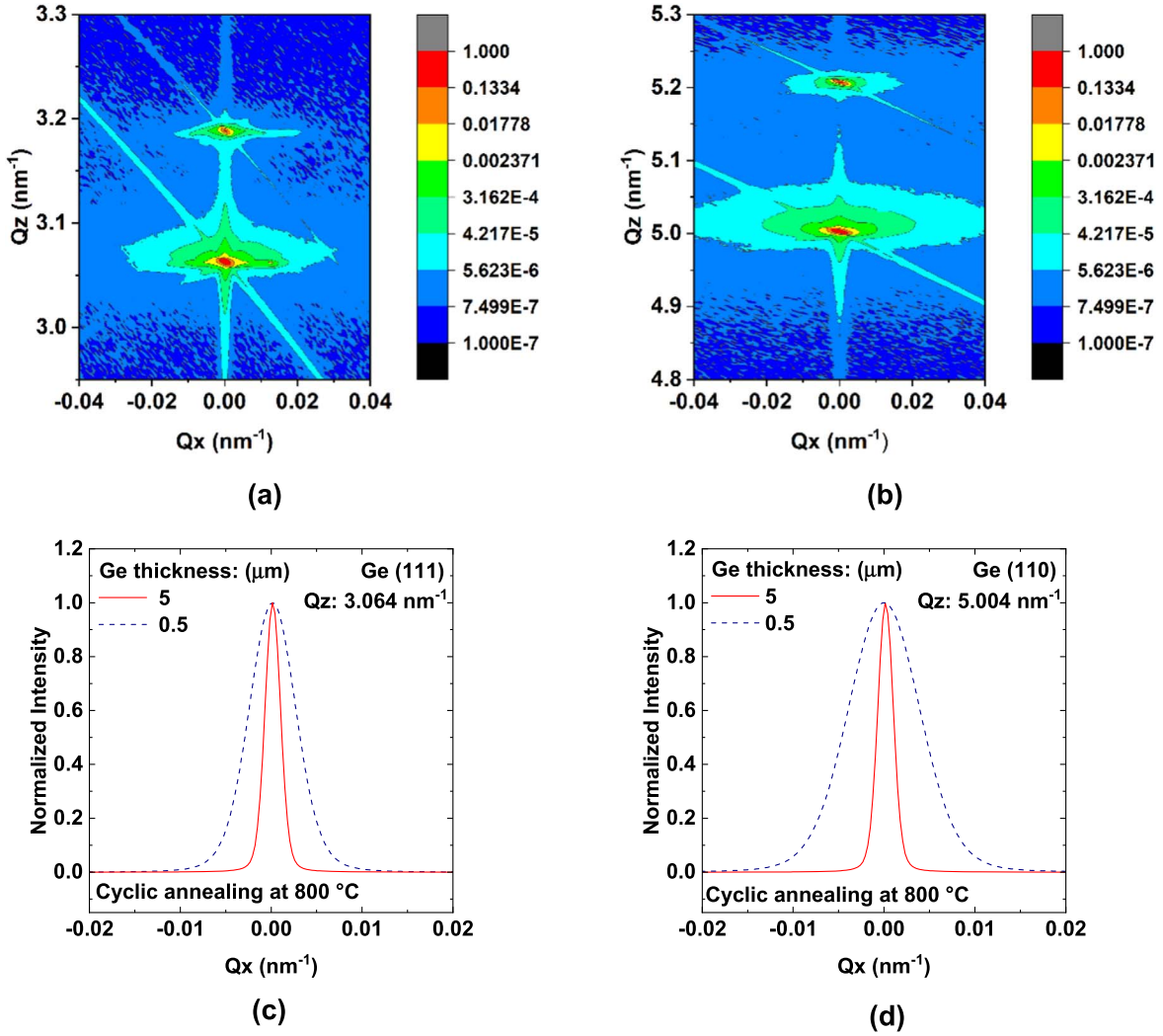


Figure 9. XRD RSM images around (a) Ge (111) and (b) Ge (220) Bragg diffraction peaks. Rocking curve scans of 500 nm and 5 μm thick Ge (111) at Q_z = 3.064 nm^{-1} and 500 nm and 5 μm thick Ge (220) at Q_z = 5.004 nm^{-1} are plotted in (c) and (d), respectively.

thickness from 500 nm to 5 μm, the full-width of half-maximum (FWHM) values of the Ge (111) and Ge (220) Bragg diffraction peaks decreases from 6.48 $\times$ 10^{-3} nm^{-1} to 2.47 $\times$ 10^{-3} nm^{-1} and 9.48 $\times$ 10^{-3} nm^{-1} to 2.46 $\times$ 10^{-3} nm^{-1}, respectively. The lower Ge peak width indicates less presence of tilted lattice planes in the Ge, which are induced by the TDs, thus indicating high crystal quality. These results also support that improvement of crystal quality occurs with increasing Ge thickness.

Conclusions

High quality epitaxial Ge deposition method on Si (111) and Si (110) surfaces investigated by using RPCVD. Two step (low / high temperature) Ge epitaxy with cyclic annealing at 800 °C, which contains several cycles of annealing by interrupting the Ge growth, is performed. For both crystal orientations, RMS roughness of below 0.5 nm and TDD of 5 $\times$ 10^6 cm^{-2} are achieved for 5 μm thick Ge by depositing at 450 °C for the Ge seed layer and at 600 °C for the main part of the Ge layer. The surface roughness and TDD are almost comparable level to the 5 μm thick Ge grown on Si (001). By the cyclic annealing at 800 °C, Si diffusion into Ge is limited to ~400 nm from interface for both crystal orientations. This method shown here may be applied for Ge (111) and Ge (110) VSs fabrication for emerging devices which requires high carrier mobility and for high quality graphene growth, respectively.

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