Piezo Electric Properties of Epitaxial SiGe

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Abstract

Strain sensors are highly demanded in industrial fields such as for precise torque control of electrical motors as well as for manipulators of industrial robots to handle soft materials to recognize the state of grabbed objects(1,2). Polycrystalline-Si based membrane sensors have great potential for downscaled and monolithic integration because their small occupying area enables high density arrays with a relatively large physical change for high sensitivity. However, by downscaling, fluctuations of the device properties, due to variation of polycrystalline grain size, become more pronounced, which strongly reduces the sensing reliability of the devices. This fluctuation could be improved by switching from polycrystalline to single crystal material. In last three decades, polycrystalline Si has been widely used as an effective material for highly sensitive strain sensors. In this study, we evaluate piezo resistivity of epitaxial SiGe to assess its potential and feasibility for strain sensor applications.

The piezo resistivity of epitaxial SiGe layers is investigated based on using the gauge factor (GF). 100 nm-thick, B-doped SiGe with 10, 20 and 30% Ge content is pseudomorphically grown using reduced pressure chemical vapor deposition on n-type Si(001). B concentrations are varied from ~1×10^{17} to ~1×10^{19}cm^{-3} verified by SIMS measurements. The deposited SiGe is patterned by photolithography and dry etching to form a 16µm wide and 300µm long stripe as schematically shown in Fig. 1 (a). Afterwards the SiGe is passivated by 200nm thick SiO_2 and windows for metal contact pads are opened. In order to ensure ohmic contact for the metal contact pads a layer stack consisting of Al/~30nm-thick Ni/Ni silicide/~50nm-thick ~1×10^{19}cm^{-3} B-doped Si was deposited onto the SiGe layer as schematically shown in Fig. 1 (b). Then, the substrate is thinned down to 200µm and diced to 2×2cm^2 square. The test structure is located at the center of the diced wafer. In order to prevent unintended relaxation of the deposited SiGe layer, temperatures for following post-epitaxy processes are limited to below 550°C.

In order to measure the piezo resistivity, the resistance is determined using four-terminal measurement with bending the sample by four-point bending method as shown in Fig. 2(3). By the wafer bending, uniaxial compressive strain along the 300µm direction is externally applied. The GF is estimated by slope of relative resistivity as function of induced strain.

In Fig. 3, GFs of the SiGe as function of resistivity with 10, 20 and 30% Ge content are summarized. For this experiment, SiGe growth is performed at 600°C for all samples. In the case of higher resistivity, (i.e. sample with lower B concentration), higher GF is observed. Within the same resistivity, slightly higher GF is obtained for the SiGe with higher Ge content. A possible interpretation would be, the GF is related to hole mobility. The hole mobility enhancement is expected by increased Ge content in the SiGe and externally introduced additional uniaxial compressive strain along current flow direction(4). In the case of higher carrier concentration, the hole mobility enhancement is less pronounced due to scattering. However, further investigation is required to understand the mechanism behind.

Next, in order to discuss influence of the SiGe growth conditions on the GF, GF of $Si_{0.8}Ge_{0.2}$ grown different growth temperature is compared. Resistivity of all samples is $6\times10^{-1}\Omega$cm. In the parallel experiment, no plastic strain relaxations of the SiGe are confirmed for the process conditions used for this experiment. It seems even though Ge concentration, thickness and carrier concentrations are the same, electrical property of the deposited SiGe is influenced by changing the growth temperature.

In order to investigate a possible reason of the influence of the SiGe growth condition on the GF, C-V characteristics of SiGe are evaluated by fabricating MOS structures. In order to reduce interface state density, a 10 nm thick Si cap layer is deposited on the SiGe layers to prevent Ge oxide formation at the oxide Si interface. The evaluation of electrical interface and bulk parameters by means of simultaneously measured high- and low frequency MOS C-V characteristics in non-steady state non-equilibrium indicate that lower density of recombination-generation centers are existing for the SiGe grown at lower temperature. Therefore, higher crystal quality is confirmed for the $Si_{0.8}Ge_{0.2}$ layer grown at lower temperature.

These results shown here gives prospect for tuning of SiGe based piezo resistivity sensors.

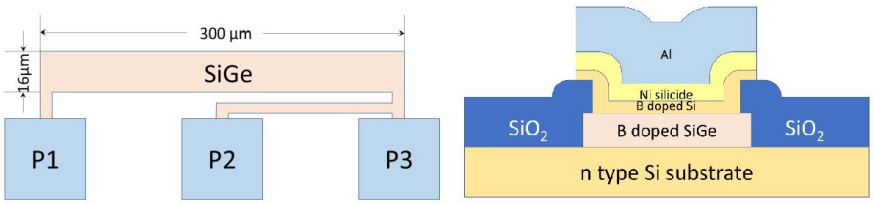
References

(1) H. Liu et al., Nanomachines **8** 10, 304 (2017)

(2) M. Amjadi et al., Adv. Funct. Mater. **26** (11), 1678 (2016)

(3) N. Inomata et al., Sens. Act. A, **346** 16 113823 (2022)

(4) M.V. Fischetti et al. J. Appl. Phys. **80**, 2234 (1996)



(a) (b)

Fig. 1. (a) Schematic top-view image of piezo resistivity measurement structure and (b) cross sectional diagram of Metal contact pads area. The SiGe structure is covered by CVD SiO_2. Al with Ni silicide is used for contact pads at P1, P2 and P3. Length and width of SiGe layer are 300 µm and 16 µm, respectively.

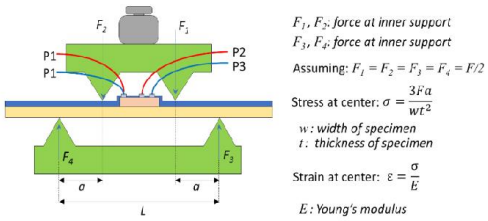


Fig. 2. Schematic diagram of tool to apply compressive strain into SiGe layer on Si substrate for piezo resistivity measurement. Current is supplied between P1 and P2 (also shown in Fig. 1(a)) and voltage between P1 and P3 is measured for resistance measurement.

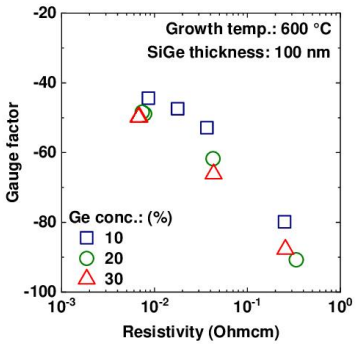


Fig. 3. GF of SiGe as function of resistivity. Ge contents are 10, 20 and 30%.

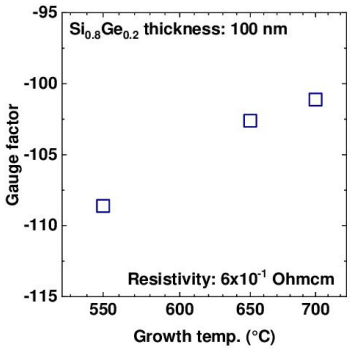


Fig. 4. GF of SiGe as function of resistivity. Ge concentration is 20%. Resistivity of the SiGe is 6×10^{-1} Ωcm.

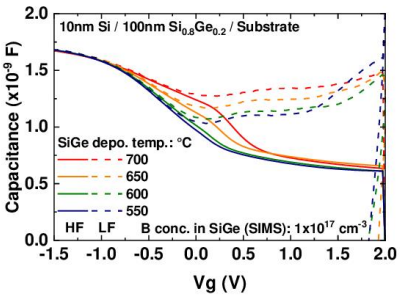


Fig. 5. C-V characteristics of SiGe with 20% Ge content. The SiGe growth temperature is varied from 550°C to 700°C. High frequency (HF) and low frequency (LF) C-V characteristics are measured using 100kHz and calculated from gate displacement current at dVg/dt = 40mV/s, respectively.

Figure 1