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Heteroepitaxy of group IV materials for future device application

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Heteroepitxy of group IV materials (Si, SiGe, and Ge) has great potential for boosting Si-based novel device performance because of the possibility for strain, band gap/Fermi-level engineering, and applying emerging artificial materials such as a superlattice (SL) and nanodots. In order to control group IV heteroepitaxy processes, strain, interface, and surface energies are very essential parameters. They affect dislocation formation, interface steepness, reflow of deposited layers, and also surface reaction itself during the growth. Therefore, process control and crystallinity management of SiGe heteroepitaxy are difficult especially in the case of high Ge concentrations. In this paper, we review our results of abrupt SiGe/Si interface fabrication by introducing C-delta layers and the influence of strain on the surface reaction of SiGe. Three-dimensional self-ordered SiGe and Ge nanodot fabrication by proactively using strain and surface energies by depositing SiGe/Si and Ge/SiGe SL are also reviewed.

1. Introduction

Heteroepitaxy of group IV materials is widely used for high-performance devices such as stressors for the channel of metal oxide semiconductor field effect transistors,[1–4] SiGe:C hetero bipolar transistors.[5–9] In order to use the benefits of material properties and engineered band gap offset, emerging devices e.g. Ge photodiode,[10–12] multi-quantum well (MQW) microbolometers,[13–15] MQW cascade lasers[16–20] and quantum computing devices[21–23] are also widely investigated. To realize heteroepitaxial processes in a desired manner, strain in the films near the heterointerface and beneath the growth front is a key. The strain formation is caused by the lattice mismatch between the substrate and the deposited epitaxial layer. In the case of Ge growth on Si, lattice mismatch is 4.2%.[24] During the initial stage of Ge growth on Si, Ge grows pseudomorphically on Si at first and accumulates strain at the interface and deposited Ge. The heteroepitaxial strain induces the local elastic deformation in the deposited Ge by the Stranski–Krastanov mechanism.[25] After exceeding a critical thickness, of a few nm only in the Ge/Si case, plastic relaxation occurs. The lattice mismatch is thus accommodated by inserting a high density of misfit dislocations (MD) and threading dislocations (TD).[26] In the case of SiGe growth on Si or Ge surface, the critical thickness is larger compared to that of the Ge growth on Si because of a reduced lattice mismatch.[27,28] Therefore, the strain of heteroepitaxial growth of SiGe is more important to manage because during the initial stage of SiGe growth on Si, relaxation of SiGe will not happen until reaching critical thickness, which is much thicker compared to that of Ge growth on Si.

In this paper, we review our recent results of our investigations of group IV heteroepitaxy using reduced pressure (RP) chemical vapor deposition. We summarized a method for abrupt SiGe quantum well (QW) fabrication by C-delta doping,[29] the influence of strain on the surface reaction of heteroepitaxial SiGe growth,[30] and three-dimensional (3D) aligned SiGe and Ge nanodot fabrication by proactively managing strain and surface energies.[31–36]

2. Abrupt SiGe MQW fabrication for microbolometer

In order to fabricate a high-sensitivity SiGe MQW microbolometer, a high Ge concentration QW is required to increase the temperature coefficient of resistivity (TCR), because an increased valence band offset enhances the thermal excitation of electrons. However, crystallinity degradation by MD happens if the Ge concentration becomes high. Additionally, by increasing Ge concentration, higher intermixing of Si and Ge at the interface and surface reflow are expected because of high strain near the heterointerface and beneath the growth front. Therefore, in order to fabricate SiGe MQW with high Ge content in Si, strain management between the SiGe layer and Si is essential. To realize a steep interface, lowering the process temperature of post-SiGe growth is necessary, especially for the Si capping process on the SiGe QW, which requires a higher temperature compared to the SiGe growth temperature. Here a method of abrupt SiGe profile fabrication on the Si (001) substrate by introducing a C-delta layer is presented.

Figure 1 shows the root mean square (RMS) surface roughness of a 10 nm thick $Si_{0.5}Ge_{0.5}$ layer on a Si substrate with/without C-delta layers at the interface and the $Si_{0.5}Ge_{0.5}$ surface at different post-annealing temperatures.[29] The $Si_{0.5}Ge_{0.5}$ growth and C-delta layer deposition are performed by H_2-SiH_4-GeH_4 gas mixture at 500 °C and by exposing CH_3SiH_3 at 500 °C without SiH_4 and GeH_4 injection, respectively. The targeted C-dose is below one monolayer at most. As a deposited condition, pseudomorphic growth of $Si_{0.5}Ge_{0.5}$ was confirmed by XRD for both samples with/without the C-delta layers. The RMS roughness of both samples is ~0.3 nm. In the case of the sample without C-delta layers, a drastic increase of surface roughness to ~1.3 nm is observed after post-annealing at 575 °C, while the surface roughening below 550 °C is much weaker. On the other hand, by introducing the C-delta layers at the interface and

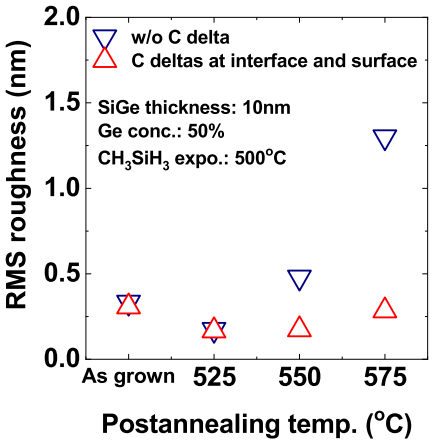

Fig. 1. (Color online) RMS roughness of 10 nm thick $Si_{0.5}Ge_{0.5}$ at different post-annealing temperatures. The post-annealing time is 1 min, ∇ shows the sample without C-delta layers and △ shows the sample with the C-delta layer at $Si_{0.5}Ge_{0.5}$/Si interface and surface.[29)]

surface, surface roughening is maintained even at 575 °C. The Reflow of SiGe is suppressed by the C-delta layers.

Next, the influence of C-delta layers on the crystallinity of 10 nm thick $Si_{0.5}Ge_{0.5}$ is discussed. Figure 2 shows cross-section transmission electron microscope (TEM) images of the 10 nm thick $Si_{0.5}Ge_{0.5}$ layers of as-deposited layers [Figs. 2(a), 2(b)], after following post-annealed layers at 575 °C [Figs. 2(c), 2(d)] and samples after Si capping at 575 °C using H_2-Si_2H_6 [Figs. 2(e), 2(f)].[29)] (a), (c), (e) show samples without C-delta layers at the $Si_{0.5}Ge_{0.5}$ and Si interface and (b), (d), (f) show samples with two C-delta layers at both the upper and lower $Si_{0.5}Ge_{0.5}$ and Si interfaces (or the $Si_{0.5}Ge_{0.5}$ surface). After the $Si_{0.5}Ge_{0.5}$ growth [Figs. 2(a), 2(b)], smooth SiGe surfaces are observed for both samples as summarized in Fig. 1. No stacking faults (SF) and MDs are observed indicating the deposited $Si_{0.5}Ge_{0.5}$ is of high crystallinity and fully strained. By post-annealing at 575 °C, strong surface roughening due to island formation is observed for the sample without C-delta layers [Fig. 2(c)]. No MDs are observed at the interface. However, SFs in the {111} plane are observed near the surface area. The surface roughening is driven by local elastic energy reduction according to the Stranski–Krastanov mechanism. The elastic energy is reduced also by injecting defects in the $Si_{0.5}Ge_{0.5}$. Therefore, Si and Ge atoms in the SiGe layer tend to move to defects, which is a region of lower elastic energy compared to other areas. On the other hand, in the case of a sample with C-delta layers [Fig. 2(d)], no surface roughening and SF formation are observed by annealing at 575 °C. The island formation by reflow of Ge and Si atoms is suppressed by the C-delta layers. The TEM image confirms that the C-delta layer at the surface is maintaining not only the surface roughness but also the

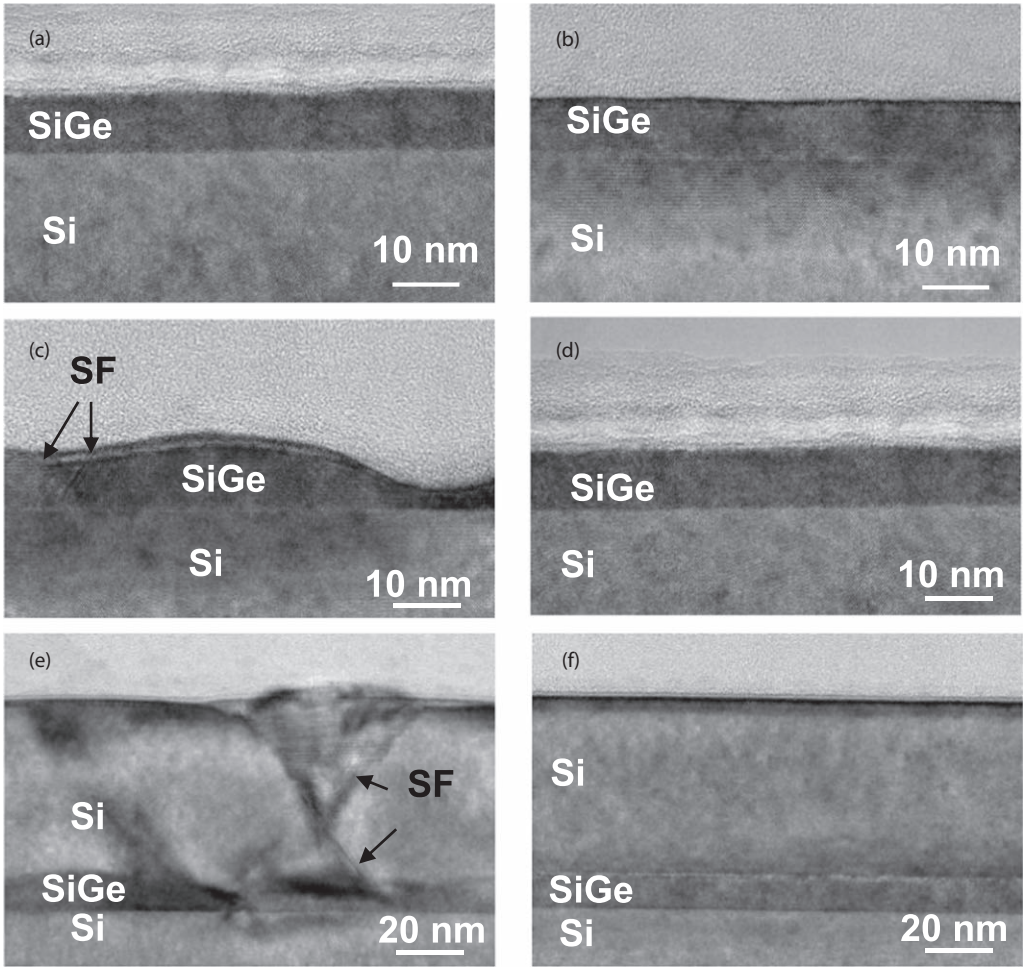

Fig. 2. (Color online) Cross-section TEM images of 10 nm thick $Si_{0.5}Ge_{0.5}$ samples (a), (b) without post-annealing, (c), (d) after post-annealing for 1 min at 575 °C samples and (e), (f) after Si cap growth at 575 °C using H_2-Si_2H_6. (a), (c), (e) show samples without C-delta layers at SiGe and Si interface and (b), (d), (f) show samples with two C-delta layers at $Si_{0.5}Ge_{0.5}$ and Si interfaces (or $Si_{0.5}Ge_{0.5}$ surface).[29)]

good crystallinity of the $Si_{0.5}Ge_{0.5}$ layer. By depositing a Si cap on the $Si_{0.5}Ge_{0.5}$ surface without a C-delta layer at 575 °C [Fig. 2(e)], a defective Si with a rough surface is grown. SFs and micro twins are visible in the Si cap layer. Non-uniform strain contrast in the Si layer is also visible due to defects. On the other hand, by introducing C-delta layers, a defect-free Si layer with a smooth surface can be grown at 575 °C [Fig. 2(f)]. The C-delta layer on the $Si_{0.5}Ge_{0.5}$ surface does not disturb the crystal quality of Si on the $Si_{0.5}Ge_{0.5}$ at 575 °C.

In Figs. 3(a), 3(b), Ge profiles of 10 nm thick $Si_{0.5}Ge_{0.5}$ layers with 50 nm thick Si cap layer grown at different Si growth temperatures are shown.[29] The $Si_{0.5}Ge_{0.5}$ and the Si cap growths are performed using H_2-SiH_4-GeH_4 at 500 °C in RP and H_2-Si_2H_6 at 500 °C to 575 °C in RP, respectively. Growth rates of the Si cap depositions at 500 °C, 525 °C, 550 °C and 575 °C are 0.3 nm min^{-1}., 0.6 nm min^{-1}, 1.6 nm min^{-1} and 2.9 nm min^{-1}, respectively. The profile is simulated by an XRD rocking curve of (004) diffraction. In the case of the sample without C-delta layers after Si deposition at 500 °C without temperature ramping up from the $Si_{0.5}Ge_{0.5}$ growth [Fig. 3(a)], no diffusion of Ge is observed. However, smeared SiGe profiles are observed after depositing Si at 525 °C and 550 °C. At 525 °C and 550 °C, no surface roughening of the SiGe is evidenced as shown in Fig. 1. That means the smeared Ge profiles are not caused by interface roughening but by interdiffusion of Si and Ge at the interface due to raising the temperature. On the other hand, by introducing C-delta layers at both interfaces, a steep Ge profile is observed even after Si growth at 575 °C. The interdiffusion at the SiGe layer is suppressed by the C-delta layer. This diffusion suppression by C-delta layers is also detected by SIMS. This phenomenon is reported for the $Si_{0.45}Ge_{0.55}$/Si interface at 650 °C in Ref. 37 too. The SiGe interdiffusion process is reported according to a vacancy mechanism.[38] Possible assumption of the interdiffusion suppression effect is vacancy trapping by C at the interface.

In Figs. 4(a), 4(b), the XRD (004) rocking curve of ×3 MQW of 10 nm and 6 nm thick $Si_{0.5}Ge_{0.5}$/50 nm thick Si superlattice without/with C-delta layers at each interface are shown, respectively. For both cases, SiGe peaks with thickness fringes and shallow periodic subpeaks from the SiGe/Si superlattice are observed. That means both SiGe MQW layer stacks are of high crystal quality and pseudomorphically grown on the Si substrate. In the case of the sample with 10 nm thick $Si_{0.5}Ge_{0.5}$ MQW [Fig. 4(a)], the peak position of the SiGe and periodicity of the SL oscillation peaks are not changed by introducing C-delta layers, indicating Ge concentration and thickness of the SiGe QWs as well as the thickness of the Si spacers are not influenced by the C-delta layers. However, in the case of the sample without C-delta layers the amplitude of the oscillation of the SL fringes is weaker compared to the sample with C-delta layers, indicating that the steepness of the interface is lower. Evidence of lower interface steepness of the sample without C-delta layers is also observed by reducing $Si_{0.5}Ge_{0.5}$ MQW thickness from 10 nm to 6 nm [Fig. 4(b)]. However, by reducing the SiGe thickness from 10 nm to 6 nm, Ge concentration is reduced to 42% if the C-delta layers are not introduced at each interface. This phenomenon is not observed for the MQW wafer with 10 nm thick $Si_{0.5}Ge_{0.5}$ [as shown in Fig. 4(a)] and also 8 nm thick $Si_{0.5}Ge_{0.5}$. On the other hand, by introducing C-delta layers at each interface, the Ge concentration of the 6 nm thick $Si_{0.5}Ge_{0.5}$ MQW is maintained. In the case of 6 nm thick $Si_{0.5}Ge_{0.5}$ MQW without C-delta layers, the $Si_{0.5}Ge_{0.5}$ peak concentration seems to be reduced by interdiffusion at the interfaces, because the plateau of $Si_{0.5}Ge_{0.5}$ QW is not thick enough.

In Fig. 5, TCR of 10 nm, 8 nm, and 6 nm thick $Si_{0.5}Ge_{0.5}$ MQW samples without C-delta layers and 6 nm thick $Si_{0.5}Ge_{0.5}$ MQW samples with C-delta layers are shown. In the case of a 10 nm thick $Si_{0.5}Ge_{0.5}$ MQW sample, a TCR of $\sim -5.5\%$/K is observed. By reducing the $Si_{0.5}Ge_{0.5}$ MQW thickness to 8 nm, only a weak influence of the thickness reduction on TCR is observed. However, by reducing the $Si_{0.5}Ge_{0.5}$ MQW thickness further to 6 nm, a significant reduction of TCR is observed. The reduced TCR is indicating the reduction of Ge concentration in the 6 nm thick MQW. By introducing C-delta layers at each interface, the TCR reduction is suppressed due to maintained Ge concentration by diffusion suppression.[39]

3. Influence of strain on SiGe growth

In this section, the influence of strain on SiGe growth is discussed. In order to investigate the influence of strain on SiGe and Ge growth, 10 cycles of Ge and $Si_{0.2}Ge_{0.8}$ SL are deposited at 500 °C using H_2-GeH_4 and H_2-SiH_4-GeH_4 system on SiGe and Ge virtual substrate (VS) with 85%,

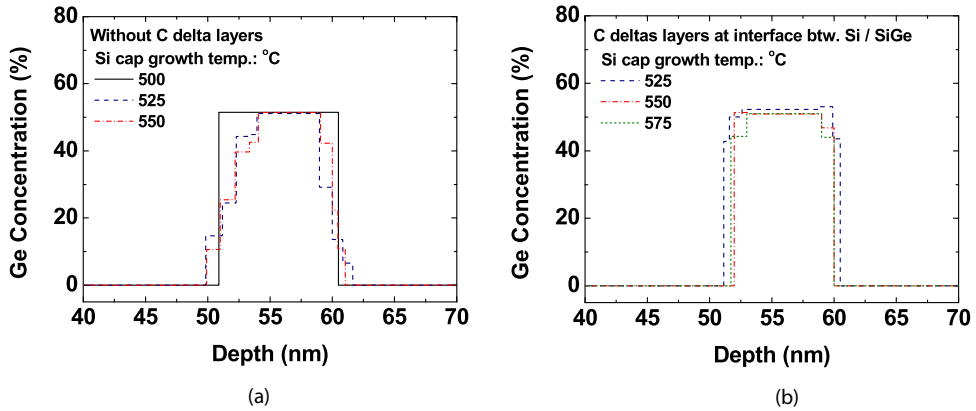

Fig. 3. (Color online) Ge profiles of $Si_{0.5}Ge_{0.5}$ with Si cap layer deposited at different Si growth temperatures. Growth conditions of the $Si_{0.5}Ge_{0.5}$ and the Si cap are H_2-SiH_4-GeH_4 at 500 °C in RP and H_2-Si_2H_6 at 500 °C to 575 °C in RP, respectively. The Ge profile is obtained by simulation of XRD rocking curves of (004) diffraction. (a) shows a sample without C-delta layers and (b) shows a sample with C-delta layers at the interfaces between $Si_{0.5}Ge_{0.5}$ and Si.[29]

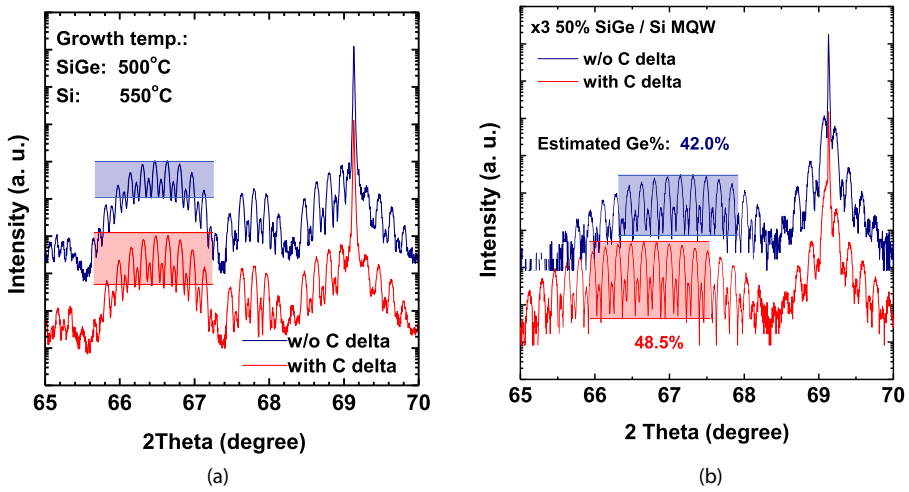

Fig. 4. (Color online) XRD rocking curves of (004) diffraction of ×3 MQW superlattice with (a) 10 nm thick SiGe and 50 nm Si spacers with and without C-delta layers at each interface and (b) 6 nm thick SiGe and 50 nm Si spacers with and without C-delta layers at each interface. The target Ge concentration of the SiGe MQW is 50%.

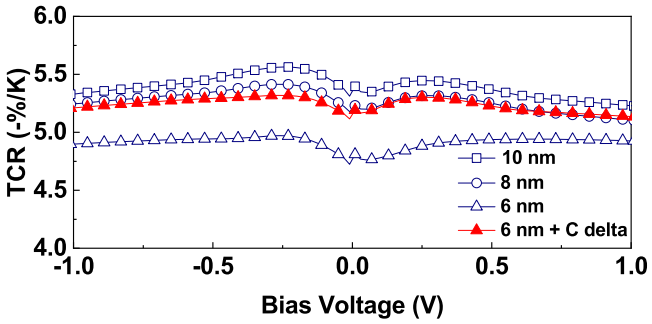

Fig. 5. (Color online) TCR versus bias voltage measured on ×3 MQW $Si_{0.5}Ge_{0.5}$/Si-based intrinsic thermistor devices with different $Si_{0.5}Ge_{0.5}$ QW thickness. The thickness of Si spacers is 50 nm and the target Ge concentration in SiGe QW is 50% for all cases. For the sample plotted with ▲, C-delta layers are inserted at all interfaces between Si and SiGe layers.[15)]

90%, 95% and 100% Ge content. The VS are fabricated by depositing heteroepitaxial SiGe or Ge on Si substrate with reverse graded buffer approach[40)] using cyclic annealing process[30,41,42)] to realize full relaxation and low dislocation density. The target thickness of $Si_{0.2}Ge_{0.8}$ and Ge in the SL layer is 15 nm. Fixed process conditions (SiH_4 and GeH_4 partial pressures and deposition times) are used for $Si_{0.2}Ge_{0.8}$ and Ge layers for each SiGe VS.

In Figs. 6(a), 6(b), $Si_{0.2}Ge_{0.8}$ and Ge thicknesses in the $Si_{0.2}Ge_{0.8}$/Ge SL deposited on VSs with 85%, 90%, 95% and 100% Ge content are shown.[30)] In the case of the $Si_{0.2}Ge_{0.8}$ layer [Fig. 6(a)], the thickness on a $Si_{0.15}Ge_{0.85}$ VS is ∼17 nm. The $Si_{0.2}Ge_{0.8}$ layer thickness increases with increasing the Ge concentration of VS from 85% to 100%. This result indicates that the growth rate of the $Si_{0.2}Ge_{0.8}$ layer is increased by increasing tensile strain. On the other hand, in the case of the Ge layer in the SL [Fig. 6(b)], the Ge layer thickness grown on the VS with 85% Ge content is ∼14.5 nm, and the Ge thicknesses grown on the VS with 90%, 95%, and 100% Ge content are ∼14.0 to ∼14.2 nm. The difference in the thickness seems to be within measurement error bars and no clear trend is observed, indicating weak or almost no influence of the Ge concentration of the VS on the growth rate of the Ge layer.

In Fig. 7, Si concentration in the SiGe layer in the SL was measured by TEM-energy dispersive X-ray spectroscopy (EDX), and the intensity ratio of Si 2p and Ge 3d was measured by X-ray photoelectron spectroscopy (XPS) with Al Kα (1486.6 eV) X-ray source are shown. Because the escape depth of photoelectron by XPS measurement is below 10 nm and the top SiGe layer thickness is 17 nm to 18 nm (as shown in Fig. 6(a), photoelectrons from the top SiGe layer are detected only, and the photoelectron intensity from the Ge layer underneath is negligible. By the TEM-EDX analysis, Si concentration in the SiGe layer in MQW on $Si_{0.15}Ge_{0.85}$ VS is ∼18%, and tends to increase slightly by increasing the Ge concentration in the VS. The increase is very small, but the increase in Si concentration is also supported by XPS analysis. Therefore, it seems that the increase of the Si incorporation with increasing Ge concentration in the VS (i.e. increasing tensile strain in the growing $Si_{0.2}Ge_{0.8}$ layer) is reliable. Based on the results of Figs. 6(a), 6(b), and 7, a possible explanation for the slight increase in growth rate for the $Si_{0.2}Ge_{0.8}$ layer [Fig. 6(a)] but not for the Ge layer [Fig. 6(b)] could be that there is an increased reaction of SiH_4 on higher tensile strained $Si_{0.2}Ge_{0.8}$ due to higher surface energy. At 500 °C, the SiH_4 reaction is in the surface reaction limited regime, but the GeH_4 reaction is in the mass transport limited regime. Therefore, the reaction of the SiH_4 is increased by higher strain, but the reaction of the GeH_4 is less sensitive to the surface energy of the Ge surface because the reaction is mainly limited by mass transport.

In Fig. 8, cross-section STEM [Figs. 8(a), 8(b)] and EDX [Figs. 8(c), 8(d)] of 10 cycles of $Si_{0.2}Ge_{0.8}$/Ge MQW are shown. Figures 8(a) and 8(c) depict samples with MQW grown on Ge VS and Figs. 8(b) and 8(d) with MQW grown on $Si_{0.15}Ge_{0.85}$ VS. For both Figs. 8(a), 8(b), no defects are observed in STEM images, indicating good crystal quality of the MQW. In both EDX images [Figs. 8(c), 8(d)], steep profiles are observed at the interface of Ge on the $Si_{0.2}Ge_{0.8}$

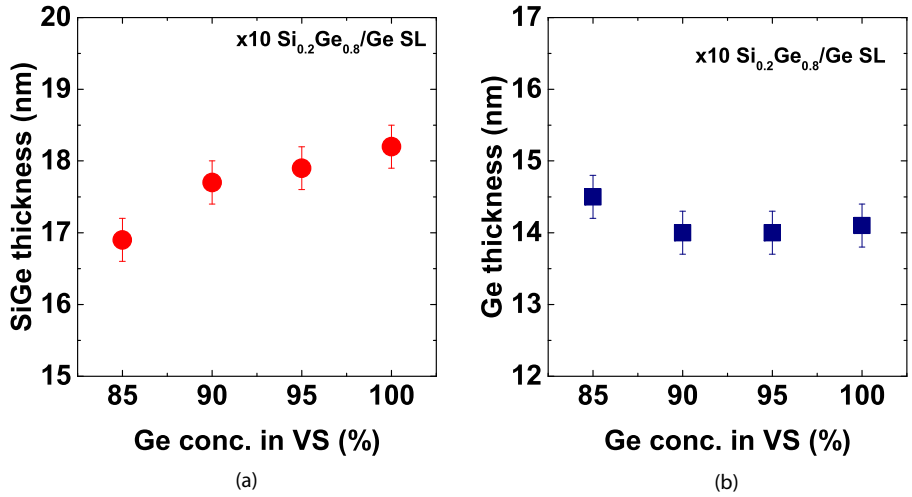

Fig. 6. (Color online) Thicknesses of (a) $Si_{0.2}Ge_{0.8}$ and (b) Ge of MQW deposited on SiGe VS with different Ge concentrations. Thicknesses of the $Si_{0.2}Ge_{0.8}$ and Ge layers are measured by cross-section TEM.[30)]

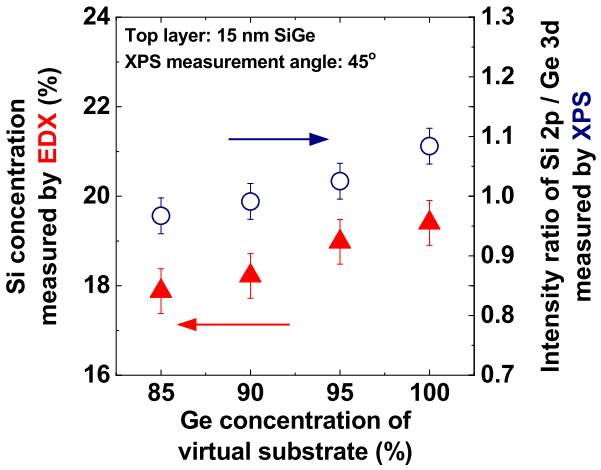

Fig. 7. (Color online) Si concentration measured by EDX and intensity ratio of Si 2*p* and Ge 3*d* of 10 cycles of SiGe/Ge SL grown on Ge or SiGe VS with various Ge content. The thicknesses of the SiGe and Ge layers are 15 nm and the top layer of the SiGe SL is SiGe.[30)]

layer, however, the interface of $Si_{0.2}Ge_{0.8}$ on Ge is blurred. One of the main reasons for the smeared interface could be the surface segregation of Ge atoms during $Si_{0.2}Ge_{0.8}$ growth,[33)] due to the lower surface energy density of Ge as compared to Si.

Table I. Summary of the steepness of interface between SiGe and Ge of MQW measured by TEM.[30)]

Virtual substrate	Interface thickness: Ge on SiGe (nm)	Interface thickness: SiGe on Ge (nm)
Ge	1.8	7.4
$Si_{0.15}Ge_{0.85}$	1.5	6.4

The estimated interface steepness of Si and $Si_{0.2}Ge_{0.8}$ measured by TEM is summarized in Table I.[30)] Because the depth resolution of the TEM image is influenced by the TEM lamella thickness, the thickness (T) range relative to the mean free path of electrons (lambda) is selected between 0.35 T/lambda and 0.5 T/lambda. In this thickness range, constant interface resolution is obtained.[30)] In the case of Ge growth on $Si_{0.2}Ge_{0.8}$, only a slight increase of the interface steepness (1.5 nm to 1.8 nm) is observed by increasing the Ge concentration of the VS from 85% to 100%. On the other hand, in the case of $Si_{0.2}Ge_{0.8}$ growth on Ge, a relatively large change (6.4 nm to 7.4 nm) of the interface steepness is observed by changing $Si_{0.15}Ge_{0.85}$ VS to Ge VS. A possible reason could be that higher tensile strain in the $Si_{0.2}Ge_{0.8}$ layer on Ge VS causes higher Ge segregation due to increased bulk energy in the $Si_{0.2}Ge_{0.8}$ layer.

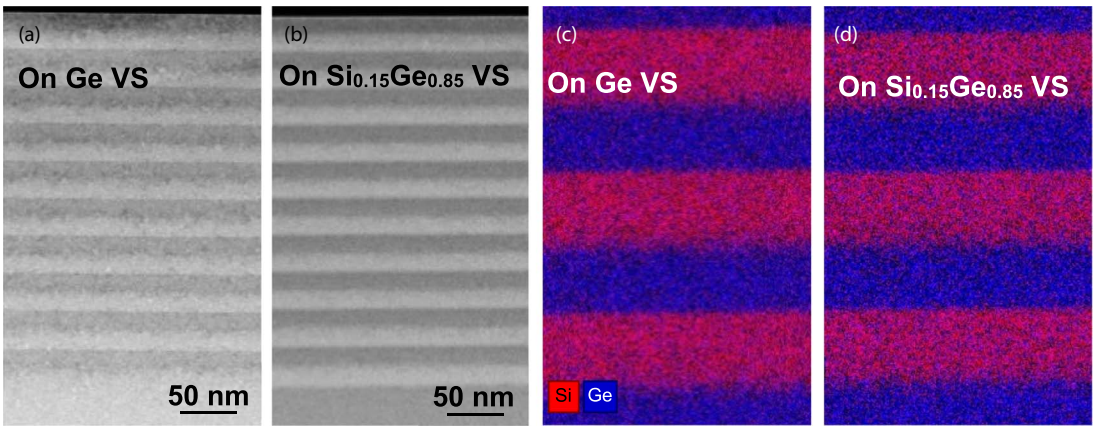

Fig. 8. (Color online) (a) Cross-section HAADF STEM images of 10 cycles of SiGe/Ge MQW deposited on (a) Ge VS and (b) $Si_{0.15}Ge_{0.85}$. (c) and (d) show Si and Ge distribution EDX mapping of the SiGe/Ge MQW on Ge VS and $Si_{0.15}Ge_{0.85}$ VS, respectively.[30)]

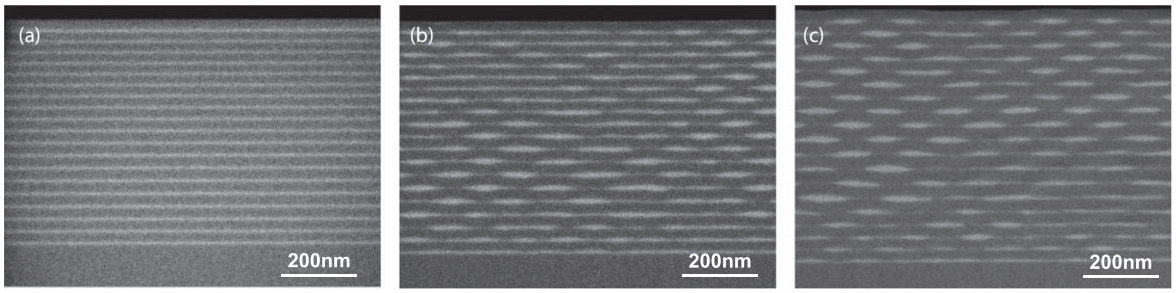

Fig. 9. (Color online) Cross-section SEM images of 20 cycles of SiGe/Si superlattice structures. Ge concentrations are (a) 25%, (b) 30%, and (c) 35%. Target SiGe and Si spacer thicknesses are 5 nm and 25 nm, respectively. H_2-SiH_4-GeH_4 in RP and H_2-SiH_4 in RP are used for SiGe and Si growth, respectively. SiGe and Si growth temperatures are 550 °C and 700 °C, respectively.[31)]

4. Self-ordered SiGe and Ge nanodot fabrication

In this section, vertically and laterally self-aligned SiGe and Ge nanodot fabrication by superlattice (SL) deposition is presented by engineering strain and surface energy. By depositing 5 nm thick $Si_{0.75}Ge_{0.25}$/25 nm Si SL at 550 °C for SiGe and 700 °C for Si, SL with flat $Si_{0.75}Ge_{0.25}$ layers are deposited [Fig. 9(a)].[31)] By increasing the Ge concentration of the SiGe from 25% to 30% and 35%, staggered aligned SiGe nanodots are formed [Figs. 9(b), 9(c)].[31)] For the both 30% and 35% samples, imperfect nanodot formation is observed for the first SiGe layers. The regular alignment becomes more pronounced after several SiGe layer depositions. A possible reason for the regular alignment of the SiGe nanodot might be related to anisotropic strain distribution around the SiGe nanodot, because of the presence of a monotonically decreased strain field toward ⟨010⟩ direction.[43)] Even if the Ge concentration of the SiGe is 30%, the staggered aligned SiGe nanodot formation was not observed if the Si spacer growth temperature is reduced from 700 °C to 675 °C. These results indicate that the driving force of surface migration for the nanodot formation for $Si_{0.7}Ge_{0.3}$ is not enough at 675 °C.

Next, the influence of process conditions on the vertical alignment of the SiGe nanodot is discussed. In Fig. 10, a cross-section SEM image of 20 cycles of SiGe layer stacks is shown. SiH_4 is used as a precursor of Si spacer for the first 10 cycles and SiH_2Cl_2 is used for the following 10 cycles. Irregular nanodot formation is observed for the first several layers due to random nanodot formation, however afterward, regularly ordered staggered aligned SiGe nanodot formation is observed by using SiH_4. By using SiH_4, a mesa structure is formed on buried Ge nanodot, resulting in a checkerboard structure.[32)] Preferred position for the next SiGe nanodots is at the concave region to reduce surface energy, resulting in staggered alignment. By switching the precursor from SiH_4 to SiH_2Cl_2, a vertical alignment of SiGe nanodot formation is observed because the surface of each Si spacer becomes flattened. In this case, the driving force of the SiGe nanodot formation is a local tensile strain of Si on the buried SiGe nanodot.[33,34)]

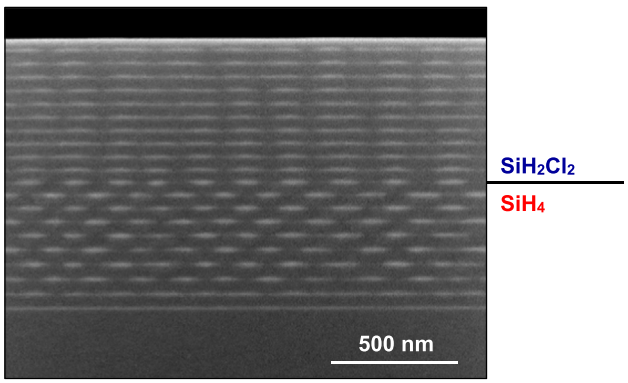

Fig. 10. (Color online) Cross-section SEM image of SiGe nanodot layer stack by SiGe/Si SL deposition. H_2-SiH_4 gas mixture is used for Si spacer deposition for the first 10 layers and H_2-SiH_2Cl_2 for the last 10 layers. The temperature for Si growth is 700 °C for both cases.[32)]

In the case of 3D-ordered Ge nanodot formation by Ge/SiGe SL, key parameters for vertical and staggered alignment are also non-uniform local strain and surface roughness of the SiGe spacer.[35,36)] By depositing the SiGe spacer at 550 °C, vertical alignment of Ge nanodot is obtained because of smooth SiGe spacer surface formation. By reducing SiGe growth temperature to 500 °C or 475 °C, staggered alignment is realized [Fig. 11(a)] due to the checkerboard SiGe spacer surface formation. Laterally ordered periodic structure is also shown in Fig. 11(b).

5. Conclusions

Our results of high-quality Si/SiGe/Ge heteroepitaxy fabrications are reviewed. In the case of fully strained SiGe QW deposition with high Ge content on Si, the Si cap process temperature is limited to avoid reflow and degradation of the crystal quality of the SiGe QW. By introducing C-delta layers at the interface of the Si cap, the crystallinity degradation and surface reflow are suppressed. The C-delta layer maintains interdiffusion of Si and Ge resulting in a steep Si and SiGe interface. In the case of SiGe growth, a higher growth rate and Si incorporation are observed with increasing tensile strain, however, the Ge growth rate is not affected by strain because the Si reaction is surface reaction limited but the Ge reaction is mass transport limited. Control of self-ordering of staggered and vertical alignment of SiGe and Ge nanodot formation is demonstrated by SiGe/Si and Ge/SiGe SL deposition. The driving force of the dot-on-dot alignment and staggered alignment is the elastic relaxation of strain energy and surface energy reduction.

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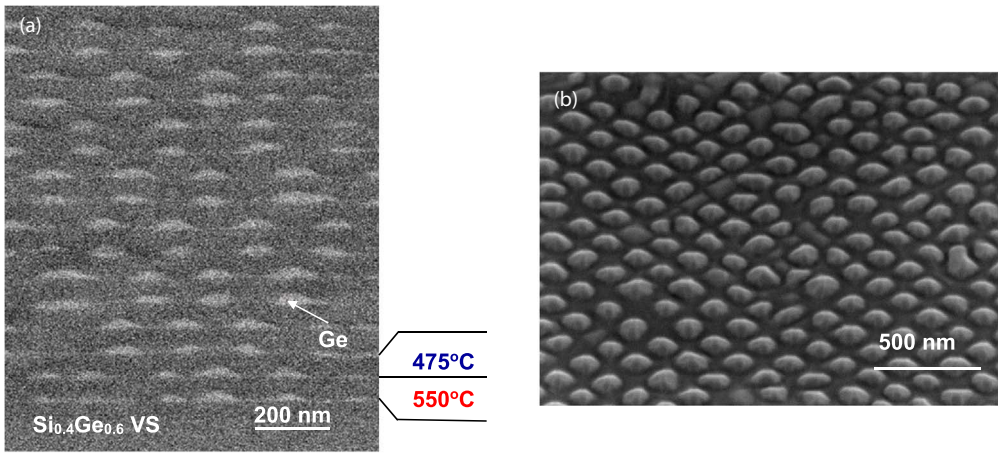

Fig. 11. (Color online) (a) Cross-section and (b) angle view (40° from the surface) SEM images of Ge nanodot layer stack deposited on $Si_{0.4}Ge_{0.6}$ VS by Ge/SiGe SL fabrication. Growth temperatures and Ge concentrations in even and odd SiGe spacer from the $Si_{0.4}Ge_{0.6}$ VS is 550 °C, 52% and 475 °C, 49%, respectively. The effective Ge thickness of the Ge nanodot layers is targeted at 12.5 nm. The growth temperature of the Ge nanodot layers is 550 °C.

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