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A Particle Detector Based on Pulse Stretching Inverter Chain

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***Abstract*—Monitoring of energetic particles responsible for the soft errors is an important requirement in the design of fault-tolerant systems for space missions. In this paper, the use of a custom-sized CMOS pulse stretching inverter chain as a particle detector is studied. The proposed detector allows for measuring the particle flux in terms of the count rate of induced Single Event Transients (SETs). In contrast to the conventional SRAM-based detectors, the proposed solution is potentially more sensitive to particle strikes, requires simpler processing logic and is more immune to multiple errors and error accumulation. The concept has been evaluated with SPICE simulations for the IHP's 130 nm CMOS technology. The target applications are the self-adaptive multi-processor systems, where the particle detector can be used to dynamically trigger the fault-tolerant mechanisms.**

Keywords—particle detector, soft error, single event transient, pulse stretching inverter chain

I. INTRODUCTION

The long-term space missions require high performance integrated circuits capable of processing huge amount of data with low power consumption and high robustness to ionizing radiation. Such requirements are often conflicting and hence impose the need for design trade-offs. A widely accepted solution is in the use of adaptive multi- or many-core architectures [1 – 3], where the cores are dynamically reconfigured according to the application requirements. For example, by varying the number of cores involved in parallel processing and powering off the unused ones, the optimal performance with minimal power overhead can be achieved. In a similar manner, the cost-effective radiation hardening can be accomplished by applying the dynamic fault tolerance [3], e.g. by configuring the cores into an N-modular redundant architecture under the critical radiation conditions (i.e. when the radiation exposure is high enough to affect the system's operation). The use of dynamic fault tolerance can be justified by the fact that the radiation exposure in space environment is not constant, and only certain events (e.g. solar winds and flares) can lead to high radiation levels lasting for hours or days [4].

In order to detect the critical radiation exposure and subsequently apply the fault tolerant mechanisms, the on-board real-time radiation monitoring is needed. For integrated circuits designed in nanoscale CMOS technologies, the most critical radiation-induced effects in space environment are the soft errors. Two possible scenarios for soft error occurrence are: (i) when an energetic particle passes through a sequential element and deposits sufficient charge to flip its logic state, or (ii) when an energetic particle hits a combinational gate and induces a voltage glitch, i.e. a Single Event Transient (SET), which is then latched in a sequential element. One of the main parameters affecting the soft error rate (SER) of digital systems is the particle flux. Namely, the SER increases linearly with the increase of particle flux [5]. In that regard, continuous monitoring of particle flux during a space mission is essential for identification of critical radiation conditions. Moreover, the radiation monitors should detect directly the incident particles rather than the resulting soft errors in the target system.

Various solutions for detecting the particles capable of causing the soft errors have been proposed. The widely used particle detectors such as PIN diodes [6] and pixel detectors [7] can measure the radiation exposure very accurately. However, the use of these detectors is often too costly because different technologies have to be combined and complex mixed-signal processing is required. The alternative solutions such as the integration of current detectors [8] or acoustic detectors [9] in the target system have been proposed, but these solutions are prone to false alarms, because the noise in the system (e.g. substrate noise) could be interpreted as a soft error. On the other hand, the use of commercial or custom-designed SRAMs as particle detectors, implemented either as stand-alone chips or integrated within the target chip, has proven to be a reliable and cost-effective solution [10 – 15].

The SRAM-based monitors measure the particle flux by counting the bit-flips in SRAM cells. However, this approach has also some important drawbacks. In the stand-alone implementation [10 – 13], the area overhead due to the error detection and correction logic may be large. In addition, the existing error detection and correction techniques suffer from the limitation in the number of detectable and correctable errors, which may lead to the error accumulation as a result of multiple upsets. On the other hand, if a data-storage SRAM within the target chip is used as a particle detector [14, 15], its sensitive area will be constrained by the application requirements, potentially resulting in lower sensitivity. Another issue with the use of data-storage SRAMs as particle detectors is that the sensitivity of individual SRAM cells will depend on the stored logic value.

In this work, a particle detector based on the custom-sized inverter chains with the pulse stretching feature is presented. By counting the SETs induced in the chain, the particle flux can be determined. The pulse stretching inverter chains have been used for characterization of SET pulse width in standard combinational cells [16, 17]. However, to the best of our knowledge, the use of pulse stretching inverter chains as particle detectors has not been investigated. We have shown through the circuit simulations that the sensitivity of a pulse stretching inverter chain to

particle strikes is higher than that of standard library cells and the 6T SRAM cell. Additional advantages are simple processing logic and hence lower cost of implementation, as well as the immunity to multiple errors and error accumulation.

The rest of the paper is organized as follows. Section II describes the operation of the pulse stretching inverter chain as a particle detector. In Section III, the characterization results are discussed. The design of the overall monitor and the typical application scenario are presented in Section IV.

II. Custom-sized Pulse Stretching Inverter Chain as a Particle Detector

The elementary pulse stretcher in CMOS technology can be realized with two cascaded custom-sized inverters as shown in Figure 1. The transistor sizes should be chosen such that in one inverter the channel width of PMOS transistor (W_{PMOS}) is smaller than that of NMOS transistor (W_{NMOS}), while in the other inverter the channel width of NMOS transistor is smaller than that of PMOS transistor. This ensures that an input pulse will be stretched as it propagates, whereby the pulse stretching (difference between input and output pulse widths) is defined by the PMOS-to-NMOS ratio. In general, for the fixed channel length L, the transistor sizes for a two-inverter pulse stretcher can be defined with the following relations [17],

$$W_{NMOS1} = W_{PMOS2} \quad (1)$$
$$W_{PMOS1} = W_{NMOS2} \quad (2)$$
$$W_{NMOS1} > W_{PMOS1} \quad (3)$$
$$W_{PMOS2} > W_{NMOS2} \quad (4)$$

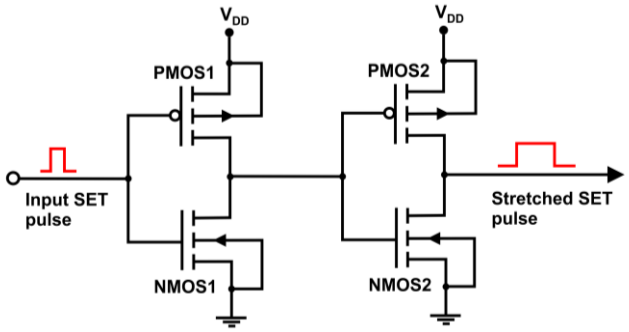

Figure 1: Two-inverter pulse stretcher

As the CMOS circuits are inherently sensitive to SETs, the particle strike on a sensitive (off-state) transistor in the pulse stretcher may result in an SET pulse which will be stretched as it propagates. In other words, if the pulse stretcher can achieve sufficient pulse stretching, even very short SET pulses caused by the low-energy particles may be observable at the output. This property qualifies the pulse stretcher depicted in Figure 1 as a promising particle detector. However, to act as a particle detector in fault tolerant applications, the pulse stretcher must satisfy the following requirements: (i) the sensitive area should be as large as possible to increase the probability of particle strikes, (ii) the sensitivity of individual inverters to particle strikes should be higher than that of standard cells used in the design of the target system, (iii) the inverters should have the same or similar sensitivity, i.e. the same or similar critical charge (or Linear Energy Transfer Threshold, LET_{TH}), and (iv) the induced SET pulse should be wide enough so that it can be detected and processed by the subsequent processing logic.

By setting a fixed logic level at the input of pulse stretcher, one transistor in each inverter will always be in the off-state and thus will be sensitive to particle strikes. Following the relations (1) – (4), the input level can be set to logic 0. This means that the off-state transistors will be NMOS1 and PMOS2, while the on-state transistors will be PMOS1 and NMOS2. By increasing the size of the off-state transistors, according to relations (3) and (4), the probability of SET generation will be increased. On the other hand, the on-state transistors act as restoring elements, providing the current to compensate the induced charge. As the drive current of restoring transistors is proportional to their W/L ratio, the smaller channel width results in higher SET sensitivity of the off-state transistors. In addition, the channel length of the restoring transistors may be also increased to further enhance the SET sensitivity. Therefore, applying these guidelines for sizing the pulse stretcher in Figure 1, the requirements (ii) and (iii) mentioned above can be satisfied.

To increase the sensitive area of the pulse stretcher, and thus satisfy the requirement (i) given above, a chain of cascaded two-inverter stretchers should be formed. An even number of inverters per chain is required to ensure the same polarity of the SET pulse at the output of the chain regardless of the strike location. Two main configurations are possible. First approach is to use a long chain of cascaded pulse stretching inverters. The alternative is to use short inverter chains connected with an OR-tree to obtain a single output. In both cases, when a particle hits any inverter, the resulting SET will propagate to the output which is fed to the processing logic.

Regarding the aforementioned requirement (iv), it must be ensured that for any deposited charge exceeding the critical charge (or LET_{TH}), the SET pulse width at the output of the chain is sufficient to trigger the subsequent processing logic. To achieve this, both the sizing of each inverter and the number of inverters in the chain must be considered. In general, the width of the SET pulse at the output of the inverter chain should be at least twice the propagation delay of the subsequent logic gates in the processing unit. The width of several hundred ps can be considered as the minimum required width.

III. Characterization of Proposed Particle Detector

To evaluate the performance of the pulse stretching inverter chain as a particle detector, extensive simulations with Cadence Spectre have been conducted. As a proof of concept, the IHP's 130 nm BiCMOS technology has been used. For simulation of SETs, the current injection approach with the bias-dependent current model [18], implemented as a Verilog-A module, has been applied. The LET_{TH} was used as a measure of SET sensitivity, and it was determined as the minimum LET causing the change of the output logic level. The timing parameters of the current pulse were: rise time = 10 ps and fall time = 100 ps. In all simulations the nominal supply voltage (1.2 V) was used.

For the purpose of comparison with the proposed detector, the LET_{TH} of the basic standard cells and the 6T SRAM cell was determined. The current pulse was injected at the output of each cell and the results are given in Table 1. For combinational cells, only the minimum LET_{TH} values and the corresponding input levels are given. It can be noticed that the 6T SRAM cell has higher sensitivity than all analyzed standard cells.

Table 1: LET_{TH} for different cells in 130 nm technology

Cell	LET_{TH} ($MeVcm^2mg^{-1}$)
6T SRAM (stored 0 / stored 1)	0.28 / 0.2
D flip-flop	0.52
INV	0.42 (for input = 0)
NAND	0.41 (for input = 01)
AND	0.42 (for input = 11)
NOR	0.27 (for input = 00)
OR	0.41 (for input = 11)
XOR	0.27 (for input = 01)
XNOR	0.29 (for input = 01)

Using the results in Table 1 as a reference, the dependence of LET_{TH} on transistor sizing of the two-inverter pulse stretcher (Figure 1) was analyzed, with the aim to determine the sizes which provide the highest possible SET sensitivity. The current was injected successively at the output of each inverter. To maintain realistic load conditions, the same pulse stretcher was connected to the output of the analyzed pulse stretcher. In Figure 2 are illustrated the obtained results.

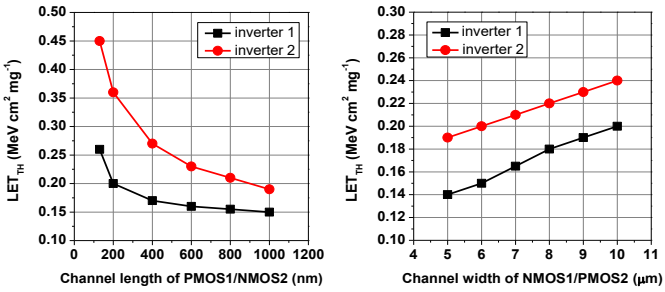

Figure 2: Dependence of LET_{TH} on the channel length of on-state transistors PMOS1 and NMOS2 (left) and the channel width of off-state transistors NMOS1 and PMOS2 (right) in a two-inverter pulse stretcher

As the SET sensitivity decreases with the increase of the channel width of on-state transistors, the minimum possible channel width of 150 nm for the on-state transistors was chosen. Then, their channel length was varied from 130 nm to 1 µm. By increasing the channel length of the on-state transistors, the LET_{TH} of both inverters is reduced, i.e. their SET sensitivity is increased. It can be seen that with the channel length of 1 µm for the on-state transistors, the LET_{TH} values for both inverters in the pulse stretcher were lower than for all cells analyzed in Table 1. On the other hand, when the off-state transistors have the channel length of 130 nm, decreasing their channel width leads to higher SET sensitivity. For instance, with the channel width of 5 or 6 µm for both off-state transistors, the inverters in the pulse stretcher had lower LET_{TH} than all cells in Table 1. Based on the obtained simulation results, the optimum sizes for the two-inverter pulse stretcher are: W/L =150nm/1µm (for PMOS1 and NMOS2) and W/L = 6µm/130nm (for NMOS1 and PMOS2). It is important to note that the channel width of 6 µm for the off-state transistors, rather than 5 µm, was chosen in order to increase the sensitive area.

Using the aforementioned transistor sizes, the impact of the number of cascaded two-inverter stretchers on the LET_{TH} and the output SET pulse width was evaluated. The results are presented in Figures 3 and 4. As can be seen in Figure 3, for a pulse stretcher with 20 inverters, the LET_{TH} values of individual inverters were almost constant, as desired. The SET pulse width increased as the target inverter was at larger distance from the output, due to the stretching feature. The minimum SET pulse width of 320 ps was obtained when the current was injected in the last inverter. This pulse width is sufficient to propagate further to the processing logic, since the propagation delay of standard logic cells in the analyzed technology is below 100 ps. For LET values up to 30 $MeV{\cdot}cm^2{\cdot}mg^{-1}$, the output SET pulse width increased gradually and then saturated, as seen in Figure 4. The saturation effect was more pronounced for the target inverters at larger distance from the output. It is worth to mention that when the number of inverters was increased to 100, the output SET pulse width increased linearly up to 164 ns.

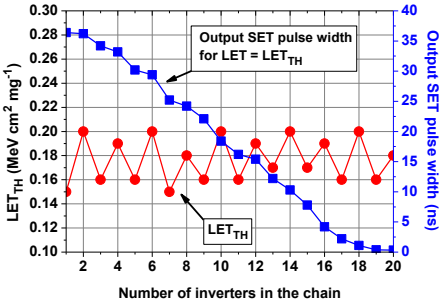

Figure 3: LET_{TH} and corresponding output SET pulse width for each inverter in the pulse stretching chain composed of 20 inverters

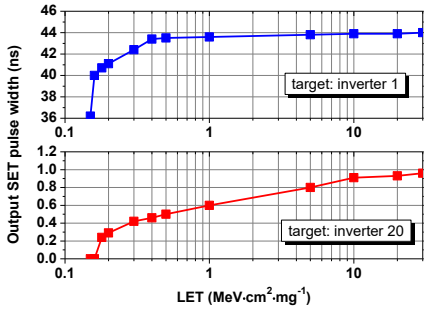

Figure 4: Output SET pulse width as a function of LET, when the current is injected in the first and last inverter of a 20-inverter chain

An important issue for any particle detector are the multiple SETs/SEUs caused by a single particle. We have evaluated the impact of double SETs on the 20-inverter pulse stretching chain by injecting the current pulses simultaneously in all adjacent inverter pairs. A sample of results is illustrated in Figure 5. In all cases the two simultaneous SETs were overlapping and resulted in a single pulse at the output of the chain. This is due to the low propagation delay of individual inverters and the stretching of the SET pulse. The only observed consequence of double SETs was the increase of the output SET pulse width. This implies that the proposed inverter chain is inherently robust to double SETs and is thus immune to erroneous SET counts.

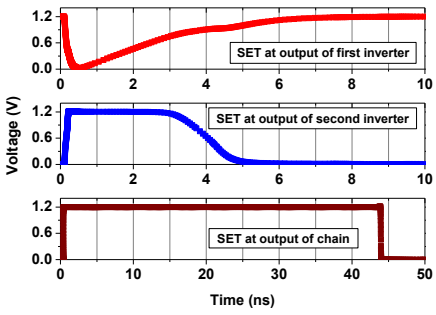

Figure 5: Effect of double SET caused by a single particle strike

IV. Monitor Design and Application

To obtain a functional particle flux monitor, the proposed detector should be interfaced with the processing logic for counting the induced SETs. A possible design of the processing logic is illustrated in Figure 6. The sensing part is composed of N chains with M cascaded pulse stretching inverters per chain, and the outputs of all chains are connected to the OR-tree to obtain a single output. This configuration was chosen instead of the long inverter chain in order to avoid very long SETs which can cause long delays during the processing. Two OR-tree units, connected with AND gate, are used to mask any SETs induced in the OR gates. The output of AND gate is fed to the Triple Modular Redundancy (TMR) ripple counter, and the counter state is stored in the register bank. The control logic is responsible for reading the counter state, periodic reset of the counter and interface with the external logic. Radiation hardening by design is applied to the counter and register bank.

In comparison with the SRAM-based particle detectors which operate on a similar principle (counting of bit-flips), the proposed solution requires less processing resources. Namely, there is no need for the readout circuitry and error detection and correction logic as in the case of SRAM monitors. As a result, the overall cost of the proposed solution would be lower. Similarly to the SRAM-based detectors, the proposed solution can be implemented in standard CMOS process. However, as the operating principle of the proposed detector is based on counting the transient events (SETs) and due to its inherent immunity to double SETs, the possibility of error accumulation is eliminated as long as the TMR counter is periodically reset.

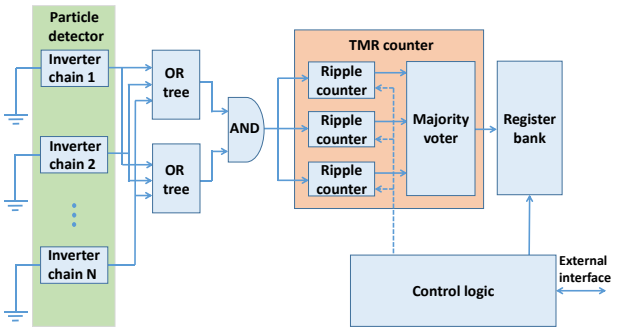

Figure 6: Particle detector with processing logic

An important requirement in the design of radiation monitor is to achieve a high ratio of detector's sensitive area to the area of the processing logic. The sensing area in this case is defined by the total area of inverter chains. The TMR counter, register bank and control logic have a fixed area which is independent of the number of inverter chains, whereas the area of the OR-tree depends on the number of chains. Taking as example N = 1024 (chains) and M = 20 (inverters), and considering that the area of one inverter with the previously defined sizes can be around 10 µm^2, the sensing area is around 204800 µm^2. For such configuration are required 341 4-input OR gates with the total area of around 4000 µm^2. Therefore, it can be estimated that the sensing area would account for more than 85 % of the overall monitor area, thus ensuring high sensitivity.

The proposed particle flux monitor can be implemented either as a stand-alone chip or integrated within a target chip. It is intended to act as an enabler of the self-adaptive switching of operating modes within a multi-/many-core processing system, in order to achieve the trade-off between fault-tolerance, power consumption and performance. Based on the measured SET count rate, the particle flux and then the SER of the target system can be calculated. With respect to the reliability requirements (desired SER), the fault-tolerance of the target system can be fine-tuned by activating various mechanisms, such as Dual Modular Redundancy (DMR), Triple Modular Redundancy (TMR), Quadruple Modular Redundancy (QMR) and frequency/voltage scaling [2, 15]. To establish the analytical correlation between the measured SET count rate and the particle flux, the irradiation tests have to be performed.

V. Conclusion

This paper investigates the applicability of custom-sized inverter chains as detectors of energetic particles responsible for the soft errors in CMOS integrated circuits. The results obtained from SPICE simulations indicate that the proposed detector has substantial advantages over the existing solutions for particle flux measurement, such as SRAM-based detectors. Future work will be focused on implementation of the detector on a chip and characterization under radiation exposure.

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