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Prediction of Single Event Transient Propagation Using Machine Learning Models

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Abstract— **In this paper, the applicability of existing machine learning (ML) models for predicting the variation of Single Event Transient (SET) pulse width during propagation through standard combinational cells is analyzed. Ten regression models have been trained on a dataset generated from SPICE simulations conducted for INV, NAND2 and NOR2 gates from the IHP's 130 nm standard cell library. The SET pulse width at the output of each gate was analyzed in terms of input pulse width and polarity, size factor of analyzed gate, size factor of load gate, supply voltage and temperature. Results have shown that some models provide best prediction accuracy for specific gates. The trained models could be also used to predict the change of SET pulse width across combinational paths, but the prediction accuracy in that case is lower than for individual gates. Future work will be focused on improving the prediction accuracy of ML models and development of an automated ML-based tool-flow for SET analysis.**

Keywords— Single Event Transient (SET) propagation, machine learning prediction, standard combinational cells

I. Introduction

Voltage glitches caused by high-energy particles, known as Single Event Transients (SETs), represent a serious reliability concern for digital integrated circuits (ICs) employed in harsh radiation environments, such as space. In ICs designed in nanoscale semiconductor technologies, SETs may be induced by particles with a very low Linear Energy Transfer (LET), e.g., LET < 2 MeVcm^{2}mg^{-1} [1], and a single particle may strike up to five or six adjacent logic gates [2, 3]. Moreover, the reduction in supply voltage and the increase in clock frequency have increased the likelihood that an SET will propagate through a combinational circuit and result in a soft error [4, 5].

Modern ICs are usually based on standard logic cells, which are inherently sensitive to radiation effects. In order to assess the SET sensitivity of a standard-cell-based design and apply appropriate mitigation measures, it is necessary first to evaluate the SET effects in standard logic cells. Depending on technology, design, operating, and irradiation parameters, the typical duration of SET pulses generated in standard logic cells may vary from tens to hundreds of ps. When no logical masking occurs across a combinational path, an SET pulse may be either suppressed due to electrical masking or broadened due to propagation-induced pulse broadening.

The SET effects in standard logic cells can be analyzed with device (TCAD) and electrical (SPICE) simulations. For characterizing the entire standard cell library, millions of simulation runs may have to be performed in order to capture complex dependencies of the SET pulse width on various parameters, such as target gate driving strength, load gate driving strength, supply voltage, temperature, particle LET, etc. Reading a large database with simulation results during analysis of a complex design may be very time-consuming even with automated tools. To overcome this issue, various analytical models for SET effects have been proposed. Physics-based SET models can reproduce accurately the real fault mechanisms, but they are usually very complex and include technological parameters that are often not available to circuit designers. Simplified models could be derived by fitting the simulation results, but these models usually cannot capture all dependencies.

Machine learning (ML) models have been investigated over the past years for the analysis of transient and permanent faults in digital designs. The key advantage of ML models is good prediction accuracy with very low runtime. ML enables the modeling of complex dependencies, which is a key advantage over standard fitting-based models. Several papers have studied the use of ML models for predicting SET generation and propagation effects [6 - 12]. However, to the best of our knowledge, the use of ML models to predict variations in SET pulse width during propagation through standard combinational cells and logic paths, while considering different design and operating settings, has not been investigated.

In this work, we present an analysis of the applicability of existing ML models for the assessment of SET propagation through combinational logic. Using results from electrical simulations as a training dataset, ten ML models have been trained to predict the variation of SET pulse width during propagation through standard combinational cells. The impact of gate size, load capacitance, supply voltage and temperature have been investigated. Our preliminary results indicate that different standard cells may require different models to achieve best prediction accuracy, which is an important finding.

The rest of the paper is organized into five sections. In Section II, the general flow for ML-based SET analysis is presented. Section III introduces the methodology for electrical

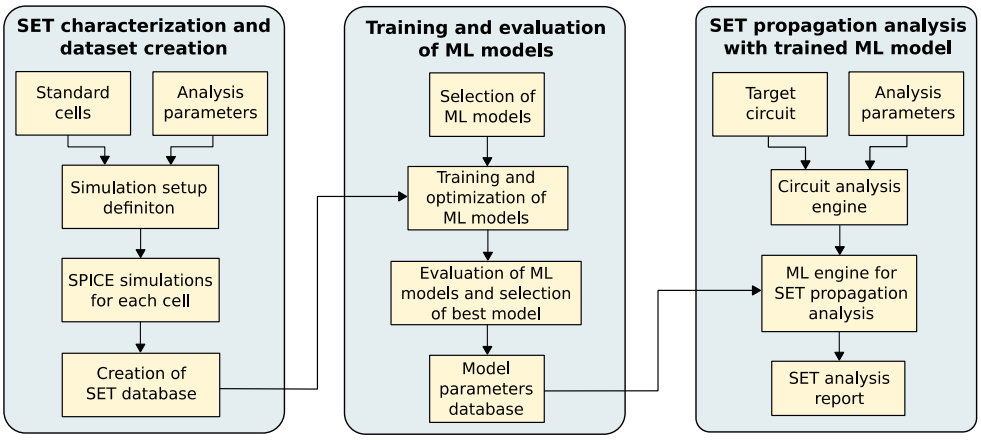

Figure 1: Proposed 3-phase flow for ML-based SET propagation analysis

level simulations of SET propagation, as a basis for establishing the training dataset for ML model training. The ML training procedure is discussed in Section IV. Obtained results are presented in Section V. The paper is concluded in Section VI.

II. Proposed Flow for Prediction of SET Propagation with Machine Learning

Our approach for ML-based prediction of SET propagation consists of three phases: (i) SET characterization and dataset creation, (ii) Training and evaluation of ML models, and (iii) SET propagation analysis with ML models. The proposed flow is illustrated in Figure 1.

In the first phase, electrical simulations are employed to characterize the SET propagation through individual standard cells. The variation of SET pulse width in terms of various parameters, such as gate size, load capacitance, supply voltage, temperature, etc., is analyzed. This process is performed only once for a given standard cell library.

In the second phase, the dataset obtained from simulations is used to train a number of selected ML models. Several existing ML models are analyzed in order to choose the one with best prediction performance.

Finally, in the third phase, the best ML model is employed to analyze the SET propagation in a real circuit. Note that this phase could also integrate the SET generation analysis.

In this work, we present the first two phases of the proposed flow. Integration of ML models into an automated SET simulation engine will be the follow-up work.

III. SET Characterization and Dataset Creation

The characterization of SET propagation through standard combinational cells was done using the Cadence Spectre tool. As a case study we have used the IHP's 130 nm bulk CMOS technology. This technology has been chosen for preliminary study because it has been qualified for space missions, and has been used for development of several commercial rad-hard chips, including several chips currently employed in the JUICE space missions.

In this analysis, three most common standard cells have been analyzed: INV, NAND2 and NOR2. Trapezoidal voltage pulse with different durations, and fixed rise and fall time constants, was used to model the SET pulse arriving at the inputs of analyzed gates. The SET pulse was fed to each input of the target gate, while other inputs were kept at logic levels enabling the signal propagation. The SET pulse width at the output of each gate was analyzed in terms of five parameters: input pulse width, driving strength of target gate, driving strength of load gate, supply voltage and temperature. The input pulse width was varied from 100 ps to 500 ps, because these are the most typical SET pulse widths for the 130 nm technology [13]. The simulations were done for both polarities of the input SET pulse. Supply voltage was varied from 0.8 V (minimum supply voltage) to 1.2 V (nominal supply voltage), and temperature was varied from -40 ºC to 125 ºC. For target and load gates, all available strengths were used, and INV gate was used as a load gate in all simulations.

IV. Training of Machine Learning Models

This section details the machine learning training procedure to predict the SET pulse propagation through various standard logic cells. The methodology is structured into three parts: (i) Preprocessing of the collected dataset, (ii) Selection of ML models, and (iii) Training and fine-tuning of ML models.

The dataset derived from Spectre simulations includes three separate datasets, one for each of the analyzed standard cells (INV, NAND2 and NOR2). For INV gate, the dataset includes 25 600 values, while each of the datasets for NAND and NOR gates includes 12 800 values. The dataset for INV has more values because there are more available driving strengths. For each gate type, the dataset consists of SET pulse widths at the gate's output for different combinations of input pulse widths, temperatures, supply voltages, gate's driving strength and load gate's driving strengths. After preprocessing, which included analysis and labelling, the dataset for each gate was split into training (70%) and testing (30%) sets. Training set was used to train the ML models, while testing set was used to evaluate the prediction accuracy of the trained models.

The regression models were chosen to predict variations in the output SET pulse width. We have evaluated 10 established regression models from the *scikit-learn* library [14] as potential candidates: Linear Regression, Ridge Regression, Lasso Regression, Random Forest, Gradient Boosting, Support Vector Machine (SVM), Multi-Layer Perceptron (MLP), XGBoost, CatBoost and LightGBM.

Table I: Comparison of performance of ten ML models trained on simulation dataset for INV, NAND2 and NOR2 gates (shaded values are for models with best performance for each gate)

ML model	INV			NAND2			NOR2		
	R^2	MSE	MAE	R^2	MSE	MAE	R^2	MSE	MAE
Linear regression	0.88755	2682.893	32.112	0.86177	4080.766	45.963	0.73577	12875.403	80.182
Ridge regression	0.88755	2682.877	32.111	0.86178	4080.522	45.956	0.73577	12875.436	80.180
Lasso regression	0.88757	2682.492	32.045	0.86185	4078.401	45.881	0.73575	12876.512	80.174
Random forest	0.99975	5.949	0.85651	0.99898	30.016	2.237	0.99870	63.187	2.588
Gradient boosting	0.98122	448.100	12.741	0.98323	495.166	15.320	0.93777	3032.351	40.560
SVR	0.88195	2816.487	30.143	0.83704	4810.851	40.658	0.71861	13711.583	75.786
MLP	0.99324	161.321	7.525	0.98726	375.968	12.666	0.97180	1373.939	24.283
XGBoost	0.99982	4.371	0.698	0.99945	16.194	1.649	0.99880	58.385	2.543
CatBoost	0.99961	9.411	1.388	0.99977	6.761	1.354	0.99903	47.318	2.373
LightGBM	0.99936	15.296	1.663	0.99948	15.430	2.080	0.99774	110.072	4.829

During the training of selected ML models, we have applied several strategies to enhance the ML models' efficiency and accuracy in making predictions. We have used StandardScaler for feature standardization to mitigate the impact of feature scale differences, crucial for consistent data environments and effective learning. ML models depend on finely tuned internal parameters for accurate predictions. We have optimized the hyperparameters of models using grid search (GridSearchCV) and cross-validation, a proven method for identifying the best parameter settings that contribute to optimal model performance. The prediction accuracy of the models was assessed with three standard metrics: Mean Squared Error (MSE), Mean Absolute Error (MAE) and R^2 score.

V. Results and Discussion

A. *Prediction of SET Propagation in Individual Logic Gates*

The performance of all trained models for prediction of SET propagation in individual standard cells, in terms of R^2, MSE and MAE metrics, is shown in Table I. It is interesting to note that different ML models have shown best performance for individual gates. For INV, the best prediction accuracy was achieved by XGBoost model, with R^2 score of 0.99982, MSE of 4.371 and MAE of 0.698. For NAND2, the best performance was achieved by CatBoost model, with R^2 score of 0.99977, MSE of 6.761 and MAE of 1.354. For NOR2, the best performance was also achieved by CatBoost model, with R^2 score of 0.99903, MSE of 47.318 and MAE of 2.373. These results indicate that multiple ML models may be required for the analysis of SET propagation in a combinational circuit.

In order to evaluate the relative error of the best ML models with respect to simulation results, we have compared the ML prediction with the SPICE results for 320 randomly selected input pulse widths and different combinations of gate sizes, supply voltage and temperature. This test dataset has not been previously used for training of ML models. The results are illustrated in Figures 2 - 4. For all investigated gates, the largest relative errors were obtained for output SETs shorter than 150 ps. If these large errors are neglected, the average relative error for INV, NAND2 and NOR2 was 18.3%, 16.7% and 15.9%, respectively. For SET pulse widths larger than 200 ps, the relative error was below 10 % for all gates. Although these errors are large, the results confirm the possibility to predict the propagated SET pulse width using existing ML models. To enhance the prediction accuracy, larger training datasets, especially for very short SETs, are needed. In addition, alternative ML models could be investigated.

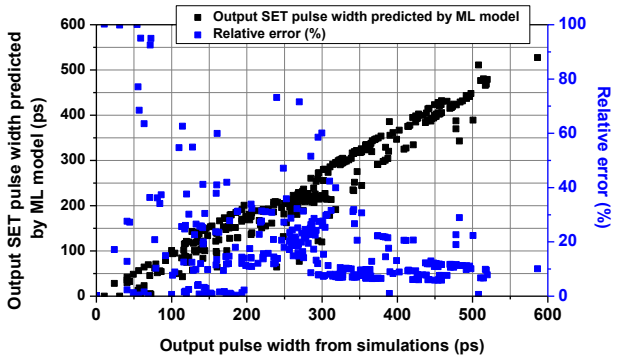

Figure 2: Relation between SET pulse width at output of INV gate obtained by XGBoost model and SPICE simulations, and relative error of XGBoost model with respect to SPICE simulations

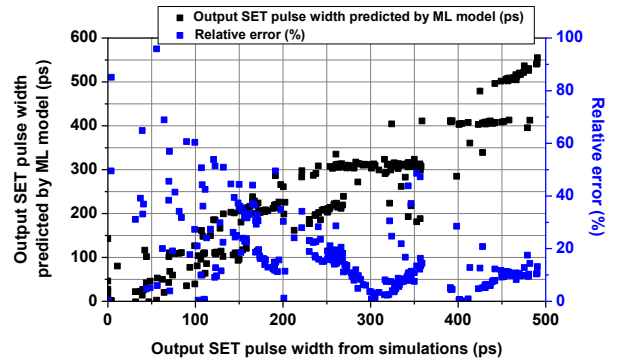

Figure 3: Relation between SET pulse width at output of NAND2 gate obtained by CatBoost model and SPICE simulations, and relative error of CatBoost model with respect to SPICE simulations

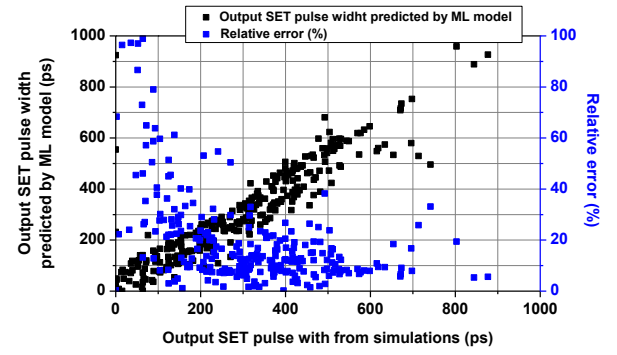

Figure 4: Relation between SET pulse width at output of NOR2 gate obtained by CatBoost model and SPICE simulations, and relative error of CatBoost model with respect to SPICE simulations

Table II: SET pulse width at the output of test logic paths obtained with ML models and SPICE simulations

Settings	Output SET pulse width from ML model (ps)	Output SET pulse width from SPICE simulations (ps)	Relative error (%)
Path 1, Vdd=1.2V, Temp = 50 ºC, Input PW = 150 ps (positive pulse)	109.4	165.7	34 %
Path 1, Vdd=1.2V, Temp = 50 ºC, Input PW = 150 ps (negative pulse)	110.5	134.4	17.8 %
Path 1, Vdd=1.1V, Temp = 80 ºC, Input PW = 380 ps (positive pulse)	510.2	400.6	27.4 %
Path 1, Vdd=1.1V, Temp = 80 ºC, Input PW = 380 ps (negative pulse)	511.7	367.1	39.4 %
Path 2, Vdd=1.2V, Temp = -20 ºC, Input PW = 240 ps (positive pulse)	215.4	302.7	28.8 %
Path 2, Vdd=1.2V, Temp = -20 ºC, Input PW = 240 ps (negative pulse)	204.6	181.9	12.5%
Path 2, Vdd=1 V, Temp = 100 ºC, Input PW = 480 ps (positive pulse)	517.7	588.3	12 %
Path 2, Vdd=1 V, Temp = 100 ºC, Input PW = 480 ps (negative pulse)	502.3	381.3	31.7 %

B. Prediction of SET propagation in Logic Chains

To assess the accuracy of ML prediction on realistic logic paths, we have applied the trained ML models to predict the SET pulse widths at the output of two short combinational paths composed of analyzed standard cells. The first path (Path 1) is composed of NAND2, NOR2, NOR2 and NAND2 gates, while the second path (Path 2) is composed of NAND2, INV, NOR2, NAND2 and NOR2 gates. For each test path, we have used randomly selected combinations of input pulse width (with both polarities), supply voltage and temperature.

The results obtained with the ML models and SPICE simulations are shown in Table II. For each gate we have used the model that has shown the best performance after training. As can be seen from the results in Table II, the relative error for the analyzed cases varies between 10 and 40%. It can be also seen that in some cases the predicted value is greater than the actual one, while in other cases it is smaller than the actual value from simulations. Such high relative errors could be related to the accumulation of error across the path. An important aspect contributing to the prediction error is that we have used only inverter as a load gate during training, while in the test paths the load gates are also NAND and NOR gates.

VI. Conclusion

In this work, we report our preliminary results for the ML-based SET propagation prediction. Using the dataset obtained from SPICE simulations, ten ML regression models have been trained to predict the variation of SET pulse width during propagation through standard logic cells. The SET pulse width at the output of a target gate was analyzed as a function of target gate's size factor, load gate's size factor, supply voltage, temperature and input SET pulse polarity. The main observation is that different models may be required to achieve the best prediction accuracy for individual gates. Initial analysis has shown that the relative error of ML models is high for very short SETs and decreases as the width of SET pulse increases.

As a future work, our primary goal will be to improve the accuracy of the ML-based SET propagation prediction. To this end, we intend to enlarge the training dataset, analyze other standard cells, and investigate other prediction models, such as Graph Neural Networks. The next step would be to consider other transient and permanent faults, and the combined impact of multiple faults. Our ultimate goal is to automate the whole characterization and analysis process in order to enable time-efficient analysis of SET effects in complex designs.

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References

[1] P. E. Dodd et al., "Production and Propagation of Single Event Transientsin High-Speed Digital Logic ICs," IEEE Transactions on Nuclear Science, 2005.

[2] R. Harada, Y. Mitsuyama, M. Hashimoto, T. Onoye, "Neutron Induced Single Event Multiple Transients with Voltage Scaling and Body Biasing," in Proc. IEEE International Reliability Physics Symposium (IRPS), 2011.

[3] J. Zhang, J. Chen, P. Huang, S. Li, L. Fang, "Angular Dependency on Heavy-Ion-Induced Single-Event Multiple Transients (SEMT) in 65 nm Twin-Well and Triple-Well CMOS Technology," Microelectronics Reliability, vol. 91, 2018.

[4] N. N. Mahatme et al., "Comparison of Combinational and Sequential Error Rates for a Deep Submicron Process," IEEE Transactions on Nuclear Science, vol. 58, no. 6, 2011.

[5] J. A. Maharrey et al., "Impact of Single-Event Transient Duration and Electrical Delay at Reduced Supply Voltages on SET Mitigation Techniques," IEEE Transactions on Nuclear Science, vol. 65, no. 1, 2018.

[6] A. Hajian, S. Safari, "Modeling Soft Error Propagation in Near-Threshold Combinational Circuits Using Neural Networks," Journal of Electronic Testing, vol. 35, 2019.

[7] R. Song et al., "Machine Learning based SET Propagation Prediction for Large Scale Integrated Circuits," in Proc. International Conference on ASIC (ASICON), 2021.

[8] C. Xu et al., "Machine Learning Regression-Based Single-Event Transient Modeling Method for Circuit-Level Simulations," IEEE Transactions on Electron Devices, 2021.

[9] M. Andjelkovic et al., "Prediction of Generated Single Event Transient Pulse Width Using Artificial Intelligence Methods," in Proc. International Conference on Microelectronics (MIEL), 2023.

[10] Z. Zhang et al., "A Learning-Based Approach for Single Event Transient Analysis in Pass Transistor Logic," in Proc. International Symposium on Online Testing and Robust System Design (IOLTS), 2023.

[11] J. Lin et al., "Machine Learning-Assisted Single-Event Transient Model for 12nm FinFETs for Circuit-Level Simulations," in Proc. International Conference on ASIC (ASICON), 2023.

[12] V. Saxena, Y. Jain, S. Mittal, "Machine Learning and Polynomial Chaos Models for Accurate Prediction of SET Current Pulse," in Proc. IEEE Computer Society Annual Symposium on VLSSI (ISVLSI), 2023.

[13] B. Narasimhan et al., "Characterization of Digital Single Event Transient Pulse Widths in 130 nm and 90 nm CMOS Technologies," IEEE Transactions on Nuclear Science, 2007.

[14] Pedregosa, et al, "Scikit-learn: Machine Learning in Python", Journal of Machine Learning Research, 2011.