Standard Delay Cells with Improved Tolerance to Single Event Transients

M. Andjelkovic, C. Calligaro, O. Schrape, U. Gatti, F. A. Kuentzer, and M. Krstic

Abstract – The radiation-induced voltage glitches, known as Single Event Transients (SETs), represent an increasingly critical reliability threat for CMOS integrated circuits (ICs) employed in space missions. In ICs realized with standard digital cells, special design measures are required to reduce the sensitivity to SETs. The standard delay cells implemented with skew-sized inverters are exceptionally vulnerable to SETs, as the SET pulses induced in these cells may be significantly longer than those in other stan-dard cells. In this work, the SET robustness of an alternative design of delay cells based on two inverters and two decoupling capacitors is investigated. Electrical simulations have shown that the SET robustness of the proposed delay cell is inversely related to the propagation delay. With appropriate transistor sizing, the proposed design is more tolerant to SETs than the standard delay cells with skew-sized inverters.

I. Introduction

Ionizing radiation is one of the main causes of failures in modern nanoscale ICs employed in space applications. Among various radiation-induced effects in ICs, the SETs are particularly critical for CMOS technologies. An SET is a voltage glitch caused by the passage of a single energetic particle through a sensitive transistor in a combinational circuit. Such a glitch may cause a soft error (bit-flip) if it propagates through a logic path and is captured by a storage element (e.g., a flip-flop). The contribution of SETs to the total soft error rate (SER) of an IC increases with technology scaling and increase of clock frequency. For example, in 40 nm technology, the SER of a combinational chain may exceed the SER of a flip-flop chain at clock frequencies beyond 2 GHz [1].

Due to the inherent electrical, logical and temporal masking effects, only a fraction of gates in any combinational circuit have dominant contribution to the total system SER. As shown in [2], around 50 % of gates in a complex design contribute to over 80 % of soft errors. Therefore, applying traditional redundancy-based hardening techniques, such as Triple Modular Redundancy, would not be cost-effective for combinational circuits due to large area and power overhead. A widely used approach for reducing the combinational SER is based on selective hardening of a small subset of the most sensitive circuit nodes [3]. Such an approach cannot eliminate all possible SETs, but it can still significantly reduce the SER, with acceptable area, power and performance penalties.

The selective SET mitigation requires to consider the SET sensitivity of individual logic cells. This is particularly important for ICs designed with standard non-rad-hard libraries. The hardening of individual standard cells can be performed by redesign of the cell's structure, replacement of a sensitive cell with a less sensitive one or an alternative logic implementation, or by connecting redundant elements to the cell's output. The aim of applied mitigation measures is to increase the critical charge of sensitive nodes, and/or to attenuate or completely filter the SET pulses. Two most versatile approaches are the transistor/gate upsizing and insertion of dedicated SET filters in logic paths.

In our previous work [4], we have shown that the standard delay cells based on skew-sized inverters are more sensitive to SETs than other standard cells. As the standard delay cells are used in digital designs for optimization of logic path delays, it is important to ensure their robustness to SETs. We have proposed two modified designs based on hardware duplication, but both solutions introduce significant area overhead [4]. In this work, we explore an alternative design based on inverters and decoupling capacitors. The proposed solution has higher SET robustness than the variant with skew-sized inverters, and occupies less area than the duplication-based solutions.

The rest of the paper is organized as follows. Section II dicusses the related work. The standard delay cell based on decoupling capacitors is intoduced in Section III. The simulation analysis of the proposed design is presented in Section IV. In Section V, the proposed delay cell design is compared with previous solutions.

II. Related Work

A typical design of standard delay cells (SDCs) is based on a chain of an even number of inverters, where some of the inverters are skew-sized. We denote such a cell as SDC_SKEW. Using the skew-sized inverters enables to obtain the required propagation delay with a minimum number of inverters in the chain, thus saving the area. Fig. 1 illustrates a schematic of a four-inverter SDC_SKEW implemented in the IHP's 130 nm bulk CMOS technology, where the second and third inverters are skew-sized. By

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adjusting the channel width and length of the skew-sized inverters, the required propagation delay can be obtained.

To the best of our knowledge, the SET effects in standard delay cells have been studied for the first time in our previous work [4]. The analysis was done by employing a standard current injection approach, with electrical simulations. For this purpose, a bias-dependent current model [5] was used to inject the current pulses in the cell nodes. It was shown that the SETs induced in SDC_SKEW may be at least 100 ps longer than those in other combinational cells. Such long SETs are attributed to the pulse stretching effect of the skew-sized inverters.

In order to alleviate the SET effects in the analyzed SDC_SKEW cells, we have proposed two mitigation solutions [4]. First approach is based on complete duplication with a guard gate (SDC_CD), as depicted in Fig. 2. Second approach (Fig. 3) employs partial duplication with a guard gate (SDC_PD), i.e., only the skew-sized transistors are duplicated. Both of these approaches have been shown to eliminate the SETs in the skew-sized inverters. However, the added guard gate and inverter are additional points of failure, and the SETs in these nodes are comparable to other standard cells. Furthermore, the area overhead is over 85 % for SDC_PD and over 120 % for SDC_CD.

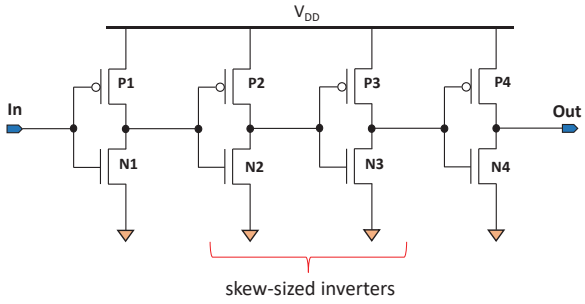

Fig. 1. Standard delay cell with two skew-sized inverters (SDC_SKEW)

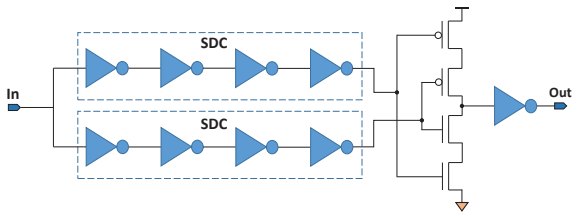

Fig. 2. SDC_SKEW with complete duplication of all inverters (SDC_CD) [4]

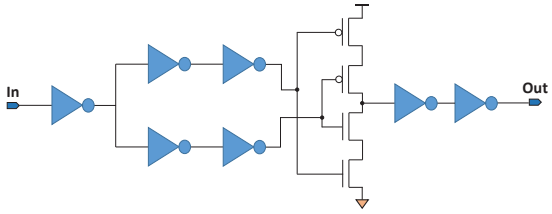

Fig. 3. SDC_SKEW with partial duplication of the most sensitive inverters (SDC_PD) [4]

III. Standard Delay Cell with Decoupling Capacitors (SDC_DECAP)

As an alternative to the standard delay cells with skew-sized inverters, we have investigated a delay cell realized with decoupling capacitors. Here we denote these cells as SDC_DECAP. The SDC_DECAP is composed of two standard CMOS inverters and two decoupling capacitors (DECAPs) connected between the output of first inverter and supply rails, as shown in Fig. 4. The decoupling capacitors are constructed from MOS transistors, by connecting the drain, source and bulk as one terminal, while the gate is another terminal.

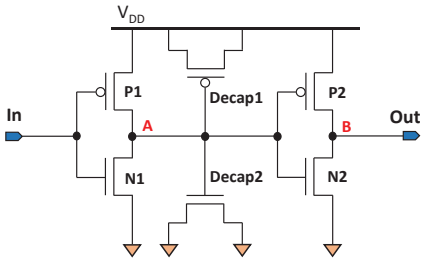

Fig. 4. Standard delay cell with decoupling capacitors (SDC_DECAP)

The propagation delay of SDC_DECAP cell is proportional to the decoupling capacitance C_{DECAP}, which is defined by the transistor size (channel width and length), according to the relation [6],

$$C_{DECAP} = C_{OX} \cdot W \cdot L + 2 \cdot C_{OL} \cdot W \qquad (1)$$

where C_{OX} is the oxide capacitance per unit area, C_{OL} is the overlap and fringing capacitance per unit width of the device, W is the channel width of transistor and L is the channel length of transistors.

Delay cells based on decoupling capacitors have been widely used for timing synchronization in digital designs [7]. However, to the best of our knowledge, the SET effects in delay cells realized with decoupling capacitors have not been investigated. In the design depicted in Fig. 4, only the inverters are sensitive to particle strikes. Since the off-state transistors are most sensitive to particle strikes, only two (out of six) transistors in SDC_DECAP will be sensitive.

IV. Analysis of Propagation Delay and SET Robustness of SDC_DECAP

A. Propagation Delay of SDC_DECAP

In order to investigate the dependence of the propagation delay of SDC_DECAP as a function of the size of inverters and decoupling capacitors, we have conducted a series of electrical simulations using a commercial tool Cadence Spectre. The propagation delay was determined as the time interval between the rising edge of input and output pulses. As a case study, we have used the IHP's 130 nm CMOS technology. This is a commercial technology with

sufficient robustness for many space applications [8]. All simulations were done for nominal core supply voltage of 1.2 V and temperature of 27 ºC.

Fig. 5 shows the dependence of the propagation delay on the channel width of decoupling capacitors, for two driving strengths of inverters (x1 and x2), and for constant channel length. The inverters with driving strength x2 have twice larger channel widths than x1 inverters, while x1 inverters have four times larger channel widths than the standard x1 inverters in the investigated 130 nm library.

It can be seen that decoupling capacitors have stronger impact on the propagation delay than inverters. The propagation delay increases linearly with the size of decoupling capacitors, which is in good agreement with the relation (1). For the channel width from 2 to 12 µm for Decap 1 and Decap 2, the delay is from 147 to 465 ps with x1 inverter, and from 110 to 298 ps with x2 inverter. Similar results are obtained if the channel length is varied, while the channel width is kept constant. Larger propagation delay can be obtained by increasing both channel width and length, but that was not analyzed in this study.

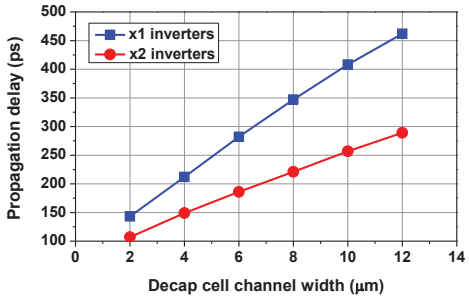

Fig. 5. Propagation delay of SDC_DECAP for different channel widths of decoupling capacitors (for channel length of 1 µm)

B. SET Robustness of SDC_DECAP

For evaluation of the SET sensitivity of the standard delay cell with decoupling capacitors, we have employed a current injection approach in Spectre simulations. A bias-dependent current source from [5] was used to inject SETs successively in nodes A and B (see Fig. 4). The rise and fall time constants of the current pulse were 10 and 100 ps, respectively. The SET robustness was assessed in terms of two metrics: (i) threshold Linear Energy Transfer (LET_{TH}), i.e., a minimum LET that can cause an SET, and (ii) SET pulse width at the output of SDC_DECAP cell.

The LET_{TH} for node A (first inverter), as a function of the size of decoupling cells, for two driving strengths of inverters, is shown in Fig. 6. It can be seen that LET_{TH} increases both with the size of inverters and the size of decoupling capacitors. However, the impact of inverter upsizing is stronger because it increases both the driving strength and the node capacitance [9]. The LET_{TH} for node B (not shown) also increases when the inverter is upsized, while decoupling capacitors have no impact.

In Fig. 7, the dependence of the SET pulse width as a function of the size of decoupling capacitors and inverters, when the current is injected in node A, is illustrated. The results are for LET of 60 MeV·cm^2·mg^{-1}, which is sufficiently large to cause SETs in most standard cells. Larger inverters provide better SET robustness, i.e., the SET pulse width decreases as the inverter size is increased. That is because larger gates have larger capacitance and driving strength, allowing for faster dissipation of induced charge [9]. However, increasing the size of decoupling capacitors leads to almost linear increase of the SET pulse width. This is due to the fact that larger load capacitance needs more time for charging/discharging [10]. Similar analysis was done for node B, and the results are shown in Fig. 8. In this case, the SET pulse width decreases for larger inverters, but it is independent of the size of decoupling capacitors.

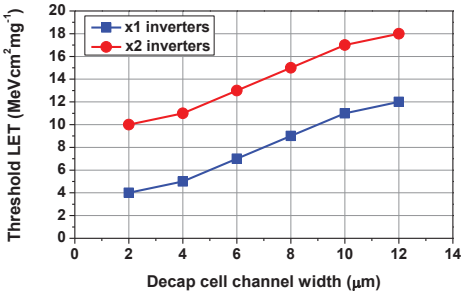

Fig. 6. Threshold LET (LET_{TH}) for node A, as a function of the channel width of decoupling capacitors and driving strength of inverters

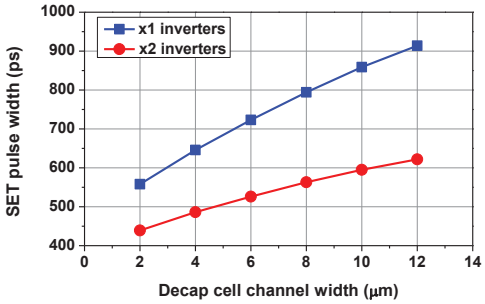

Fig. 7. SET pulse width as a function of channel width of decoupling capacitors and driving strength of inverters, when the SET current pulse with LET = 60 MeVcm^{2}mg^{-1} is injected in node A (see Figure 4)

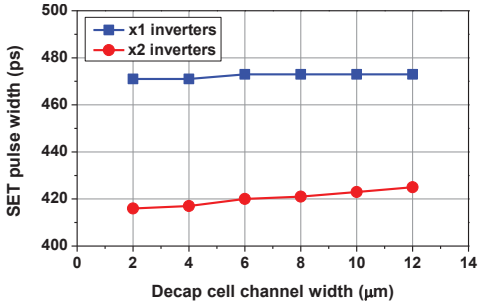

Fig. 8. SET pulse width as a function of channel width of decoupling capacitors and driving strength of inverters, when the SET current pulse with LET = 60 MeVcm^{2}mg^{-1} is injected in node B (see Figure 4)

TABLE I

COMPARISON OF FOUR STANDARD DELAY CELL IMPLEMENTATIONS WITH PROPAGATION DELAY OF 250 PS (NOTE: SET PULSE WIDTH RESULTS ARE OBTAINED FROM SIMULATIONS FOR LET = 60 MEV·CM^2·MG^{-1})

Standard delay cell variant	LET_{TH} (MeV·cm^2·mg^{-1})		SET pulse width (ps)		No. of sensitive nodes	No. of transistors per cell
	Most robust node	Most sensitive node	Most sensitive node	Most robust node		
SDC_SKEW	1.2	0.4	756	452	4	8
SDC_PD	1.22	0.8	634	486	4	18
SDC_CD	1.22	0.76	621	455	2	22
SDC_DECAP	17.4	1.25	597	423	2	6

C. Design Considerations for SDC_DECAP

Previous discussion has shown that while the upsizing of inverters and decoupling capacitors provides immunity to low LET (up to 20 MeV·cm^2·mg^{-1}), larger decoupling cells increase the sensitivity of first inverter for higher LET. Thus, the design of SDC_DECAP cells for radiation environment requires a compromise between the propagation delay and the SET robustness. According to Figs. 5 and 7, the SET pulse width due to strikes in first inverter increases almost linearly with the propagation delay. In other words, the cells with larger decoupling capacitance are less robust to SETs resulting from high LET. The SET pulse width can be reduced with larger inverters, but this also reduces the propagation delay.

Therefore, an optimal solution would be to have small propagation delay per cell. Then, larger propagation delay could be achieved by cascading multiple delay cells. For example, with x2 inverters and propagation delay of 200 ps, the SET pulse width at LET of 60 MeV·cm^2·mg^{-1} would be less than 550 ps, which could be filtered with conventional SET filtering logic.

V. COMPARISON OF STANDARD DELAY CELL IMPLEMENTATIONS

Table 1 presents a comparison of the SDC_DECAP cell with the standard delay cell based on skew-sized inverters (SDC_SKEW), and two variants of SDC_SKEW cell based on duplication (SDC_PD and SDC_CD). For the sake of fair comparison, all four implementations have been designed for the propagation delay of 250 ps.

As can be seen, the main advantages of SDC_DECAP over SDC_SKEW and SDC_PD is that it has less sensitive transistors (only two) and better SET robustness (higher LET_{TH} and lower SET pulse width). SDC_DECAP and SDC_CD have the same number of sensitive transistors (two), but due to different sizing, SDC_DECAP is more robust to SETs. Note that SDC_DECAP has 6 transistors, while SDC_SKEW, SDC_PD and SDC_CD have 8, 18 and 22 transistors, respectively. This indicates that the proposed SDC_DECAP design would be a favorable option among the four analyzed solutions in terms of chip area and power consumption saving.

VI. CONCLUSION

In this paper, the SET sensitivity of standard delay cells based on decoupling capacitors is analyzed. It has been shown with Spectre simulations that the proposed design has better SET robustness compared to the imple-mentation with skew-sized inverters. Furthermore, the area overhead is negligible compared to the hardened delay cells based on duplication with a guard gate.

As a future work, it is important to investigate the dependence of the propagation delay and SET sensitivity on supply voltage, temperature and process variations. It is also important to consider the layout effects. In addition, the applicability of delay cells as SET filters will also be addressed in our future work.

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