A 10/100 Ethernet Transceiver for Space Applications

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Abstract

As space systems evolve to become more complex, they need larger computing and communication capabilities. For example, larger data rates must be supported and more flexible technologies that enable several applications to share the network resources while providing predictable and reliable performance are needed. One of the approaches to address those issues is the adoption of Ethernet in space. This has the benefit of reusing existing and field proven technology that also provides evolution to larger data rates. Ethernet is currently used in some space systems and it is being designed into many others like the next generation of Arianne launchers or NASA Orion capsule. Integrated circuits that are used in space systems need to be designed to withstand the effects of radiation that causes errors and failures. These devices known as rad-hard need to be designed and manufactured using specific techniques and processes. Therefore, for Ethernet to be adopted in space, the respective rad-hard Integrated Circuits (ICs) need to be available. The European industry is working on several such ICs including an Ethernet switch and a transceiver. European industry has enhanced and extended the standard with Time Triggered Ethernet (TTE) to provide predictable and reliable performance. In this paper, SEPHY a 10/100 Mb/s rad-hard Ethernet transceiver designed for space applications is presented.

I. SPECIFICATIONS

The SEPHY transceiver is designed to support 10 and 100 Mb/s over twisted pair cabling as specified in the IEEE 802.3i and IEEE 802.3u standards commonly known as 10BASE-T and 100BASE-TX. The device does not implement the automatic configuration features defined in Ethernet like auto-negotiation or the automatic cable crossover [1]. These features are not required since space systems are designed with a fixed configuration and a deterministic behaviour is desired. This is just the opposite of home or offices on which ease of use and the ability to add and remove devices is key. Other functional difference with commercial transceivers is that the device implements special registers to count the number of radiation errors detected in the registers and cold spare capabilities for cold redundancy. Two interfaces for communication with the Media Access Controller (MAC) are supported, the Media Independent Interface (MII) defined in the IEEE 802.3 standard and the Reduced Media Independent Interface (RMII).

In terms of radiation tolerance SEPHY is designed to withstand up to 300 krad to TID and a SEU Bit Error Ratio better than 10^{-12} at LET>70 MeV/mg/cm². This enables the use of SEPHY chip in most space missions and particularly in launchers and earth orbiting satellites [2]. A key requirement is that the device has no ITAR restriction and to achieve this Microchip 150nm SOI technology targeted to space applications is used.

II. ARCHITECTURE

The block diagram of the device is shown in Figure 1 where digital blocks are coloured in blue and analog blocks in orange. It can be seen that SEPHY chip consists of five main blocks: A MAC interface block, a 10BASE-T digital block, a 100BASE-TX digital block, an Analog Front End (AFE) and a Common Blocks.

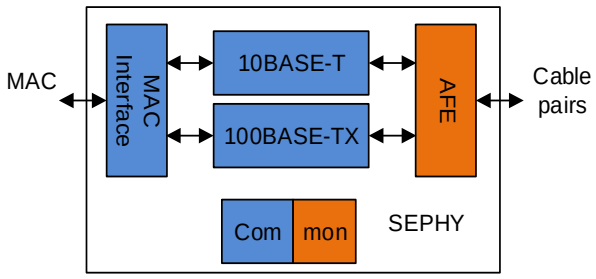

Figure 1: SEPHY block diagram

The MAC interface implements both MII and RMII at 10 and 100 Mb/s. The 10BASE-T and 100BASE-TX blocks implement the transmitters and receivers for both standards [3]. The analog front end is in charge of converting the analog signals received from the cable to digital on reception and the other way around for transmission. Finally, the common block contains both analog and digital functionality that is used in complete device providing clock, reset and the configuration/status registers.

The 10BASE-T part of SEPHY contains a Manchester encoder and a shaping filter on transmission and a Manchester decoder on reception. The device operates at 100MHz in this mode so that 10 samples are available per symbol, which facilitates the receiver implementation. In 100BASE-TX mode, the device operates a 125MHz so that only one sample is taken per symbol. The 100BASE-TX transmit path includes

a 4 to 5 bits mapping followed by a scrambler and an MLT3 encoder. The receiver for 100BASE-TX is by far the most complex block of the device and includes a programmable gain amplifier, an adaptive feedforward equalizer, clock recovery and baseline wander functions, an MLT3 decoder and a descrambler. The block diagram of the receiver is illustrated in Figure 2.

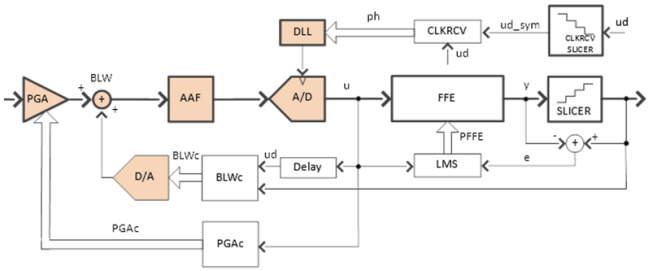

Figure 2: Block diagram of the 100BASE-TX receiver

The Analog Front End (AFE) contains a Digital to Analog Converter (DAC) and a shaping filter on transmission. On reception, it has a Programmable Gain Amplifier (PGA) to compensate cable attenuation followed by an Anti-Aliasing Filter (AAF) and an Analog to Digital Converter (ADC). A Delay Locked Loop is also used to adjust the clock of the ADC to that of the remote transmitter and a small DAC is used to compensate the Base Line Wander (BLW). These last two blocks are only needed in 100BASE-TX mode.

The common block generates the clock and reset signals for the rest of the blocks. To that end, it has a Phase Locked Loop (PLL) that can generate a 100MHz or a 125MHz clock depending on the mode selected (10BASE-T or 100BASE-TX). The common block also contains the Management Data Input Output (MDIO) interface defined in the standard to configure the transceiver and check its status.

III. TRANSCEIVER IMPLEMENTATION

The architecture described in the previous section has been implemented in Microchip´s 150 nm SOI technology targeting a 64 pin CQFP encapsulation. The device has a total area of 18.5 mm^2 and an estimated power consumption of 270 mW in 10BASE-T mode, 22% of which comes from digital section and of 635mW in 100BASE-TX mode with 70% of it coming from digital section. The digital part occupies most of the area with a total of around 80kgates. In more detail, over 75% of the area is digital and the rest is analog. On the digital part, the largest block is the adaptive equalizer that accounts for more than two thirds of the digital area. On the analog side, the largest block is the PLL. This device has been verified on simulation over PVT corners with cables lengths up to 100m and beyond as required by the standard.

IV. CONCLUSIONS

This paper has presented the first prototype of SEPHY, the first European space grade 10/100 Ethernet transceiver. The device has been manufactured with Microchip 150nm SOI Rad Hard technology (ATMX150RHA) and is designed to withstand radiation for TID levels higher than 300 krads and SEE for LET>70 MeV/mg/cm² [3] while achieving a BER better than 10^{-12}, so that it can be used in most space applications.

The die size is 4.3x4.3 mm^2. Estimated power is 270mW for 10BASE-T mode and 635mW for 100BASE-TX mode. Electrical and radiation tests on silicon are expected for September 2018. System tests will be performed in October 2018. Future work will focus on reducing the area and power of the device for the final version. This can be done by carefully dimensioning the adaptive equalizer that accounts for a significant part of area and power [4].

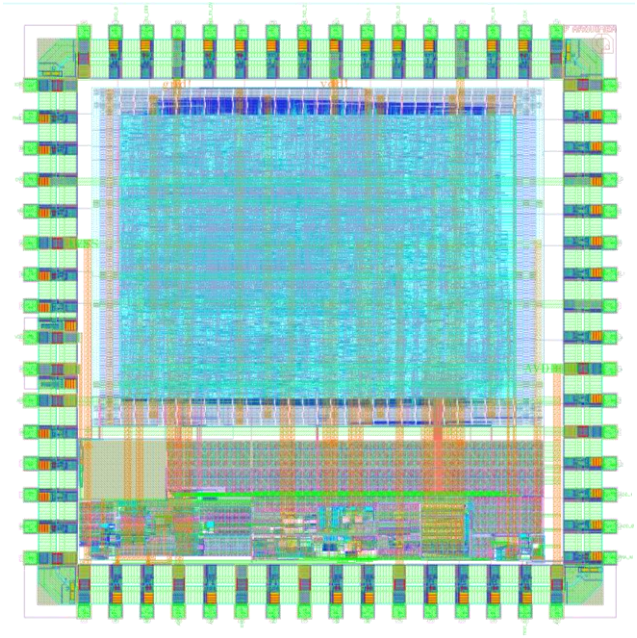

Figure 3: SEPHY die

V. ACKNOWLEDGEMENTS

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No.640243.

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