The Wafer-level Package Integration of a K/ Ka band Diplexer-on-PCB

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***Abstract*—Demanded by the increasing need for high data throughput in 5G and satellite communication, the operation frequency of the diplexers is continuously driven towards higher spectrums and the idea of integrating it on-chip or in-package is getting more appealing. In this paper, an edge coupled K/ Ka band diplexer is designed using the PCB technology with a 2.2 GHz band at receiving frequency and 2.6 GHz band at transmitting frequency with attenuation less than 3.2 dB. The RF performances of the diplexer is evaluated and optimized after being integrated with the chip front-end utilizing an advanced wafer-level packaging technique. The insertion loss of the chip-PCB interface is optimized to 0.3-0.5 dB, barely lowering the RF performances of the diplexers in the package.**

Keywords—diplexer-on-PCB, K/ Ka band, wafer-level package,

I. INTRODUCTION

In the wireless communication, a diplexer plays a key role in preventing intermodulation and filtering the transmitted and received signals in the frequency domain. To meet the future trend of high data throughput demand, the K and Ka band are chosen to be the operation band of the diplexer for satellite communication applications. Specifically, the downlink frequency is set to be 18-21 GHz and uplink is between 27-31 GHz.

With the increase of the operation frequency, the sizes of diplexers are becoming smaller, making them feasible to be integrated on-chip or in-package [1] [2]. For an easier integration, the planar printed filters are suitable options. An edge coupled microstrip filter is implemented on a PCB interposer for K/ Ka band duplexing. The resonating structures are only designed on a single layer to avoid the prepreg thickness variations during the fabrication for multi-layered boards. And the parallel coupled half wavelength filters are used to achieve a wide pass band by having a large coupling.

The K/ Ka band diplexers have been intensively explored due to its potential application in 5G and satellite communications [3] [4] [5]. Yet very few has filter designs operating at K/Ka band based on the PCB technology. Furthermore, even fewer investigates the performances of in-package diplexers. In this study, a K/ Ka band diplexer is designed and fabricated on an interposer PCB. The chip-board transition is taken into consideration

II. K/ KA BAND DIPLEXER ON PCB DESIGN

Two 5-pole Chebyshev bandpass filters are used as components for the diplexer. The resonance is implemented by using coupled microstrip lines with different characteristic impedances. Based on the designated filter performances listed in Table I, the design parameters can be easily extracted. However, the fabrication limits need to be taken into consideration as well.

TABLE I. DESIGN SPECIFICATIONS OF THE K/ KA BAND DIPLEXER

	Receiving band	***Transmitting band***
Passband	18 – 21 GHz	27 – 31 GHz
Stopband	< 15 GHz, > 25 GHz	< 25 GHz, > 35 GHz
Passband Attenuation	< 3.2 dB	< 2.5 dB
Stopband Attenuation	> 20 dB	> 20 dB

Considering a common RF material used in PCB fabrication – Astra MT-77, it has a dielectric constant of 3 and loss tangent of 0.0017. The available core thicknesses are

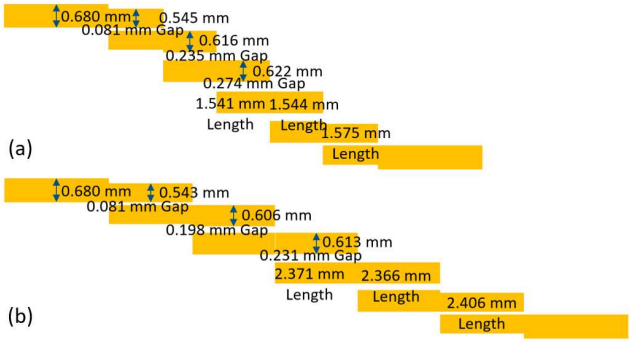

Fig. 1 The dimension of designed Bandpass filter on PCB. (a) is the geometry of the bandpass filter for transmitting band (~30 GHz), and (b) is the geometry of the bandpass filter for receiving band (~20 GHz).

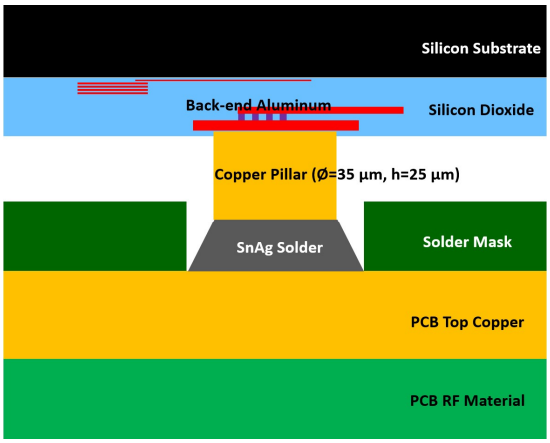

Fig. 2 The detailed cross-section view of the bump-on-pad technology using copper pillars. The interconnection is between chip and PCB.

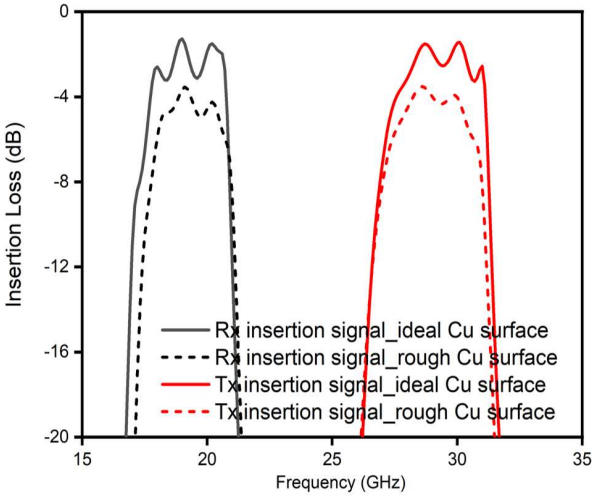

Fig. 4 The comparison of insertion losses for transceiving signals

from 0.064 mm to 1.524 mm. Considering the PCB fabrication limitation and signal wavelength, the microstrip line width needs to fall between 0.1 mm and 1.5 mm, ruling out the cores thicker than 0.5 mm. On the other hand, because of the minimum spacing of the standard PCB technology is 80 µm, adding another restraint to the filter design. This makes the filters with a thin substrate suffer from a larger in-band attenuation and narrower bandwidth. As a result, a 254-µm substrate is selected for the diplexer design, as is shown in Fig. .

III. WAFER-LEVEL PACKAGE INTEGRATION

The integration of the diplexer-in-package with the front-end circuits is facilitated by the advancing of wafer-level packaging technologies. Instead of using conventional wire bonds and solder bumps as chip-to-package interconnections, wafer-level packaging ensures a higher pin count and better electrical performances. In this study, a 200 mm BiCMOS wafer with IHP's state-of-the-art SG13 technology is used for wafer-level packaging. And a copper pillar technology from Pactech is selected for chip-package interconnection. As can be seen in Fig. 2, copper pillars are electro-plated on TM2 aluminum pads and then capped with SnAg solder. Finally

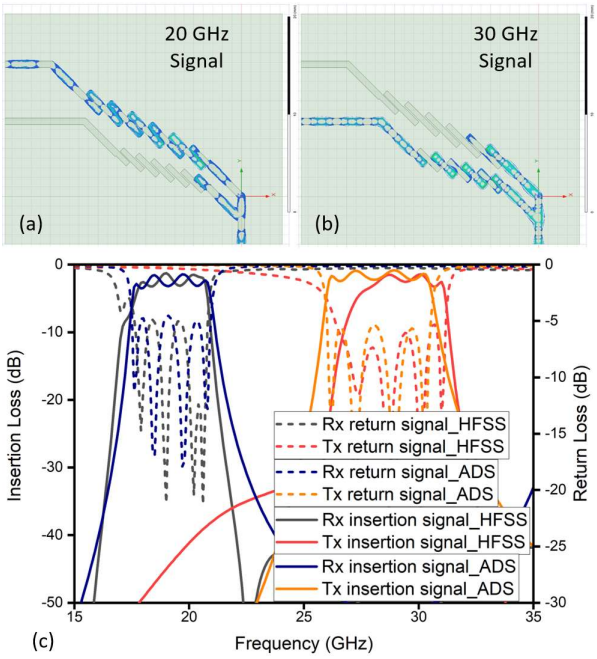

Fig. 3 The simulated performances of the diplexer on the PCB. (a) and (b) are the electric field propagating on the diplexer, corresponding to 20 GHz signal and 30 GHz signal respectively. (c) is the S parameter of the insertion and return losses of the bandpass filters.

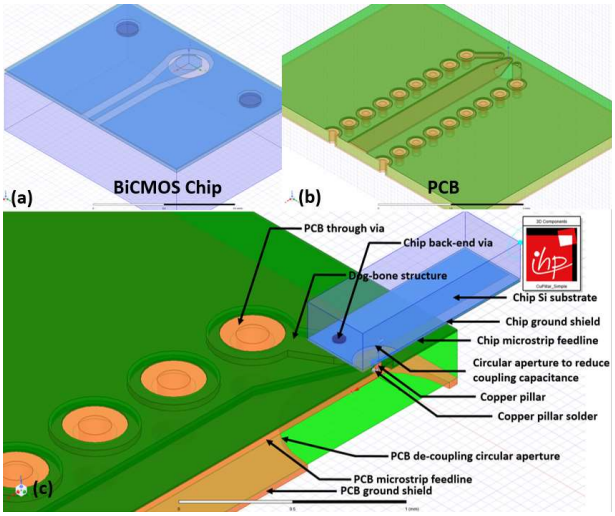

Fig. 5 The microstrip transition between the chip and the PCB. (a) is the feeding line on BiCMOS chip back-end structures, and (b) is the PCB feeding line. (c) is copper pillar interconnection assembly of the chip and the PCB.

the chips will be diced and flip-chipped onto PCB for soldering. The technological details of the copper pillar can refer to [6]. From packaging perspective, aside from the copper pillar size, another limiting factor is the I/O pitch. In general, a small pitch is desired to achieve a high I/O count. In this specific case, since the feature size of the PCB technology is much larger than that of the BiCMOS chip technology, the pitch is determined by the PCB. Taking the standard 1 oz copper core for example, the minimum spacing for standard technology is 85 µm and the minimum diameter of solder mask opening is 65 µm. Considering a 50 µm solder

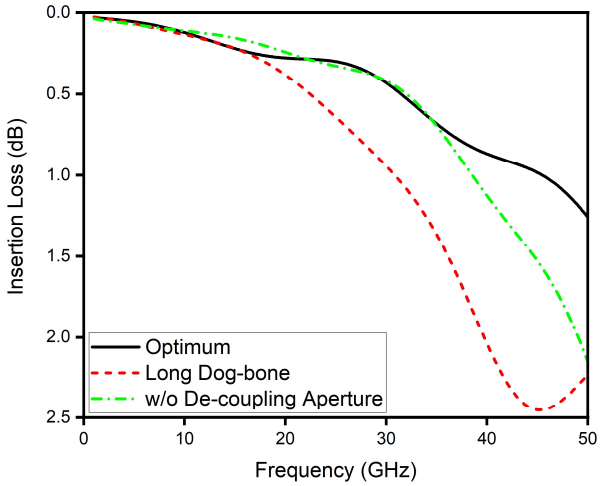

Fig. 6 The optimized insertion loss for a copper pillar microstrip transition and the influences of the key features of such a transition.

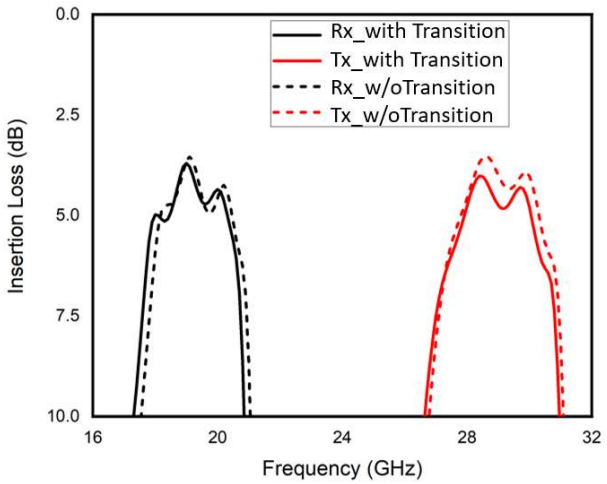

Fig. 7 The insertion losses comparison between filters with and without copper pillar microstrip transitions.

mask to metal clearance, the minimum I/O pitch for a standard PCB technology is 250 µm.

IV. Simulation Results and Optimization

A. The Performance of the Diplexer on the PCB

The characterization is firstly performed on a stand-alone diplexer on the PCB. ANSYS Electronics Desktop 2021 R1 HFSS and the keysight Advanced Design System (ADS) are used as the design tools. In the HFSS simulation, a driven modal solution is selected together with wave ports for S parameter analysis. The exterior boundary is set to be radiation instead of perfect matched layer due to the constrained fields. As for the meshing, since HFSS utilizes iterative meshing approach, a delta S of 0.02 is set to obtain results with high accuracies. On the other hand, the coupled-line bandpass filter design guide is used. The simulation results are shown in Fig. 3, where the S parameters obtained both from HFSS and ADS are compared. The bandwidth for 3 dB attenuation is 2.2 GHz (18.5 – 20.7 GHz) for Rx and 2.6 GHz (28.0 – 30.6 GHz) for Tx. The isolation between two channels are larger than 25 dB, indicating that the PCB-based diplexer is working properly at K/ Ka band. Additionally, the E-fields corresponding to 20 GHz and 30 GHz wave propagation are plotted in Fig. 3 as well. Worth noticing that the PCB copper cladding is notoriously rough to have enough adhesion, and needs to be accounted at the design stage. The Huray model with a 5 µm roughness value (Ra) is applied to the model as boundary conditions to evaluate the influence of the rough copper surfaces. The rough surface induces 2.3 dB loss at receiving frequency and 2.1 dB at transmitting frequency as is shown in Fig. 4.

B. The integration with the wafer-level packaging

The influence that the package assembly has on the performances of the diplexer is characterized by extending the feed line to the chip side. The transition is implemented using microstrips, the signals between PCB RF core material are transferred into chip back-end dielectrics. The grounds of PCB and chip back-end are connected with vias and a dog-bone configuration is used to structure PCB pads to avoid challenges of via-in-pad technology. As is illustrated in Fig. 5, the interconnection between the chip and the PCB requires huge dimension transition from around 600 um strip width on PCB to less than 20 um signal width on the chip, tapered lines are used on both sides to ensure a smooth transition and minimize radiation losses.

Two key features are found to have huge influences on the insertion loss of the transition structure – the de-coupling aperture underneath the copper pillar and the dog-bone structure. The influence of both of them are shown in Fig. 6. The feeding line losses are de-embedded from the results using the waveport de-embedding function in HFSS to extract the pure copper pillar transition loss. The de-coupling aperture, which has been mentioned a lot in many studies [7] [8] [9], doesn't start to increase the insertion loss until above 35 GHz. This result agrees with the previous study that such a feature is necessary for high frequency applications. However, for our 20-30 GHz diplexer application, no big difference is observed. On the other hand, the dog-bone structure adds an additional resonance frequency. With its length getting shorter, the resonance frequency is pushed higher, making the insertion loss smaller. According to the simulated results, the insertion loss is reduced by 0.5 dB at 30 GHz with a smaller dog-bone length. As a result, the insertion loss at is optimized to be -0.28 dB at 20 GHz and -0.43 dB at 30 GHz. The optimum performance is achieved with the dog-bone length set to be 0.4 mm, the PCB de-coupling aperture radius set to be 0.45 mm and the chip de-coupling aperture set to be 0.12 mm.

With the optimum transition configuration obtained above being applied to the diplexer, the insertion losses in the Rx and Tx band are presented in Fig. 7. The average insertion loss at the Rx and Tx band are increased by 0.16 dB and 0.53 dB respectively, showing a similar performance with the transition simulated alone. Based on the results obtained here, the copper pillar interconnection from chip to board contributes less than 0.5 dB insertion loss at K/ Ka band.

V. Conclusion

In this paper, an edge coupled diplexer operating at K/ Ka band is implemented using standard PCB technology. The copper surface roughness resulted from the PCB technology is found to have a 2.1-2.3 dB increase on the insertion loss. The received and transmitted signals are routed onto a standard BiCMOS chip using copper pillars. With such an advanced wafer-level packaging technology, an I/O pitch of 250 μm is realized, facilitating a high pin count. On the other hand, the transition loss of the RF signal using a microstrip structures with defected ground planes at 20 GHz and 30 GHz is shown to be 0.28 dB and 0.43 dB respectively. Such a loss is far less than the loss induced by PCB copper roughness, indicating a good prospect of the designated wafer-level packaging technology in RF applications.

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VI. Bibliography

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