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An assembly process oriented thermal-mechanical characterization of a fan-out wafer-level package

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***Abstract* — This study focuses on the stress analysis using finite element methods regarding a wafer-level Cu pillar package assembly process. The detailed assembly process is described, and a process-oriented thermal-mechanical coupled model is developed as the stress analysis tool. The finite element analysis is divided into two sections, namely the identification of the critical assembly step, and the analysis of the critical stress development. The package dimension and material property variables are parametrized by taking all the possibilities that could happen in the assembly process into consideration. The influence of each parameter is characterized and critical parameters are addressed, together with some initial assembly test results taken as validations. It is found that the most critical step for the solder is the reflow process, and the most critical stresses are the Cu pillar solder shear stress as well as the solder ball tensile stress.**

***Keywords* — Heterogeneous integration, chip-scale packaging, microassembly, thermal stresses**

I. Introduction

The wafer level packaging technology is acquiring more attentions nowadays due to its high I/O density, as well as outstanding electrical and thermal performances. One of the most critical issues associated with this packaging configuration is the fanning out the signals – it suffers from the large pitch required by the controlled collapse chip connection (C4) bumps and usually have a pitch between 0.3 and 0.5 mm [1]. On the other hand, the solder features a bad thermal and electrical conductivity, leading to bad performances for high frequency signals. Although some fan-out packaging approaches managed to solve both issues by embedding chips in redistribution layers or having silicon substrate as an interposer, both of them require additional set of masks, and thus increases the fabrication cost. In this study, a copper pillar based wafer level chip scale package based on cheap PCB technology is implemented and characterized using finite element methods. Unlike conventional solder joints, the copper pillar technology reduces the pitch to 0.25 mm. And by having a solder cap, the conductivity is kept close to that of the copper. Additionally, aside from the copper pillar deposition, all redistribution is implemented on PCB, greatly reducing additional mask costs.

Although such a package configuration has many advantages, its mechanical stability and reliability remains a challenge due to large mismatch of coefficient of thermal expansion (CTE) between the silicon chip and the PCB. Therefore, the mechanical characterization is of great importance. Most of the copper pillar reliability studies focus on the solder thermal cycling fatigue, as well as the bump shape optimizations [2-4]. This study, instead of investigating its long term reliability, attempts to reduce the stresses developed during the assembly by optimizing the packaging processes.

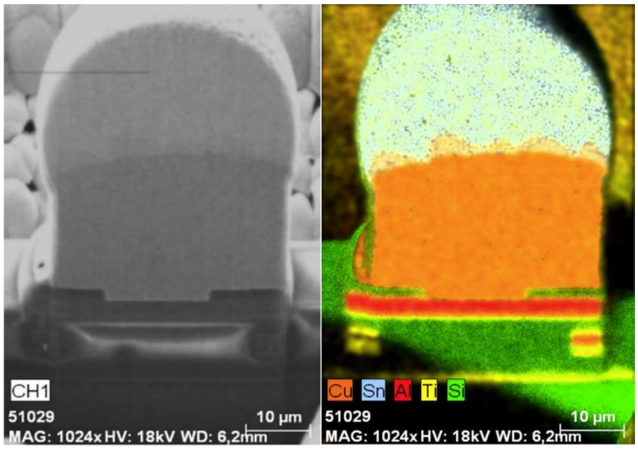

Fig. 1 A Cu-pillar example on a BiCMOS wafer.

II. Process Flow of the Assembly

In order to obtain a high interconnection conductivity, copper pillars are used to replace the conventional solder bumps. Unlike the solder bump connections, the copper pillar technology is compatible with the standard BiCMOS back-end processes. After the back-end passivation opening, a seed layer is sputtered onto the wafer. Then a mask is covered onto the wafer and aligned, preparing for the copper electro-plating. Then the Cu pillar and a SnAg solder cap are sequentially deposited. Lastly it goes through a reflow process to facilitate a good solder to copper adhesion. The finished copper pillar is shown in Fig. 1

The PCB, as an interposer to fan out the signals on the chip, also needs to be prepared. First thing is the selection of the pad configurations between solder mask defined (SMD) pads and non-solder mask defined (NSMD) pads. Due to the small solder volume (15 µm solder cap height), SMD pads are preferred to

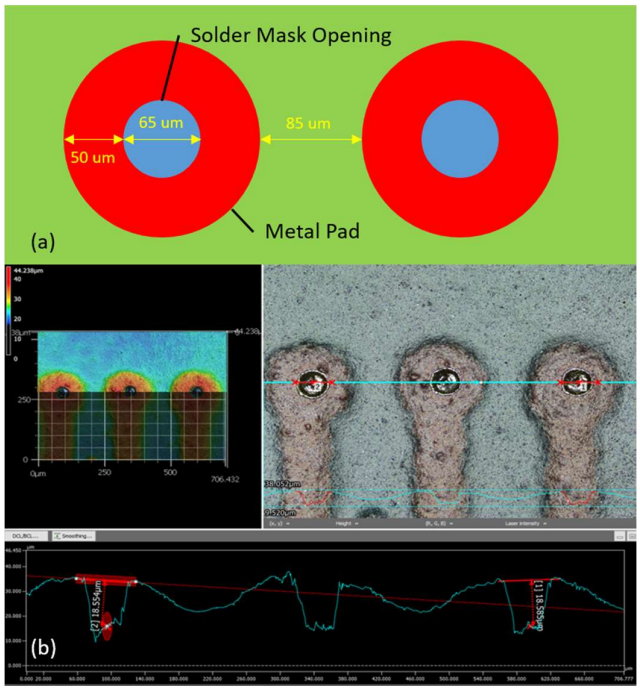

Fig. 2 The SMD pad configuration. (a) is the sketch, and (b) is the profilometry of the fabricated pads.

confine the solder spreading area and ensure a good soldering. As is shown in Fig. 2, the SMD pads are defined by a 165 µm diameter copper pad with a 65 µm laser opening of the mask. The pad to solder mask offset is designed to be 50 µm to mitigate misalignment errors. Additionally, the inter-trace spacing is 85 µm, which can be achieved using normal PCB technology. All the dimensions added up to a 250 µm pitch for the copper pillar interconnection. Then all the copper bare surfaces are coated with the ENEPIG surface finishing, namely a sequential coating of nickel, palladium and gold, to ensure a good solderability.

Then the assembly takes place. The chip is flipped onto the package PCB and aligned. After going through a reflow process, the copper pillar assembly is finished as the first step. Then an additional assembly step between the package board and the main board is carried out by another reflow process with low melting temperature solder bumps. The assembled samples are shown in Fig. 3, together with the cross section sketch as illustrations. During the whole process, the controllable variables are the solder mask thickness on the package board, the underfill between the package board and the main board, and the thermal interface material (TIM) between die surface and the main board.

III. Finite Element Modelling

An accurate numerical model is of great importance to the mechanical analysis of the package. In this study, ANSYS 2021R1 is exploited to develop the mechanical model.

A. Simulation Initial Setup

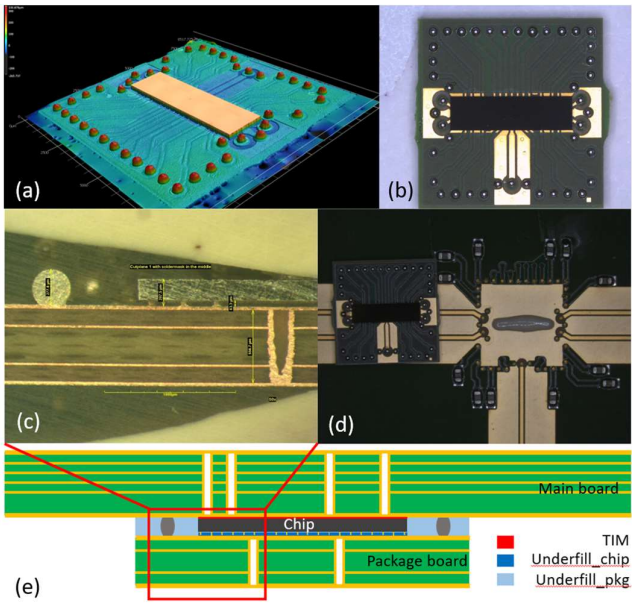

Fig. 3 An example of an assembled package with the proposed techniqeu. (a) and (b) are the chip to package board assembly, (c) and (e) are package cross section illustrations, and (d) is the package board to main board assembly.

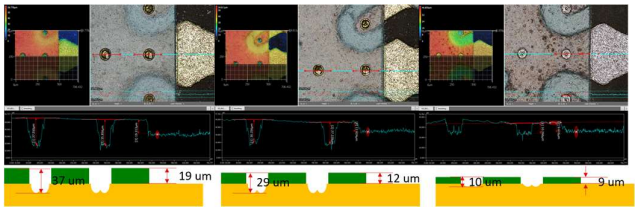

Fig. 4 The controlling of solder mask thickness.

Table 1. Material properties used in the mechanical model

	Temperature (°C)	CTE (ppm)	Young's modulus (Gpa)	Poisson ratio
Underfill_chip	-	10-80	2-8	0.3
Underfill_package	-	10-80	2-8	0.3
TIM	-	100-500	0.0001 - 0.0005	0.3
Silicon chip [5]	25	2.813	129.6	0.28
	150	3.107	128.4	0.28
solder (SAC305) [6]	25	21.5	52.6	0.4
	125	23.1	45.8	0.4
	200	23.5	40.4	0.4
PCB_substrate [7]	-	x/y: 12	19.2	0.183
	-	z: 60		
solder mask [8]	-	19	6.9	0.35
PCB_copper [9]	-	16.9	125	0.31

To ensure the accuracy of the model, the correct material properties are critical. The developed model utilizes the following materials, the copper used in the PCB traces and copper pillars, the PCB substrate resin material, the anisotropic silicon, the solder material for copper pillar and solder bumps, the underfill material, and the TIM material. The corresponding material properties are listed in Table 1.

Apart from the material properties, the modelling of the trace information is another key point. Due to the high aspect ratio and irregular shapes of the traces, the normal meshing techniques, namely the sweeping or tetrahedral patching, add complexity to the model calculation due to large number of elements. The trace mapping technique provides an alternative for a detailed interpretation of PCB trace information. Usually the structured mesh is firstly realized on the PCB body. Based on the meshing, the metal fraction within each element is calculated, and is assigned with an equivalent material property according to the material fraction. Such that the model includes all the necessary trace information for thermal characterization without complicating the model.

Lastly, a proper constraint of the degree of freedom is essential in the mechanical model to ensure a free warping of the package, and meanwhile without undermining the model convergence. Nodal displacement is applied to four corner nodes as boundary constraints – one node is constrained by all translational motions, two nodes are free to move only in the direction along the edge of the package, and one node is constrained by vertical movements. Such an approach facilitates the package body to warp freely, and having enough supports to avoid the undesired rigid body rotation.

B. The controlled input and output variables

A systematic study of the mechanical behavior of the package requires a careful selection of characterizing variables. In this assembly oriented study, the controlled variables are mainly the assembly interfaces, namely the solder mask between the copper pillar and die, the underfill and solder bumps between the package board and main board, as well as the TIM between the die and the main board. The critical part of the die to package board interface is the solder mask thickness, which can be controlled between 10-20 μm (see Fig. 4) or without solder mask. If it's thick enough to contact the die surface (Fig. 4), it behaves similarly to the underfill material – constraining the relative movement between die and package board surfaces and reduce the shear stresses accumulated on the solder. On the other hand, if it's thin, the solder will undertake all the stress coming from the CTE mismatch. The interface between the package board and the main board is characterized by the underfill and solder bumps. The dominating variables are the underfill CTE and Young's modulus, as well as its filling ratio. Besides, the distance between two boards can be viewed as another important factor, which can be characterized by solder ball size and chip thickness. Lastly, the interface between the die and the main board is characterized by the TIM material. And the variable parameters are its thickness and Young's modulus.

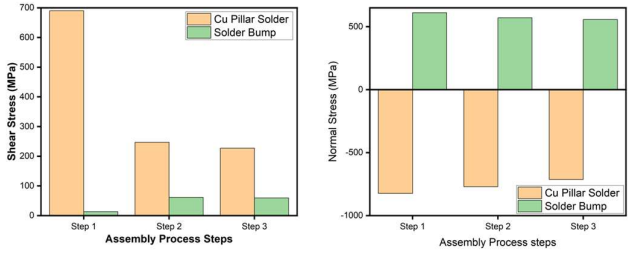

Fig. 5 The solder shear and normal stress development in the assembly process.

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C. The Assembly Process Modelling

The assembly and measurement of the package can be divided into three major steps – the reflow soldering, the fixation of the board onto the measurement chuck, and the normal operation of the package. During the reflow process, the package interface is stress free before the solder melting temperature. After the solder forms bonds between the contacting surfaces, and is cured to solid, stresses start to develop within the material. So the first step in the simulation setup is the solder cooling – because of the CTE mismatch between chip and boards, the package is warped during this process. Then, as the second step, the warped package is fixed onto a flat chuck using five screws. And lastly, the chip is put into normal operation in a steady state thermal model, then generated heat is coupled into the static structural through the power maps for thermal-mechanical simulation.

IV. Result Analysis and Discussion

Since the focus point of this study is the package assembly, the characterization is done for the copper pillars solder caps and the solder balls. For these materials, the analysing points are the shear stress induced by the CTE mismatch, as well as the tensile stress induced by the package deformation.

A. The stress variation during the assembly process

According to the definition of assembly steps above, three main steps are taken into consideration. The variation of the shear and normal stresses associated with each step are demonstrated in Fig. 5. As can be seen, the shear stress in the solder on Cu pillars are much more critical than that on the large solder balls, and the first step introduces the most shear stresses – almost 700 MPa shear stress is observed in the Cu pillar solder material. On the other hand, the solder bumps suffer more from the tensile stresses – over 500 MPa tensile stress is developed during the first assembly step. Based on these, the focus of the following analysis should be the first assembly step, and mainly about the shear stress in Cu pillar solders and normal stress in the solder balls.

B. The influence of the assembly processes

After identifying the fragile positions and critical stress types, the influence of the assembly needs to be taken into account as well.

There are many technological parameters can be varied during the assembly, e.g. the chip thickness, the solder mask thickness, and etc. All these variations are investigated regarding the two stresses afore mentioned. Fig. 7 demonstrates

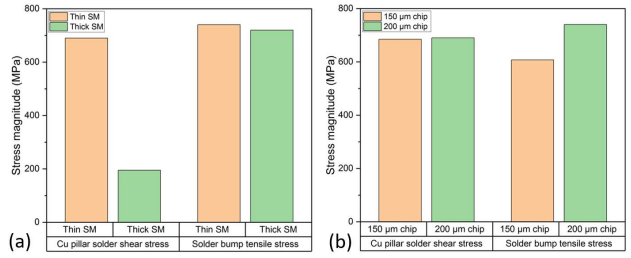

Fig. 6 the influence of the assembly process. (a) is the influence of the solder mask thickness, and (b) is the influence of the chip thickness.

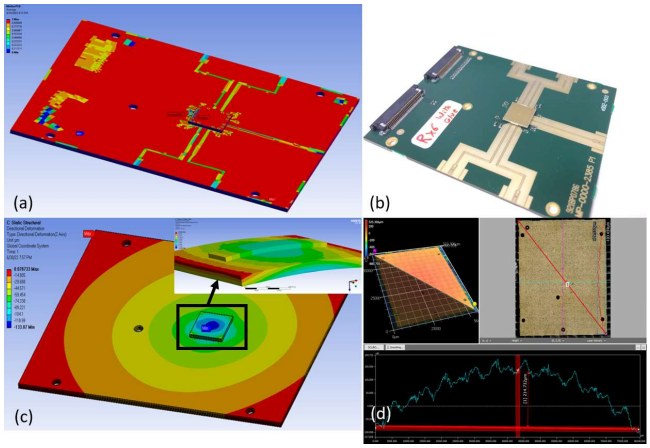

Fig. 7 The simulation and the measurement of the package warpage. (a) is the full-scale finite element model and (b) is the assembled package. (c) is the simulated package board warpage and the mother board warpage, and (d) is the package backside warpage measurement.

the influence of the assembly processes regarding the Cu pillar solders and solder balls, namely the solder mask thickness and the chip thickness. Firstly, the solder mask thickness can effectively reduce the shear stress at the Cu pillar solder joints. On one hand, it contacts the chip and restrict the relative movement of the chip and the board, on the other hand, it can also constrain the solder from flowing around. So a thick solder mask will have positive influences on the mechanical stability of the Cu pillars. Secondly, the thickness of the chip, which can be controlled by post-process grinding, is also a critical factor. A thicker chip, although doesn't change the shear stresses on Cu pillars during the first assembly step, increases the tensile stress around 20% in the solder balls during the second assembly step.

Such a stress development assembly process is not only observatory in the finite element models, it can be characterized using bow measurements as well. Due to the large CTE mismatch in the first assembly step, the package board has already demonstrated large bow as is shown in Fig. 7. During the second assembly step, such a large bow is transferred to the mother board through solder balls, creating tensile stresses in the solder. A comparison between the simulated package warpage and the measured warpage is shown in Fig. 7. The simulated bow is 134 µm, while the measured bow is 215 µm, showing a deviation of around 81 µm. Considering the complexity of both the model and the assembly process, such a result is more than acceptable.

V. Conclusion

The assembly process of a Cu pillar based wafer level package is modelled with finite element methods. The stress development during the reflow process is analyzed in details. The Cu pillar solder shear stresses, together with the solder ball tensile stresses are observed to be the critical points during the package assembly.

During the first assembly step, the chip is flipped onto the package board, and Cu pillars suffer from the shear stress after the reflow process. By controlling the solder mask thickness, the shear stress at the Cu pillar developed during the assembly can be largely reduced to less than 30% of its original value.

During the second assembly step, the mother board is forced to warp together with the warping of the package PCB, developing tensile stress in the solder balls. Assembling with thinner chips can effectively alleviate this tensile stress. Additionally, the package warpage resulted from the second assembly step is characterized by both the simulation and the measurement. The deviation is 81 µm, validating the accuracy of the modelling and paving the way for further packaging investigations.

Acknowledgment

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