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An Advanced Finite Element Model of the Cu Pillar Solder Reflow Assembly

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Abstract

The recently emerged Cu pillar technology has drawn a lot of attention in the wafer-level packaging field due to its fine pitch and superior electrical performances. Flip-chipping Cu pillar dies to low-cost PCBs is considered a promising and cost-effective packaging approach. This paper focuses on developing a thermal-mechanical finite element model to identify how different Cu pillar and board configurations impact Cu pillar shear stresses. Furthermore, this model extracts shear stresses from Cu pillar solders in various positions, providing valuable information about Cu pillar shear strengths when compared to the visual inspection results of the package's cross-section. This model is a significant step towards the further development and standardization of the Cu pillar flip-chip technology.

1. Introduction

The emerging of the Cu pillar was driven by the continuously shrinking pad pitch and the increasing I/O density. The C2 (Cu pillar with solder cap) solder mass reflow flip-chipping has drawn some attentions in the past few years. Compared with conventional solder bumps, the smaller solder volume facilitates a higher thermal and electrical conductivity, and reduces the needed area to accomodate the collapsed solder material. However, due to the miniaturization of the solder volume, the portion of the solder material and the intermetallic compound (IMC) will also change, leading to different mechanical properties [1] [2] [3]. Therefore, it's important to conduct a quantitative study to investigate the mechanical strength of the Cu pillars. On the other hand, the low-cost organic substrates, although being cost-effective, is rarely used as the Cu pillar flip-chip substrates. One of the reasons is the low mechanical stability caused by the large coefficient of thermal expansion (CTE) mismatch between the silicon (~3 ppm/°C) and the PCB (12-19 ppm/°C) [4] [5]. Driven by these factors, a thermo-mechanical finite element model is developed to characterize the shear stresses of the Cu pillar solder joints. The model takes the reflow process into consideration, exploiting a global-local method to correlate the solder shear stresses with its positions. Different Cu pillar and board configurations are compared and analyzed. Lastly, the cross sections of the Cu pillars at different positions are inspected and compared with the simulated stresses to extract the shear strength information.

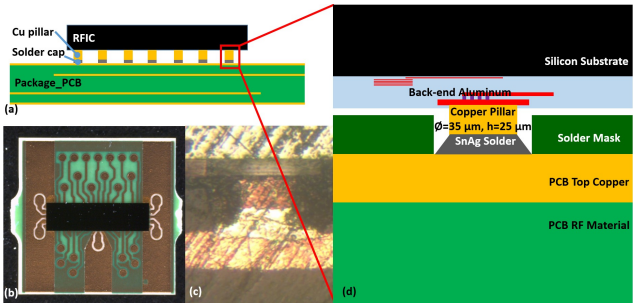

Fig. 1. The C2 flip-chip configuration. (a) is the schematic drawing of the package, (b) is the assembled package, (c) is the cross-section of the Cu pillar, and (d) is the schematic drawing of the assembled Cu pillar.

In this study, a comprehensive finite element model is developed to investigate the shear stresses of Cu pillar solder joints. It also provides valuable information on the mechanical strength of Cu pillars, which can aid in the further development and standardization of the Cu pillar flip-chip technology, and improve the reliability of integrated circuits.

2. Methodology

The components used for flip-chip assembly are a SiGe BiCMOS chip (1.2 mm x 5.3 mm x 0.3 mm) and a 4-layer Astra-MT77 PCB (50 mm x 50 mm x 1.6 mm). The Cu pillars are directly deposited on the passivation opening of the aluminum pads, and then capped with a 15 µm layer of SnAg solder. On the PCB side, solder mask defined (SMD) pads with the ENEPIG finishing are used. The pad pitch is controlled to be 250 µm, with an 80 µm spacing, 50 µm solder mask to copper clearance and a 65 µm solder mask opening. The solder mask is maintained at 15 µm to enable a good contact of the flipped solder bump. The specific dimensions of the Cu pillar is shown in Fig. 1.

The flip-chip is implemented using a mass reflow soldering process. After the solder flux is dipped to the tip of the solder cap, the alignment is made with a ± 3 µm accuracy. Then the whole package is placed in the reflow oven for flip-chip assembly. Due to the use of the Pb-free solder, the temperature has to go up to about 220 Celsius to reach the melting temperature. After the assembly, the samples are prepared for cross

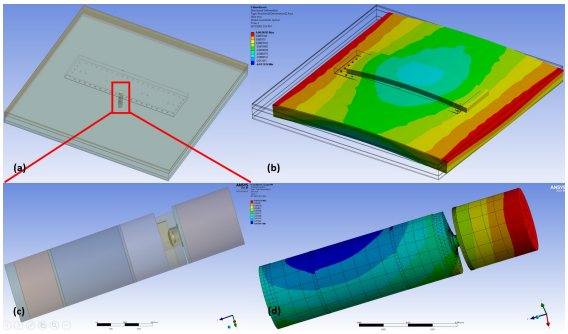

Fig. 2. The global-local modelling of the Cu pillar flip-chip. (a) and (b) are the global models of the package, (c) and (d) are the local models.

Table 1. Material properties used in the mechanical model

	Temperature (°C)	CTE (ppm/ ℃)	Young's modulus (Gpa)	Poisson ratio
Silicon chip	25	2.8	129.6	0.28
	150	3.1	128.4	0.28
solder (SnAg3.5)	25	22.4	50.7	0.4
	125	24.4	43.2	0.4
	200	25.9	37.6	0.4
PCB_substrate	-	x/y: 12	19.2	0.183
	-	z: 60		
solder mask	-	19	6.9	0.35
PCB_copper	-	16.9	125	0.31

section inspection. The packaged samples are molded in the epoxy and then fixed by a holder. The cross-sectioning is implemented by a from-coarse-to-fine grinding and polishing processes. During this process, the structures of soldered Cu pillars are unveiled, as is shown in Fig. 1 (c).

In order to accurately characterize the mechanical behaviors of the flip-chip package, all of the above assembly procedures are included in the finite element model. Specifically, the model is developed using ANSYS v2021r1 static structural module. The material properties used in the mechanical model are detailed in Table I [6] [7]. However, due to the large aspect ratio of the package's features – the Cu pillar pad thickness and solder are in µm range, while the size of the PCB substrate is in mm range. The number of elements required to achieve an adequate meshing is too large and will lead to a long iteration time. To handle this issue, the global-local method is exploited. As is shown in Fig. 2, the global model includes both the chip and the PCB, models the package-chip interaction during the reflow process. Then the local model is integrated into the global model, including all the detailed stack-up and pad information of one Cu pillar connection. The displacement information gathered from the global model is transferred to the local model as boundary conditions to ensure an accurate interpretation of the static stresses.

Specifically, in the global model, the chip and the PCB are modelled as rectangular blocks with a meshing size of 100 µm and 200 µm respectively. Small cylinders are used to represent the Cu pillar and solder joints. After the temperature rises above the melting point, the solder material will become liquid and form a joint between the chip and package. In this study, the package is assumed to be stress free at the melting point, and the stress starts to accumulate during the cooling process together with the solidification of the solder. The initial temperature is applied uniformly to all the bodies and is set to 230 ℃, and the final room temperature is set to 22 ℃. A ramped loading is specified to facilitate the convergence. Aside from the temperature loading, the position of the board also needs to be fixed to make the calculation of the board deformation easier. To achieve this, the four corner nodes are restrained from translational movements and are set free in all the rotational degrees of freedom at the same time to facilitate a free deformation of the package. Worth noticing, the trace information of the package board is directly mapped to the surface of the PCB body using the trace mapping technique. The copper trace information is assigned as material thermal conductivities to each corresponding meshing element, greatly reducing the number of elements and saving the modelling efforts. On the other hand, the local model only models one Cu pillar interconnection by considering a 100 µm radius cylinder at the Cu pillar position. The displacement results extracted from the global model are directly assigned to the cylinder side walls so that the Cu pillar interconnections experience the same stresses as they do in the global environment. The local model features a very fine meshing size to capture all the details of the Cu pillar interconnection, the element sizes for the solder and Cu pillars are specified to be around 5 µm. With this approach, the stress details corresponded to the Cu pillars at different positions can be accurately extracted by simply inputting different boundary conditions. As a result, the average shear stresses on the solder material given different global and local environments are characterized.

Although the finite element model is one of the most efficient approaches to characterize the mechanical behavior of a package, it cannot fully reflect every details of the real package due to the variation of the fabrication/ assembly processes. Some manufacturing tolerances have to be considered in the model as well. Specifically, in the local model, the solder shear stress variations regarding different Cu pillar heights, different Cu pillar diameters, different Cu pillar shape, different pad flatness, and different pad opening sizes are extracted for comparisons. These variations reflect the influences of the Cu pillar solder joints have on the solder shear stresses. And in the global model, both the copper structures on the PCB and the solder mask thickness are varied. All of the above variations show how much the solder stresses

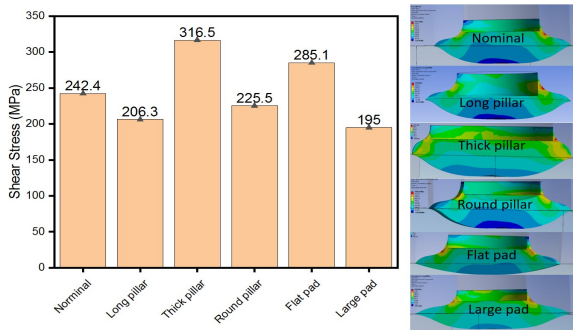

Fig. 3. The influences of the manufacturing variations in the local model.

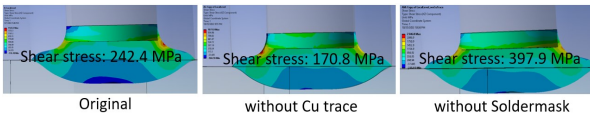

Fig. 4. The influences of the manufacturing variations for the global model.

can be influenced by the fabrication/ assembly variations.

3. Results and discussion

As described in the preceding section, the local and global models were utilized to examine the influence of Cu pillar configurations and PCB design on solder joint shear stresses. The Cu pillar configurations under investigation include variations in the length, diameter, and shape of the pillar. As laser drilling is used to form the solder mask opening, a small indentation on the PCB pad is frequently observed due to over-powered laser beam. Both the indentation depth on the pad and the opening size of the solder mask are both subjected to the laser power, they are also set as variables in the local model. The simulation results, presented in Fig. 3, demonstrate that alterations in the Cu pillar and pad configurations significantly impact the solder shear stresses. For instance, an increase of the pillar length by 5 µm results in a 14.9% decrease in shear stress, whereas increasing the pillar diameter to 50 µm raises the shear stress by 30.6%. Furthermore, rounding the pillar head results in a 7.0% reduction in shear stress, while a shallower indentation in the PCB pad results in a slight 17.6% increase in shear stress. In addition, a 10 µm increase in the solder mask opening results in a 19.6% decrease in shear stress. In summary, the different Cu pillar and pad configurations bring about variations in shear stress ranging from 10% to 30%. However, changes in the global model have a much more significant impact on solder joint shear stresses. For instance, the existence of copper traces causes a 20% change in the bow value, and eliminating the copper traces decreases the shear stress value at the chip corner by 29.5%. Furthermore, the solder mask plays a crucial role in the assembly process. Due to the small size of the Cu pillars, the solder mask acts as a

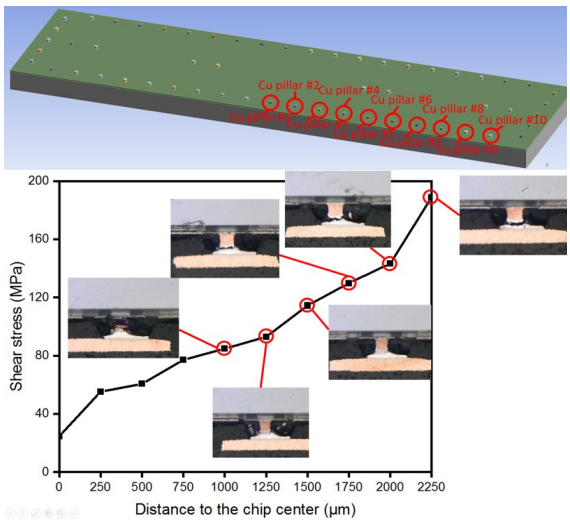

Fig. 5. The shear stresses extracted from solder joints located at different locations. The cross-sectioning of the corresponding Cu pillars are shown for comparison.

layer of underfill, buffering the interactions between the chip and the PCB. In the simulation, a thick solder mask leads to a 39.1% decrease in the solder joint shear stress. By comparing the shear stress variations between the local and global models, we observe that changes in the copper structures and solder mask have a much more significant impact on solder stresses than the Cu pillar and pad configurations.

The solder shear stress values shown in Fig. 3 and Fig. 4 are extracted from the solder joints located at the corner of the chip. In order to investigate the shear stress values at different positions, a series of solder joints were characterized. As illustrated in Fig. 5, the Cu pillars from #1 to #10 are aligned in a straight line from the center of the chip to the corner. Due to the coefficient of thermal expansion (CTE) mismatch, the different expansion rates between the chip and the PCB result in different displacements at different joints. The results show that the shear stresses are almost proportional to the distance from the chip center, with larger shear stresses observed further away from the center. At the corner of the chip, stress values reach the maximum 184 MPa. Although the shear strength is expected to increase with decreasing solder volume, this high stress value far exceeds documented solder shear strengths [7] [8], indicating that solder fractures are expected under such high shear stress. Consequently, cracks are observed in the cross-section inspection at the corresponding solder joint positions. The penetrating cracks appear from the solder joints located 1.75 mm away from the chip center, indicating a shear strength of approximately 120 MPa. This result is close to the 80 ± 10 MPa reported in the literature [8], taking into account the variations of different manufacturing parameters and modeling approaches.

4. Conclusions

In this paper, a comprehensive thermo-mechanical finite element model is developed to investigate the solder shear strengths during the flip-chip reflow soldering process. In total, two sub-models are exploited to investigate the influences from different aspects – the local model focuses on the interconnection details, characterizing the solder shear stresses resulted from different Cu pillar and pad configurations, while the global model is dedicated to characterizing the impacts of copper structures and solder mask on the solder shear stresses. It is found that the variation of the Cu pillar configuration brings 10 % - 30 % shear stress change in the local model, and the variation of the PCB brings 30 % - 40 % change. Obviously, the variations on the PCB level are more critical to the stability of the Cu pillar flip-chip package. Additionally, the shear stress values are closely related to the positions of the solder joints – they gradually increase as the interconnections get further away from the chip center. In our specific case, penetrating fractures appear after the distance exceeds 1.75 mm, corresponding to a shear stress of around 120 Mpa according to the developed finite element model.

With such a model, the risk of the Cu pillar flip-chip solder reflow can be minimized by defining its application scenarios, taking advantage of its low cost and high throughput benefits.

Acknowledgments

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