Characterization and optimization of the heat dissipation capability of a chip-on-board package using finite element methods

Zhibo Cao, Matteo Stocchi, Matthias Wietstruck, Thomas Mausolf, Corrado Carta, and Mehmet Kaynak

***Abstract*— The present study endeavors to investigate the thermal dissipation capability of a chip-on-board package by means of a comprehensive experimental and numerical analysis. For this purpose, a BiCMOS chip is designed and fabricated in conjunction with three different printed circuit board configurations, including a single-sided board, a thermal via board, and a copper frame board. Transient thermal measurements are carried out on all three packages, and the results are subsequently transformed into cumulative structure functions. Then the finite element models are established for each package configuration, and their validity is confirmed through comparison with the experimental structure functions. The models are then characterized in accordance with the JEDEC 38-set boundary conditions, followed by a series of optimizations targeted towards the printed circuit board, including the board stack-up and the board sizes. Parametric studies are performed to quantitatively assess the impact of these parameters on the thermal performance. Finally, the present study provides a comprehensive discussion of the optimal application scenarios for each board configuration, with a view to achieving good thermal performance. The findings of this study will contribute to the development of more thermally effective chip-on-board packages for high-performance electronic systems.**

***Index Terms*—thermal dissipation; finite element model; chip-on-board package; transient thermal measurement; structure function; PCB stack-up**

I. Introduction

As the semiconductor industry moves along Moore's Law or even towards "More than Moore", more functionalities will be integrated into the chips with even smaller sizes. Power density, therefore, continuously grows and heat dissipation becomes a challenging issue for package design. Especially for the systems operating at D-band (~140GHz) and above, the increase of power consumption due to the decreasing of amplifiers' efficiency at higher frequencies has inevitably led to thermal concerns. This makes heat dissipation a major issue for mm-Wave frontends regarding both wireless communications and radars.

The printed circuit boards (PCB), being the carrier of electronic components and the redistributor of the signals, play significant roles in the package thermal management. Due to the increasing power density and advancements in PCB technology, new features, such as copper coins, microchannels, and embedded components, appear to facilitate heat dissipation. [1] - [4]. But in practical application scenarios, there is no general solutions that can fulfill all the design requirements. Therefore, an accurate thermal model is of paramount importance. It can provide the necessary information for engineers and researchers, saving both time and effort in performing optimization and achieving good thermal performances.

The compact thermal model (CTM) is a good approach to model the package's thermal behavior. JEDEC proposed both a two-resistor model and the DELPHI model to facilitate a thorough analysis of the package [5]. Many other studies have also put significant efforts into CTM development [6]. Although the fast computing speed and simplicity of such models are advantageous, the flexibility and accuracy of the compact model are inferior to those of 3-D numerical models. In this study, 3-D finite element models are developed and calibrated by the measured cumulative structure function curves, further ensuring the accuracy of the structural information contained in the developed model. And by simplifying the model using the trace mapping technique, the computation time is limited to just 3-4 minutes. Therefore, both a high accuracy and an acceptable computing time are achieved using this model.

This study presents a comprehensive investigation of the thermal dissipation capabilities of chip-on-board packages using well-calibrated finite element models, shedding new light on the optimization of thermal performance in high-performance electronic systems. The optimization focuses on both the PCB stack-ups and the sizes, quantitatively analyzing the influence of each part under different boundary conditions. It is found that the thermal via can effectively conduct the heat to a heatsink or a cold plate, while presenting a much poorer

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Z. Cao, M. Stocchi, M. Wietstruck, T. Mausolf, C. Carta and M. Kaynak are with the IHP – Leibniz-Institut für innovative Mikroelektronik, 15236 Frankfurt Oder, Brandenburg, Germany (e-mail: cao@ihp-microelectronics.com)

C. Carta is also with Technische Universität Berlin, EN4, Einsteinufer 17, 10587 Berlin, Germany.

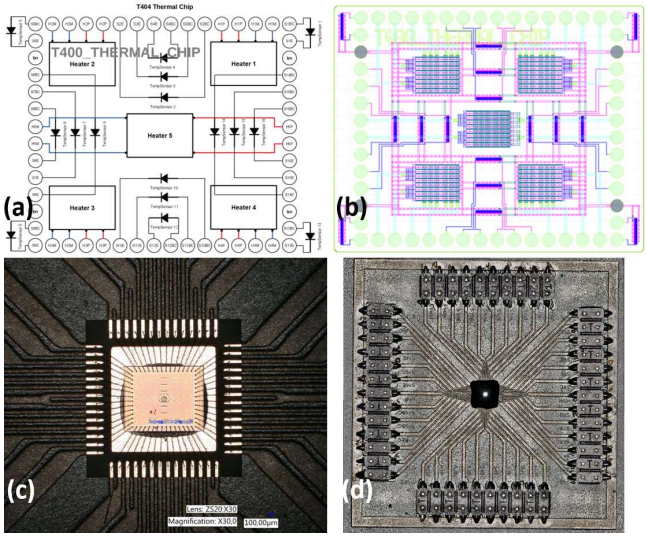

Fig. 1. The overview of the thermal chip and the package. (a) is the schematic view of the thermal chip, (b) is the GDS layout of the thermal chip, (c) is the top view of the assembled thermal chip under a laser microscope, and (d) is the top view of the whole package under the laser microscope.

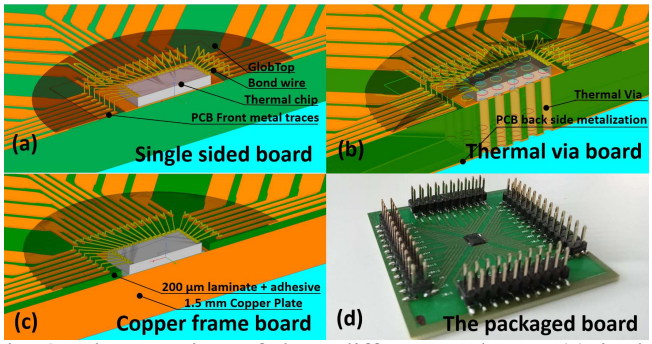

Fig. 2. The overview of three different packages. (a) is the cross-section sketch of the single-sided board, (b) is for thermal via board; (c) is for Copper frame board, and (d) is the picture of a fabricated sample.

performance under convection conditions. The thermal performances of multi-layer PCBs, on the other hand, although cannot dissipate the heat as efficiently as the thermal via boards, are less susceptible to the boundary conditions. With such a model and the results obtained in this study, the engineers and researchers can gain a deeper understanding of the thermal behavior of different structures in the PCB and customize the designs according to specific needs. The findings facilitate the development of more thermal efficient chip-on-board packages and contribute to the advancement of the field.

II. Thermal Characterization Methods of the Packages

The characterization is organized into two sections, namely the transient measurement of the packages, and the modeling of the packages. They validate each other and together enable a thorough understanding of the targeted package configuration.

A. The experimental setup

In order to characterize the heat dissipation capability of the PCB, a chip-on-board package is utilized. A BiCMOS chip based on IHP's SG13 technology is face-up mounted onto a

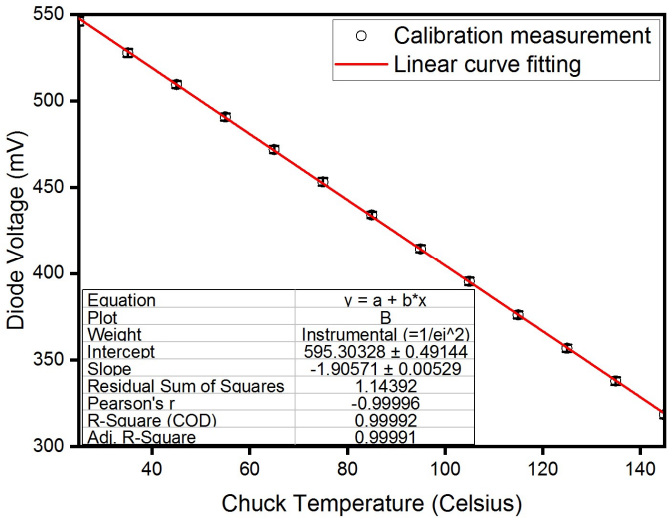

Fig. 3. The linear fitting of the calibration curve measured on temperature controlled cold plates. The slope indicates the temperature coefficient of the diode.

TABLE I
MATERIAL PROPERTIES USED IN THE SIMULATION

	Density (kg/m^3)	Thermal Conductivity (W/m K)	Specific Heat (J/kg K)
Silicon	2330	148	714
Copper	8933	380	385
FR4-R1755M	2000	0.57	930
GlobTop	1100	0.66	900
TIM	8500	2	550

PCB using thermal paste. Several PCBs with the same dimensions are manufactured using different stack-ups and technologies. A comparison of their thermal performances leads to a profound understanding of the thermal contributions made by different PCB structures.

The chip size is fixed to 1.935 mm x 2.42 mm x 0.3 mm, allowing for the accommodation of poly resistors as heat sources, thermal diodes as sensors, as well as the I/O pads to fan out all the signals. The on-chip pads are soldered with wire bonds to the PCB, and the pin headers are soldered on PCB pads to connect the boards to SMU. As illustrated in Fig. 1, the thermal chip schematic view and the package configuration are shown. The temperatures on the chip are measured through the thermal diodes. It is well-known that the diodes can be used for a wide variety of moderate-precision temperature sensing (± 0.8 °C [7]) because of their linear temperature coefficient. Temperature calibration of the sensors is carried out by controlling the package temperature using a thermal chuck. The chuck is integrated with a FormFactor 200 mm probe station system and utilizes the MicroVac technology to hold the packages with the vacuum. Additionally, the temperature control system is implemented by a CMI control unit from an ATT system. The calibration procedure is similar to the one that is stated in [8]. The chuck temperature is set from 25 to 145 Celsius with an interval of 10 degrees, and the diode voltages are extracted correspondingly with a fixed feeding current of 1 µA. With these data, the diode temperature coefficient is plotted

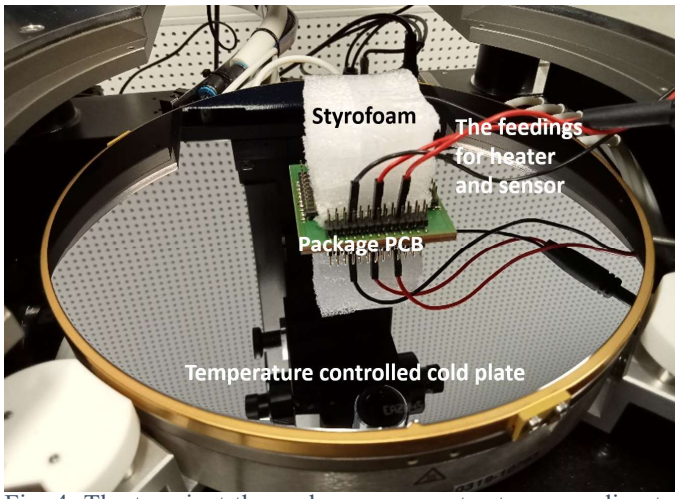

Fig. 4. The transient thermal measurement setup according to the JESD51-14.

in Fig. 3 with a slope of -1.906 ± 0.005 mV/°C, agreeing well with a typical value of -2 mV/°C reported by other studies [9].

While taking the PCB as the main heat dissipation path, the size of the board must be fixed as a baseline for the study. A 50 mm x 50 mm size is chosen to have enough space to fan out all the I/Os on the chip and to fit in the pin headers. Besides, the standard PCB thickness of 1.6 mm is picked as the target thickness value for the test board. Considering the standard PCB technologies, three different PCB configurations are prepared for heat dissipation comparison – the simple single-layer PCB, the board with thermal via, and the board with the copper frame technology. The above three configurations are listed in Fig. 2. The first board is a simple single-layer board, with only the 1 oz (35 µm) copper cladding on the front side to fan out signals. The core material is chosen to be R1755M from Panasonic to achieve higher thermal stability than conventional FR-4. The second board is a double-layer board, using densely arrayed thermal vias to dissipate the heat. The via diameter is 300 µm with a 25 µm thick copper wall plating. To ensure the best dissipation capability, The pitch is reduced to 500 µm, the technological limit, to maximize copper density and improve heat dissipation. The third board is designated to achieve the best heat dissipation configuration. Therefore, similar to the insulated metal substrate (IMS) technology, a 200 µm epoxy layer is attached to a 1.5 mm thick copper plate using a thin adhesive layer. A small window is cut in the middle of the epoxy to allow the chip to sit directly on the copper. Such a configuration ensures the optimum heat dissipation capability, and the fan-out of the signals is implemented on top of the epoxy layer. For all the boards, The chips are affixed to the PCBs using thermal conductive silver paste – the EN-4900 GC from the Hitachi group. Additionally, due to the vulnerability of the wire bonds, the Globtop encapsulation is applied to the packages by dam and fill. The Globtop G8345-6 from the NAMICS Europe GmbH is an epoxy-based liquid encapsulation material and, correspondingly, the G8345D is used as the dam material.

After the package is assembled, the next step is thermal characterization. The transient thermal behavior is measured to

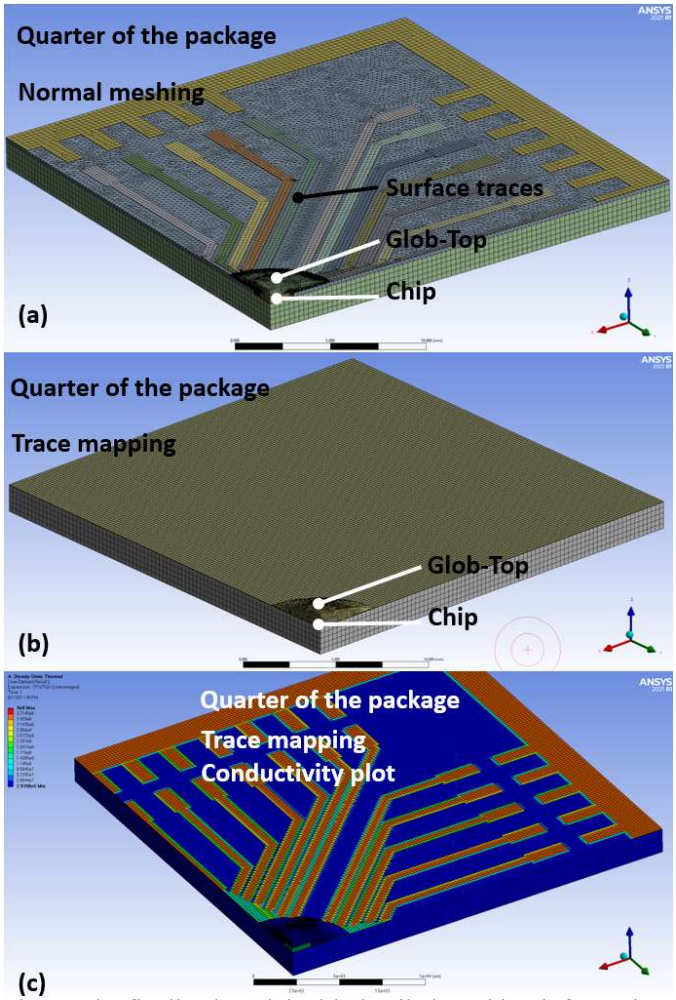

Fig. 5. The finalized model with detailed meshing information. (a) is the model with normal meshing, (b) is the model with trace mapping meshing, and (c) is the thermal conductivity plot of the model with trace mapping.

obtain structure functions of the designated packages. The structure functions contain not only the packages' thermal information, but include its structural information as well. A match between the model and measured structural functions indicates accuracy in both aspects. As shown in Fig. 4, both the heater and the sensor are fed by the B2901A Source/ Measure Unit (SMU) from Keysight. In order to fulfill the 50-points-per-decade rule specified by JESD51-14 [10], the sampling rate is set to 10 µs/ point (the fastest allowable sampling rate offered by B2901A) for the first 200 ms, and then switching to 1 ms/ point for 20 s, and lastly 100 ms/ point for 120 s. The measurement setup is established according to the recommendations from JESD51-14 (Fig. 4), a 5-cm thick Styrofoam is covered on top of the package to isolate it from the top surface dissipation. On top of this, 250 g weights are placed on top to fix the position of the package and minimize the contact thermal resistance as well. On the bottom, the package is placed on top of a temperature controlled cold plate with and without silver paste for comparison to extract the contact resistance values. The utilized silver conductive epoxy adhesive is #8330S from MG Chemicals. The input power is fixed to 1 W with a standard deviation of 8 µW for single sided

boards and thermal via boards, and 5 W for copper frame boards to have a better signal-to-noise ratio.

With the transient measurement results, the extraction of structure function is the next step. It can be extracted from either a heating curve or a cooling curve [11] [12]. In this study, the heaters and sensors are separated components, and no interactions between the heating and sensing need to be concerned. Thus the heating curve is favored for its simplicity. After obtaining the transient measurement of the different package configurations, the TDIM-Master is used to convert the time domain data to accumulative structure functions by deconvolution [13].

B. The simulation setup

Despite the experimental characterization, numerical models are developed as well to facilitate a better understanding of the package's thermal behaviors. In this study, the ANSYS 2021 R1 is used as the numerical analysis tool.

The cooling scheme can be roughly divided into two parts: internal and external heat conduction. Generally, numerical solvers use different approaches to tackle different problems. The finite volume method used by ANSYS Icepak is preferred to solve equations based on physical conservation laws (e.g. fluid dynamics), and the finite element method used by ANSYS structural is specialized in dealing with complex geometries. Since the external environment is strictly controlled in this measurement, it can be assumed to have uniform boundary conditions. Within this context, the fluid dynamics simulation is no longer needed, the focus of the model should be the structural details and dynamic heat conduction inside different bodies. Therefore, ANSYS transient thermal module is selected for model development

To establish a model, the general procedures are the development of the geometry, the input of material data, the adjustment of contacts between different domains, the meshing, and the assignment of the boundary constraints. All of them will be detailed in this section. Firstly, the materials are listed in

. Secondly, the meshing of the whole board structure is challenging due to the irregular bodies, such as the Globtop, wire bonds, metal traces. As for the Globtop, a tetrahedral meshing technique – independent patch, is good to handle such structures. And the cylindrical wire bonds are simplified to square rods with the same surface area to reduce the number of elements by around 10000 – a simple comparison shows such a simplification introduces less than 10% thermal performance variation, which is negligible considering the amount of heat going into the wire bonds only takes a small fraction.

As for the PCB, it is composed of copper, resin, glass fiber, and many other materials. Among them, copper has a much higher thermal conductivity, resulting in anisotropic heat conduction properties on the board. This requires the finite element model to capture the details of the copper structure, which is an arduous task by every means, and almost impossible for sophisticated boards. Therefore, the simplification of the model is imperative in both thermal and mechanical finite element modeling of the PCB. There are different simplification approaches, the most exploited method is taking the whole board as an equivalent uniform material [14], while others claim more accurate results by using trace mapping [15] [16]. In this study, trace mapping is implemented manually – a structured meshing is firstly generated on the PCB bodies, and based on the element size and position, the corresponding material property is averaged in each element. Compared with a conventional meshing with all the details, such a simplification reduces the total number of the element by around 25000 in this study, drastically improving the iteration speed. Worth noticing that unlike the trace mapping function embedded in the ANSYS thermal module, the exploited trace mapping method does not require netlist information from the PCB designers and is implemented manually using the fabrication files (e.g. Gerber file). The conductivity plot in Fig. 5 (c) ensures the validity of this approach.

TABLE II
THE COMPARISON OF THE THERMAL RESISTANCES BETWEEN THE CALCULATION AND SIMULATION

	Board resistance (calculated)	Chip resistance (calculated)	Junction-to-ambient resistance (simulated)
Single sided	150.3 K/W	0.9 K/W	51.2 K/W
Thermal via	9.5 K/W		18.5 K/W
Copper frame	0.4 K/W		2.4 K/W

Thirdly, based on the measurement setup explained in the previous section, the simulation setup and boundary conditions are determined. The bottom of the package is attached to a cold plate in the measurement – the bottom surface is fixed to a constant temperature in the simulation. The top of the package is covered with a thick foam – no heat dissipation is assumed from the top surface in the simulation. The side of the package is exposed to air – a 10 W/m^2K dissipation rate is applied to the side surfaces of the package in the simulation. And symmetric boundary conditions (thermal insulation surfaces) are exploited to represent the whole model with only a quarter section – greatly reduces the computation effort. In the analysis setting, the end time is specified as 120 s, and the auto time stepping is turned on. The minimum step size is set to 1 μs.

III. CHARACTERIZATION OF PACKAGE HEAT DISSIPATION CAPABILITIES

Using the approaches mentioned above, detailed finite element models can be developed based on the transient measurements. A good matching between the model and the extracted structure function ensures the accuracy of the model. And such a sophisticated 3-D model facilitates a comprehensive characterization of the thermal performance of the package.

A. The validation of the finite element model

Before going into details, An estimate of the thermal resistances of the package is obtained using analytical methods. Such a comparison serves as a rough validation of the developed finite element model.

The chip-on-board package allows for two principal directions of heat transfer (top and bottom). However, a 5 cm thick foam exploited in the measurement makes the top heat

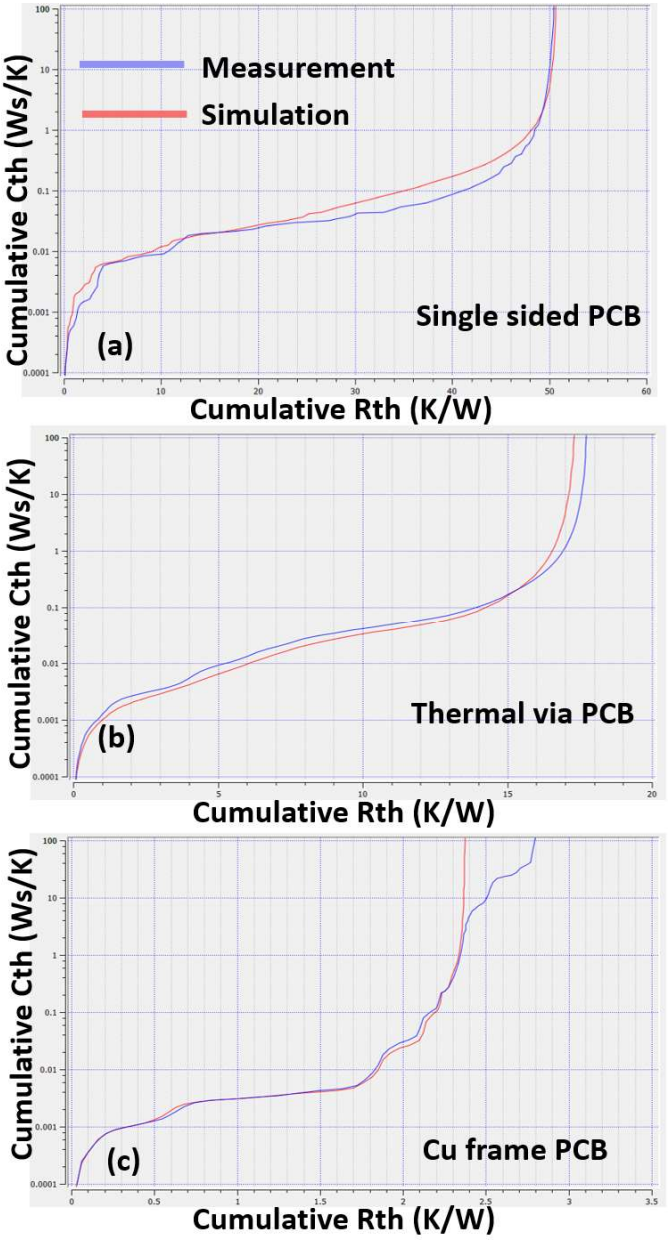

Fig. 6. The comparison of the cumulative structure functions extracted from the transient measurement and from the developed finite element models. All of the three fabricated package configurations are shown.

dissipation negligible, only the bottom heat path is analytically characterized. The main contributors on the bottom heat path are the chip, the thermal interface material (TIM), the PCB, and the contact resistance between the PCB and the cold plate. Among them, the resistances of the chip and PCB are extracted and listed in Table II. Using the analytical model developed by Ellison et al. [17], the spreading resistances of the chip, the single sided board, and the copper frame are obtained. The resistance of the thermal via configuration is calculated using the 210 K/W resistance of a single via provided by the manufacturer. Comparing the calculated values with the ones from the simulation, it is found that both the thermal via and the single sided PCB deviates away from the prediction. Two possible reasons are identified: 1) The heat spreading effects of

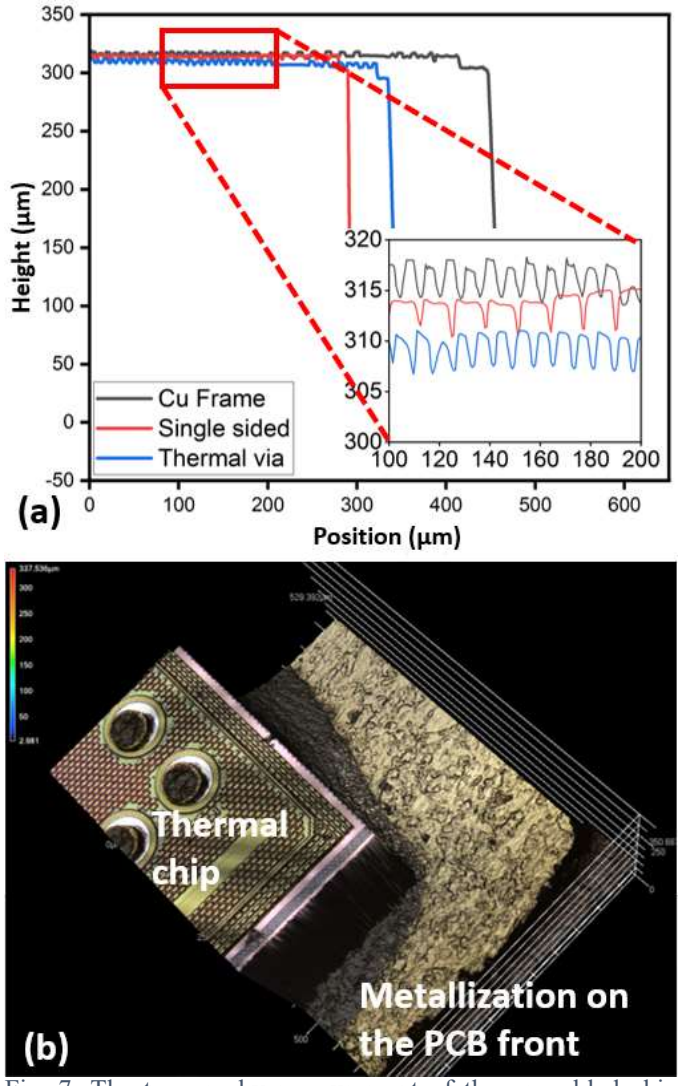

Fig. 7. The topography measurement of the assembled chip using the laser scanning microscope. (a) is the chip + TIM height measurement, and (b) is the scanned 3D image of the chip-on-board package, only the corner of the chip is shown.

the surface copper traces are challenging to account for in the calculation, resulting in an overestimation of the board resistance, and 2) Not all thermal vias are fully engaged in thermal conduction due to the limited area of the chip. To conclude, the analytical approaches, although can provide fast solutions, have very limited accuracies compared with finite element models in dealing with complex packaging configurations. However, such a pre-analysis is also valuable in providing overviews of the packages' thermal performances.

The development of the finite element models begins with the transient measurements, which contain comprehensive information both from the thermal aspect and the structural aspect of the packages. The revealing of the implicit structural information hidden in the transient curve is the key step to incorporating all the necessary information into the thermal model. The structure functions are well-suited for this task. They contain all the thermal and structural information of the transient measurements and are clear enough to be directly interpreted in the finite element thermal models. Fig. 6 shows

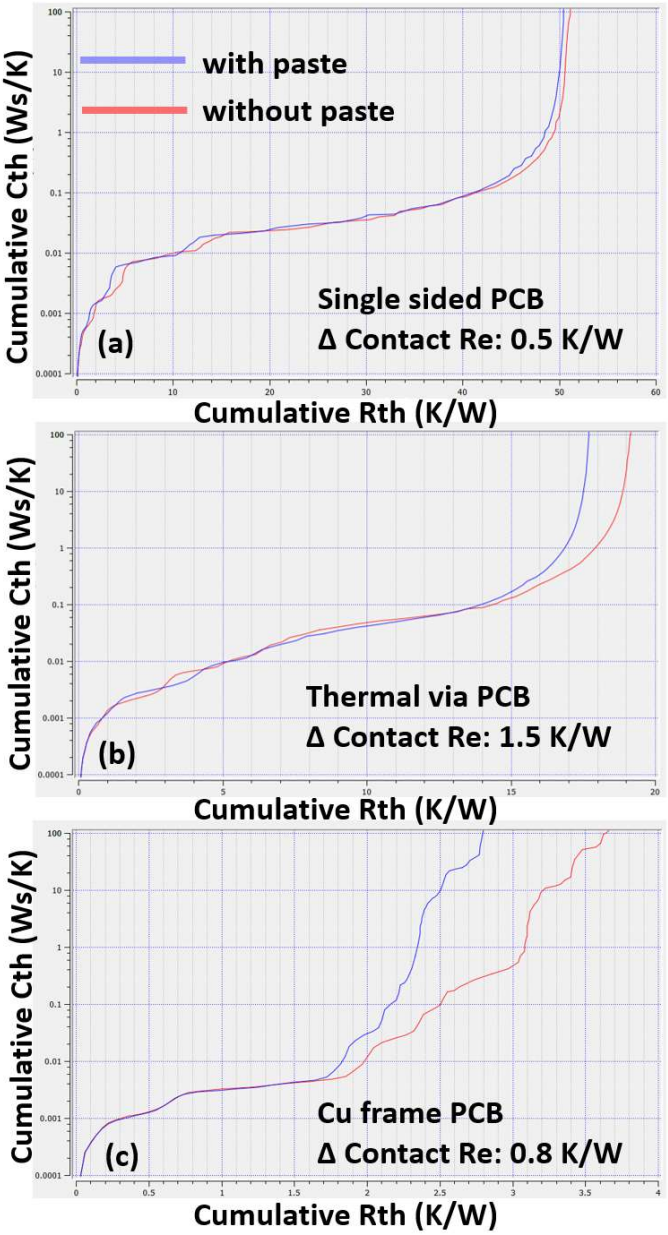

Fig. 8. The contact resistance measurement using the structure functions. The difference between the two measurements with and without the paste is considered as the PCB-to-cold plate contact resistance.

the comparison between the simulation and measurement results. A relatively good match is observed between the simulation and measurement results, indicating that the developed finite element models capture most of the thermal characteristics of the fabricated package. Such a result ensures the accuracies of the package dimensions, material properties and the boundary conditions within the model.

During the model development, most of the information can be easily obtained from the fabrication files or datasheet. However, the assembly of the package has to be performed manually and variations are inherently inevitable. Specifically, the TIM between the chip and the PCB, as well as the contact resistances between the PCB and the cold plate, pose challenges to the model development. To tackle these problems, additional measurements are carried out to fulfill these gaps. Firstly, the

TABLE III
THE CHARACTERIZATION OF THE FABRICATED THREE CHIP-ON-BOARD PACKAGES USING DIFFERENT BOUNDARY CONDITIONS

	Boundary conditions (W/mK)			Junction temperature (Celsius)		
	Top	Bottom	Side	Single sided	Thermal via	Copper frame
Forced convection	*100*	*100*	*100*	82.4	51.3	30.1
	100	*1*	*100*	88.6	54.7	31.8
	1	*100*	*100*	95.3	54.8	31.7
	200	*200*	*200*	75.3	48.7	29.1
	50	*50*	*50*	90.7	54.4	31.9
	10	*100*	*10*	93.3	54.3	31.8
	100	*10*	*10*	87.6	54.3	31.9
Free convection	*10*	*10*	*10*	118.6	70.8	46.8
	30	*30*	*30*	97.7	57.6	34.4
Heatsink	*10*	*500*	*10*	83.2	48.5	28.9
	10	*1000*	*10*	81.0	46.5	28.5
Cold plate	*10*	*10000*	*10*	78.5	40.7	28.0
	1	*10000*	*1*	79.0	40.7	28.0
Fluid bath	*1.00E+09*	*1.00E+09*	*1.00E+09*	52.7	35.5	27.6
	10000	*10000*	*10000*	54.5	38.4	28.0
	1000	*1000*	*1000*	62.6	43.5	28.3
	500	*500*	*500*	67.4	45.7	28.5

thermal impedance of the TIM is largely dependent on the material thicknesses, which can be directly measured. The laser profilometry in Fig. 7 shows that the TIM thickness varies from 5 to 15 μm, corresponding to 2.5 – 7.5 $mm^2 \cdot K/W$. On the other hand, taking the JESD51-14 as a reference, the PCB-to-cold plate contact resistances are extracted by comparing the measured resistance values with and without silver paste while attaching the package to the cold plate. The results shown in Fig. 8 indicate that the thermal via package suffers most from the contact resistance due to the concentrated heat flow. The extraction of both interface resistances enhances the accuracy of the designated model.

Despite the good matching between the simulation and measurement, it is crucial to take into account the uncertainties to enhance the model's applicability. The measurement uncertainties arise from both the diode voltage measurement and the conversion from measured voltages to temperature values. Although the voltage measurement by SMU has a precision of 1 μV, the achievable precision is only around 0.4 mV (the standard deviation is 0.38 mV extracted from one of the measurements) due to the output voltage oscillation. Additionally, the standard deviation of the diodes' temperature coefficient is 0.005 (Fig. 3). Based on the propagation of the uncertainty, the standard deviation of the derived temperature values is thus calculated to be 0.7-0.8 Celsius within the temperature range of 25-70 Celsius. This inherent uncertainty is believed to have a limited impact (< 10%) once the measured temperature exceeds 35 Celsius.

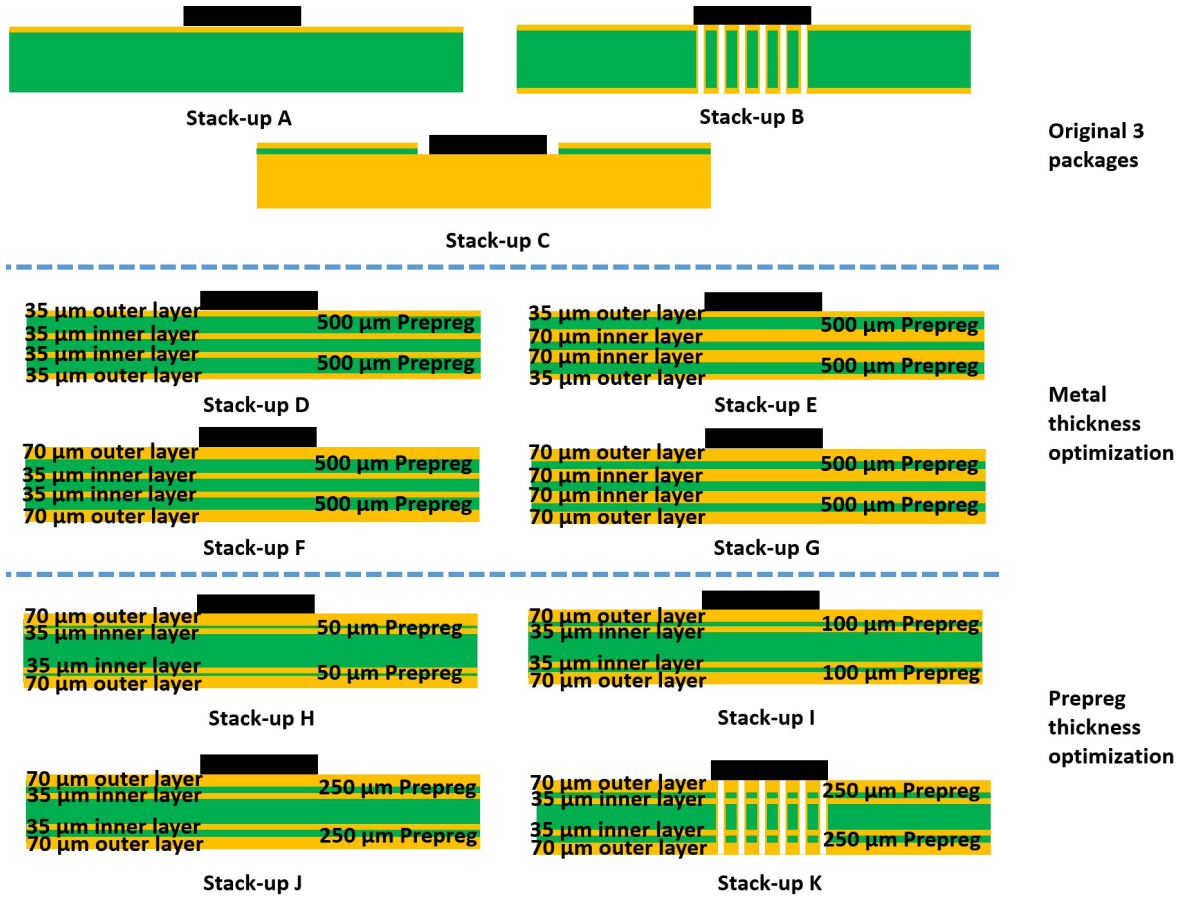

Fig. 9. The variations of stack-ups used in the developed finite element model to study the heat dissipation capability of the package under different boundary conditions.

B. The thermal performance characterization

With the models ready, the thermal performance of the packages can be easily characterized. The characterization is implemented using JEDEC's 38-set boundary conditions [5] to obtain an overview of the package's behaviors in different application scenarios. However, since the leads (corresponding to wire bonds) are protected by GlobTop, only three variables are available for boundary condition assignment, namely, the top, the bottom, and the side. Besides, the top side of the designated package cannot be attached to a heatsink or a cold plate. Consequently, only a subset of 16 boundary conditions is exploited to characterize the thermal performance of the designated packages. The simulation results using the developed models are listed in Table III.

From the results in Table III, the Cu frame package provides good thermal performances in all conditions, the thermal via package behaves well in almost all cases except for the natural convection, which drastically increases the junction temperature by over 10 Celsius compared with most other scenarios due to the concentrated heat flow. But overall, the thermal via package has a good thermal performance with less than 30 K/W junction-to-ambient resistance. The single sided board, however, suffers a lot from its poor dissipation capability. a junction-to-ambient resistance of greater than 50 K/W is seen in almost all boundary conditions except for the fluid bath. And the heatsink/ cold plate attached to the package back side doesn't present significant advantages over the pure convection cases due to the high resistive heat path to the PCB bottom.

IV. Optimization of the Package Heat Dissipation Capabilities

Based on the previous analysis of the chip-on-board packages' thermal performances with regard to thermal contributions from different parts, a proper selection of the PCB technologies is critical considering different applications.

For extremely high power applications, such as LED drivers and electrical motor drivers, one of the best solutions is always the copper frame board – by attaching the chip directly to the copper structure and having the whole board as its dissipation area, the copper frame can easily achieve a thermal resistance of less than 1 K/W. Similar concepts can be found with different names, such as copper coins, copper inlay, and copper core. All of them insert a bulk of copper below the heated component to facilitate the heat spreading, yet they are also faced with similar problems – 1. Only a few manufacturers are able to do this, and the boards are usually much more expensive than standard PCB technologies (the unit price of the copper frame board is 4 times of the single sided board, and 3 times of the thermal via board in this specific case); 2. The distribution of the signals is influenced or restricted due to the presence of the bulk copper

TABLE IV
THE CHARACTERIZATION OF DIFFERENT PCB STACK-UPS USING DIFFERENT BOUNDARY CONDITIONS

	Boundary conditions (W/mK)			Junction temperature (Celsius)							
	Top	Bottom	Side	D	E	F	G	H	I	J	K
Forced convection	*100*	*100*	*100*	80.3	78.0	70.2	68.6	53.0	54.5	64.5	39.1
	100	*1*	*100*	82.3	79.8	72.0	70.4	55.5	55.9	65.9	41.3
	1	*100*	*100*	87.6	84.4	76.2	74.1	49.8	58.5	69.1	41.4
	200	*200*	*200*	76.5	74.6	67.2	65.9	54.0	52.5	62.1	37.8
	50	*50*	*50*	84.5	81.8	73.7	72.0	55.1	57.0	67.2	41.3
	10	*100*	*10*	86.9	83.8	75.6	73.6	52.9	58.2	68.7	41.3
	100	*10*	*10*	82.2	79.8	71.9	70.4	69.6	55.8	65.8	41.2
Free convection	*10*	*10*	*10*	105.9	102.7	94.4	92.4	56.8	72.6	83.1	56.5
	30	*30*	*30*	88.6	85.7	77.5	75.7	52.4	59.8	70.1	43.9
Heatsink	*10*	*500*	*10*	83.1	80.2	72.0	70.1	51.9	55.4	65.9	37.9
	10	*1000*	*10*	82.4	79.6	71.3	69.6	51.4	54.9	65.4	37.1
Cold plate	*10*	*10000*	*10*	81.5	79.0	70.7	69.0	51.5	54.4	64.9	35.1
	1	*10000*	*1*	81.9	79.4	71.0	69.3	41.7	54.6	65.1	35.1
Fluid bath	*1e9*	*1e9*	*1e9*	57.9	57.6	52.4	52.2	42.8	43.6	49.5	32.3
	10000	*10000*	*10000*	59.7	59.3	54.1	53.8	46.0	44.7	50.9	33.9
	1000	*1000*	*1000*	67.3	66.3	60.2	59.5	47.6	48.4	56.2	35.8
	500	*500*	*500*	71.2	69.9	63.2	62.3	51.6	50.1	58.8	36.6

beneath the component. Both of the above factors motivate the search for a more cost-effective solution without undermining its electrical performance. The developed finite element model offers a comprehensive understanding of the thermal impacts of different PCB structures, through two sections of analysis: the PCB stack-up and the board size. By using this information, the thermal performance of chip-on-board configurations can be optimized to meet the specific requirements of different applications.

A. The characterization of the PCB stack-up

The characterization using the developed finite element model starts from the stack-up, including the metal thicknesses, the prepreg thicknesses, and via configuration. The standard metal thicknesses used in PCB technology are 0.5 oz, 1 oz, and 2 oz (corresponding to 17.5 μm, 35 μm, and 70 μm respectively). And the typical prepreg types used in PCB are 106, 1080, 2116, and 7628 (corresponding to fabrication thicknesses of 38 μm, 64 μm, 97 μm, and 173 μm respectively). To achieve an overview of the influence of the thickness values, the stack-up of the high effective thermal conductivity test board from JESD51-7 [18] is exploited as the baseline for optimization. The total board thickness is fixed to 1.6 mm, with 4 copper layers. The prepreg thicknesses (the outer layer to inner layer spacing) are 0.5 mm on both sides.

The first variable is the metal thickness – in Table IV, 4-layer PCBs with different metal thicknesses are compared using the aforementioned 16-set boundary conditions. During this optimization, the prepreg thicknesses are fixed to 0.5 mm on both sides (Fig. 9 Stack-up D-G). The heat dissipation capabilities of 1 oz copper are compared with the 2 oz copper quantitatively, with the influence of inner and outer layers characterized separately. It is found that for the 4-layer stack-up characterized in this study, a 2 oz copper reduces the junction-to-ambient resistance by around 20% in most of the boundary conditions when compared with a 1 oz copper case. And the outer layers contribute over 85% of such an improvement.

On the other hand, the prepreg thicknesses also play important roles. Given a fixed substrate thickness of 1.6 mm, the prepreg thicknesses are varied to observe their influences on the packages. Considering the typical prepreg thicknesses, a starting point of 50 μm is practical. 100 μm and 200 μm are common values used in normal fabrication, and with a 500 μm prepreg, which can be realized by stacking several prepregs, the substrate is separated evenly by the metal layers. As a result, these four values are selected as the prepreg thicknesses to characterize. The corresponding stack-up drawings are also sketched in Fig. 9 (Stack-up H-J). Similarly, the stack-up of the JESD51-7 test board is used as the baseline. Like the exploitation of thicker metal layers, thinner prepregs effectively enhance the copper density close to the heat source region to improve the heat dissipation capabilities. It's worth noting that, given some specific boundary conditions, the 100 μm prepreg boards perform better than the 50 μm ones. The possible reason is that the heat is dissipated from the front or side surfaces instead of the bottom. But practically speaking, the prepregs less than 50 μm on a thick copper is rarely used due to bad isolations and large parasitic capacitances. Therefore, it is concluded that for most of the prepregs thicker than 100 μm, a thinner prepreg always leads to better thermal performances. Quantitatively speaking, in our specific stack-up, the average reduction of the junction-to-ambient resistances are 12.8%, 24.5%, and 7.7% when the prepreg thickness varies from 500 μm to 250 μm, from 250 μm to 100 μm, and from 100 μm to 50 μm, respectively. Within this context, a stack-up with 100 μm prepreg gives the best overall thermal performance.

Comparing the obtained results with the thermal via PCB

TABLE V
THE CHARACTERIZATION OF DIFFERENT PCB SIZES USING DIFFERENT BOUNDARY CONDITIONS

	Boundary conditions (W/mK)			Junction temperature for K board (Celsius)					
	Top	Bottom	Side	25x25 mm	35x35 mm	45x45 mm	55x55 mm	65x65 mm	75x75 mm
Forced convection	*100*	*100*	*100*	42.8	40.2	39.4	39.0	38.9	38.8
	100	*1*	*100*	49.2	44.0	41.9	40.9	40.4	40.1
	1	*100*	*100*	49.4	44.1	42.0	41.0	40.5	40.2
	200	*200*	*200*	39.2	38.1	37.9	37.8	37.8	37.8
	50	*50*	*50*	49.8	44.0	41.9	40.8	40.3	40.1
	10	*100*	*10*	50.5	44.2	41.9	40.8	40.3	40.1
	100	*10*	*10*	50.4	44.2	41.9	40.8	40.2	40.0
Free convection	*10*	*10*	*10*	105.4	73.7	60.4	53.6	49.7	47.4
	30	*30*	*30*	59.1	49.0	45.0	43.1	42.0	41.4
Heatsink	*10*	*500*	*10*	39.5	38.3	38.0	37.9	37.9	37.9
	10	*1000*	*10*	37.8	37.2	37.1	37.1	37.1	37.2
Cold plate	*10*	*10000*	*10*	35.1	35.0	35.1	35.1	35.1	35.1
	1	*10000*	*1*	35.1	35.1	35.1	35.1	35.1	35.1
Fluid bath	*1E+09*	*1E+09*	*1E+09*	32.2	32.3	32.3	32.3	32.3	32.4
	10000	*10000*	*10000*	33.8	33.8	33.8	33.9	33.9	33.9
	1000	*1000*	*1000*	35.7	35.7	35.8	35.8	35.8	35.8
	500	*500*	*500*	36.8	36.6	36.6	36.6	36.6	36.6

package, it is found that such a 4-layer stack-up is less susceptible to the change of the boundary conditions when compared with the thermal via configuration. The variations of the junction-to-ambient resistances regarding different boundary conditions are around 20% for all the 4-layer stack-ups, whereas 35% for thermal via configuration. Specifically, for most of the 4-layer stack-ups, the forced convection average junction temperature is similar to that of the heat sink and cold plate (1-2 Celsius difference in average), the thermal via presents 5.7 Celsius difference between forced convection and heatsink, as well as 6.8 Celsius between the heatsink and cold plate. On the other hand, the thermal via demonstrates an outstanding thermal performance while being attached to a heatsink or cold plate. Based on this observation, the combination of both the thermal via and the multi-layer can provide the package with good thermal performances at both pure convection cases and the heatsink attached cases. For comparisons, the thermal vias are incorporated with a 250 µm prepreg baseline stack-up for comparisons (Stack-up K). It outperforms all the other stack-ups (except for the Cu frame) given all the 16 boundary conditions characterized in this study. Therefore, this stack-up is exploited for further optimization.

B. The characterization of the PCB size

Aside from the PCB stack-up, the size of the package is another appealing aspect to investigate. Different sizes of the PCBs result in different dissipation areas, and are, therefore, directly correlated with the junction temperatures. Table V lists the junction temperatures of the K board given the size of the board as the variable. The influence of the board size is dependent on the boundary conditions. For the convection cases, the junction temperature decreases with the increase in the board size. The higher the convection coefficients are, the smaller the dissipation area is. In most of the forced convection cases, when the board size exceeds 35 x 35 mm, the junction temperature becomes less sensitive (~ 10% from 35 x 35 mm to 45 x 45 mm) to the enlarging of the board sizes. After exceeding 45 x 45 mm, the influence of the board size further decreases to under 5% per 10 mm increase in the board side length. In case of the free convection, the junction temperature is more dependent on the board size – even from 65 x 65 mm to 75 x 75 mm, the junction temperature decreases by 2 K/W in the 8th boundary condition set. The heatsink boundary conditions, on the other hand, are much less influenced by the board size. After the board exceeds 35 x 35 mm, not much change is observed by further increasing the board sizes. Similarly for the cold plate case, a 25 x 25 mm PCB is shown to be large enough to dissipate the heat. As a conclusion, to ensure the optimum thermal performance of the package with stack-up K, boards with different sizes should be given different boundary conditions – a board larger than 75 x 75 mm can be used in free convection, larger than 50 x 50 mm can be used in forced convection, larger than 35 x 35 mm can be used in heatsink cases, larger than 25 x 25 mm can be used in cold plate cases. If the board is even smaller, only a fluid bath can ensure good thermal performance.

After a thorough investigation from the thermal perspective, the last point to consider is the fabrication efforts. The copper frame is the most demanding technology among all the aforementioned boards. The cost of such a PCB is 3-4 times of the normal double sided boards, and not all vendors are capable of doing it. Additionally, it is limited in the number of redistribution layers due to the existence of a copper bulk. In contrast, the thermal via adds around 20% expense, the 2 oz copper is 10-20% more expensive than the 1 oz copper, and the price of a 4-layer board is usually twice of the double sided board. A good combination of them (e.g. stack-up K) can already make the designated PCB capable of handling most of the thermal conditions without extra cost for the thermal consideration. Meanwhile, the challenges for signal routing is largely minimized in case of a 4-layer board.

V. Conclusion

This study presents the development of advanced finite element thermal models for three chip-on-board package configurations. The models are based on structure functions extracted from transient thermal measurements and provide a comprehensive characterization of the packages' thermal performance under various boundary conditions. The calibrated models are used to analyze the impact of different structures on the chip-on-board packages' heat dissipation capabilities. This approach enhances our understanding of the thermal contributions made by different structures in the PCB and enables optimal thermal performance to be achieved in different application scenarios.

Specifically, three different PCBs, namely the single sided board, the thermal via board, and the copper frame board are fabricated, and corresponding structure functions are extracted from the transient thermal measurement to calibrate the finite element models. The developed models are then exploited for optimizing the stack-ups and sizes of the PCB to achieve better heat dissipation capabilities. In the investigation of the 4-layer PCB stack-ups, it is found that the junction-to-ambient resistance can be reduced by around 20% when increasing the 1 oz copper to 2 oz copper. And considering our specific stack-up, over 85% of such an improvement is contributed by the outer copper layers. Besides, the use of thin prepregs effectively increases the metal density in the region close to the heat source. The decrease of the prepreg thickness from 500 µm to 250 µm, from 250 µm to 100 µm, and from 100 µm to 50 µm effectively reduces the junction-to-ambient resistance by 12.8%, 24.5%, and 7.7% respectively, indicating that from a pure thermal perspective, a 100 µm prepreg is the most cost-effective choice. Aside from the stack-ups, the size of the PCB is investigated regarding their thermal impacts as well. It is found that the area needed by the board to dissipate the heat varies with the surface boundary conditions. Under high dissipation conditions (e.g. fluid bath and cold plate), even a 25 x 25 mm board can efficiently dissipate the heat; for the heatsink attached scenario, the board size has to be at least 35 x 35 mm; for the forced convection cases, the board size has to be larger than 50 x 50 mm; and for the free convection cases, the board size needs to be over 75 x 75 mm to get rid of the size effects.

The finite element model developed in this study, together with the investigation approach provides a comprehensive overview of the designated chip-on-board package's thermal performances, guiding the optimization of the thermal design and enabling the development of more efficient and reliable electronic devices. In essence, this study contributes to advancing the field of thermal management, paving the way for the development of even more innovative and sophisticated electronic devices in the future.

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