Double Cell Upsets Mitigation Through Triple Modular Redundancy

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Abstract: A triple modular redundancy (TMR) based design technique for double cell upsets (DCUs) mitigation is investigated in this paper. This technique adds three extra self-voter circuits into a traditional TMR structure to enable the enhanced error correction capability. Fault-injection simulations show that the soft error rate (SER) of the proposed technique is lower than 3% of that of TMR. The implementation of this proposed technique is compatible with the automatic digital design flow, and its applicability and performance are evaluated on an FIFO circuit.

Keywords: triple modular redundancy (TMR), double cell upsets (DCUs)

1. Introduction

As technology scales, the charge sharing induced multi-cell upsets (MCUs) have become a serious concern for the radiation effects mitigation of microelectronics [1], [2]. Researches show that both the direct charge collection and well-collapse source-injection can cause MCUs [3]. With the presence of MCUs, the traditional single-node upsets (SNUs) and single-cell upsets (SCUs) hardened techniques, e.g., the dual-interlocked storage cell (DICE) [4], could fail [5]. To maintain the hardening performance of those techniques, intentional node/cell separation is needed. The simulation research in [6] reveals that, in a 130 nm complementary metal-oxide semiconductor (CMOS) bulk technology, a 2 μm distance between transistors should be applied to avoid the charge sharing. The radiation test results in [7] show that, in 65 nm, the neutron-induced charge sharing in the form of single-event multiple transients (SEMTs) can only occur within a distance of 1.5 μm. These critical distance guidelines have instructed the developments [8]-[10] and evaluations [11]-[13] of several hardened storage elements. To harden sequential cells, one way is to adopt a hardened circuit topology, e.g., DICE, and apply the critical distance rule to layout the transistors carefully. Then this cell can be added into a standard cell library and instantiated in any circuits to enable radiation hardening. This type of method is popular, however, there are two main issues regarding it. First, due to the ever shrinking of feature size, spacing out transistors to avoid change sharing becomes less effective. The study in [14] reveals that, for 16 nm FinFET static random access memories (SRAMs), the change sharing induced MCUs can contribute about 75% of the overall soft error rate (SER). This tells that the charge cloud can easily cover multiple cells in advanced technologies and, as a result, spacing out transistors to a safe distance in a single cell can be difficult. Given that the technology shrinking is a major factor driving the evolution of digital systems including radiation hardened microelectronics, the issue mentioned above deserves more attention. Second, experimental characterizations of the hardening performance will be required first before any newly developed cells can be applied in a real project, and recursive work may be needed as well, which can introduce extra time-to-application and higher costs. Both these issues may encourage designers to look for other solutions other than custom-designing radiation hardened cells. It is noted that it is not uncommon to design radiation hardened systems without any hardened cells available. In those cases, designers can switch the hardening from circuit-level to system-level, and the majority voting based modular redundancy techniques, e.g., triple modular redundancy (TMR) [15], [16], are commonly considered and adopted. Unfortunately, modular redundancy methods also suffer from the charge sharing/MCUs issue, and it may be difficult to apply the critical distance guidelines for them, especially for those implemented through the automatic design flow, because:

1) It is the place-and-route (P&R) tool that determines the locations of sequential elements. The P&R process mainly tries to meet the timing, routing, and area requirements, while spacing out sensitive components is not a factor considered. As a result, some methods need to be developed to automatically identify all sequential cells that belong to the same modular redundancy units but are too close to each

other and then separate them to safe distances. However, it is not clear if such methods can be always effective, because moving around cells may cause routing difficulties, especially in areas that are already very congested.

2) The critical distance can vary from one technology to another. Therefore, it is probable that this distance of a specific technology is unknown to designers. This uncertainty may lead to i) too optimistic spacing that is still with MCUs risks, and ii) too pessimistic spacing that, because cells are separated too far away from each other, induces timing degradation and routing difficulties.

Because TMR is only SCUs tolerant but MCUs sensitive, the charge sharing issue may make this technique not a very safe solution in advanced technologies. To address this, more unhardened replicas can be added into a modular redundancy unit to increase the number of correctable errors. One example can be the quintuple modular redundancy (QMR) which uses five replicas to mitigate double errors in them. However, a non-ignorable problem of this brute force is its very high overhead. Over 400% area and power penalties of QMR can make this method unacceptable in many projects.

In this paper, we propose and study a TMR based design technique for double cell upsets (DCUs) mitigation. Its enhanced error correction capability is achieved by adding three more self-voter circuits into a traditional TMR structure. As will be discussed later, compared to the traditional TMR, the extra area costs induced by the proposed technique can be acceptable (around 36% on average). The implementation of the proposed technique is compatible with the digital design flow, and its applicability is evaluated on a first-in-first-out (FIFO) module.

The rest of this paper is organized as follows. Section 2 illustrates the proposed technique and its radiation hardening principle. Section 3 evaluates the applicability and costs of the proposed technique. This paper is concluded in Section 4.

2. Proposed technique

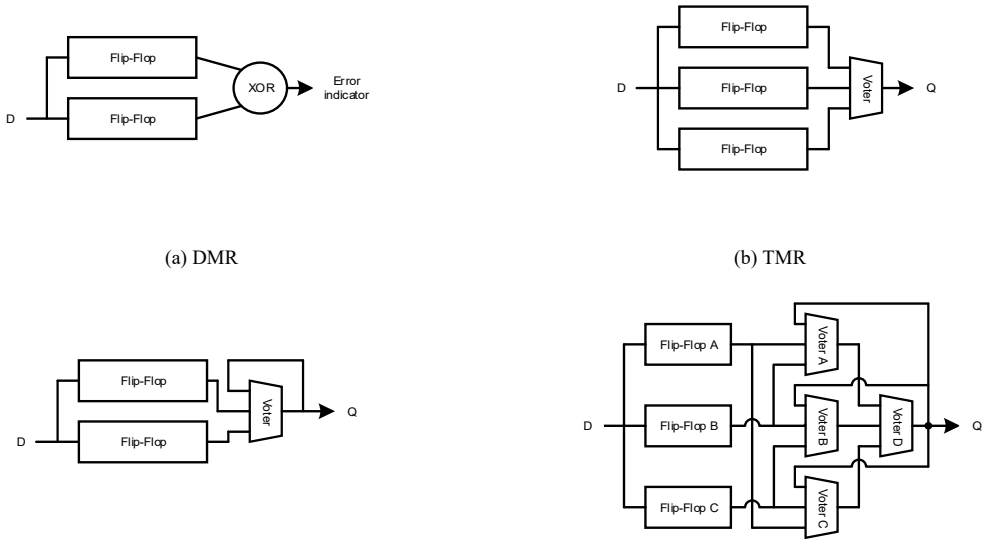


Fig.1. DMR (a), TMR (b), DMR with self-voter for error correction (c), and the proposed technique (d).

Before presenting the proposed technique, we first start from a review of other two well-known hardening techniques for sequential cells: the dual modular redundancy (DMR) [17], [18] for fault detection (Fig. 1. (a)) and TMR for error correction (Fig. 1. (b)). In a DMR structure, since only two redundant flip-flops are

used, the mismatch between their states can indicate the occurrence of an error at either one of them, but the DMR itself cannot identify which flip-flop is affected by an SCU. An exclusive-OR (XOR) gate can act as an error detector in a DMR, as shown in Fig. 1. (a), and its output can be used to trigger certain kinds of recovery schemes implemented. For a TMR structure, a same data is written into three identical flip-flops, and therefore, an SCU occurred at either one of them can be recognized and corrected through the majority voting process. The TMR voter circuit is simple and its logic function is O = AB+BC+AC. It is noted that, feeding a same data to only two of the three inputs of a TMR voter can change its output, no matter what the state of the third input is. This feature is utilized to realize a "self-voter" [18] circuit, as shown in Fig. 1. (c), to enable the error correction capability of a DMR. The output of the self-voter is connected back to one of its input, while the other two inputs are driven by two flip-flop replicas, respectively [17]-[19]. The same data hold by these two flip-flops can propagate through the voter and appear at its output and consequently the third input of the voter. When an SCU occurs at either one of the two flip-flops, this error cannot propagate since two out of the three inputs of the self-voter are still maintaining the correct states. As a result, the DMR system in Fig. 1. (c) obtains the SCUs mitigation capability, because the correct state, once established, is "memorized" by the self-voter itself. Another alternative to realize the DMR-based SCUs correction is called the design with Built-in Soft Error Resilience (BISER) [20]. BISER uses a C-element [21] to mask an upset at either one of the two precedent flip-flop replicas. This technique can be more cost-effective than TMR but needs custom-design implementation, because the C-element is a special logic gate that is commonly not available in a standard cell library. It is noted that TMR can also be realized at the block level. Compared to a simple flip-flop, each block replica can have a much larger sensitive area due to its complexity. Thus soft errors can affect different block replicas in different ways, e.g., particles hitting different parts and causing upsets at different flip-flops inside, which may make the outputs of the three block replicas totally different from each other and thus lead to meaningless majority voting. Therefore, block level TMR may not always be preferable.

Inspired by the DMR with self-voter structure in Fig. 1. (c), a TMR with self-voters technique is proposed in this paper, as depicted in Fig. 1. (d). As shown in this figure, the key point is that the output of the final stage Voter D is connected back to the inputs of internal Voter A, Voter B, and Voter C. The normal operation and SCUs/DCUs mitigation of this technique are described as follows.

2.1. Normal operation

The three redundant flip-flops in Fig. 1. (d) share the same input D. Once the same and correct data is sampled by them, this data will propagate to the following Voter A, Voter B, and Voter C. As analyzed above, the identical data at two inputs of each one of those voters can guarantee the correct outputs of those voters. Consequently, Voter D will see three identical inputs and then generate the corresponding output Q. This output, which is the same with the outputs of flip-flops, is fed back to Voter A, Voter B, and Voter C, making all inputs of those three voters identical. Therefore, the proposed structure can perform the normal functionality of a D-type flip-flop when no soft error occurs.

2.2. SCUs mitigation

The analysis of the SCUs mitigation of the proposed technique is relatively simple. An SCU occurred at any one of the three flip-flops will be seen and masked by two of the following three self-voters. For example, assuming that Flip-Flop A in Fig. 1. (d) has experienced an SCU, its incorrect output then propagates to Voter A and Voter C. Because the other two inputs of Voter A and Voter C remain their correct states, the SCU at Flip-Flop A will be blocked and the state of this flip-flop will be corrected in the next clock cycle. This is shown in Fig. 2. (a).

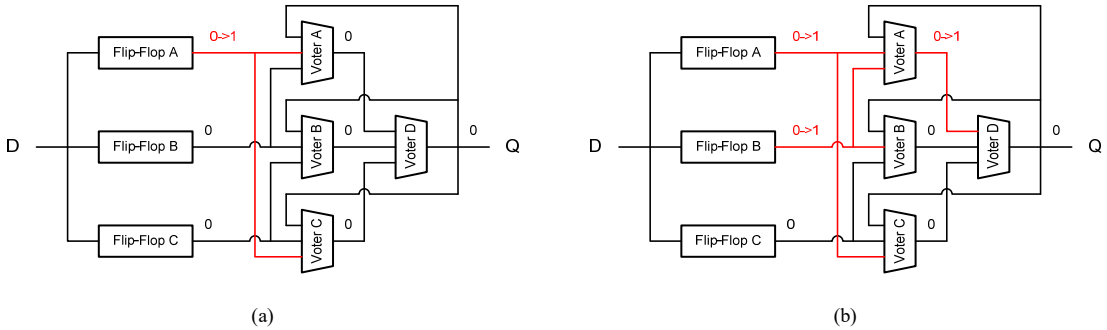


Fig.2. SCU (a) and DCUs (b) mitigations of the proposed method.

2.3. DCUs mitigation

The proposed technique in Fig. 1. (d) can provide DCUs mitigation capability. When any two of the three flip-flops get flipped, their errors can propagate through a following self-voter that these two affected flip-flops are both driving but will then be masked by the final stage Voter D. For example, let us assume that DCUs have occurred at Flip-Flop A and Flip-Flop B. The errors can propagate through Voter A and arrive at Voter D. However, the change of only one input of Voter D is not able to affect the final output Q. Because Flip-Flop C is still holding the correct state, the other two self-voters, Voter B and Voter C, will keep their correct outputs and ensure that Q is correct too. As a result, the upsets at Flip-Flop A and Flip-Flop B are blocked by the proposed technique. This is shown in Fig. 2. (b).

2.4. Fault-injection evaluation

The Verilog fault-injection (FI) simulations are performed to evaluate the soft error resilience of the proposed technique. For the comparison purpose, the regular, TMR, and QMR flip-flops are also involved. In the FI simulations, the groups of 1) 50 regular flip-flops, 2) 50 TMRs (150 regular flip-flops involved), 3) 50 QMRs (250 regular flip-flops involved), and 4) 50 proposed structures (150 regular flip-flops involved) are instantiated. The FI process in each clock cycle is as follows: 1) zeros are written into all regular flip-flops and regular flip-flops of hardened structures first to refresh their states; 2) N, 3N, 5N, and 3N different regular flip-flops in the regular, TMR, QMR, and the proposed structure groups are randomly selected and ones are injected into them to mimic soft errors; 3) the numbers of errors observed from the four groups are recorded and added into their total error amounts, respectively. The above FI process is repeated for 100,000 clock cycles, as shown in Fig. 3. It is noted that, compared to the regular group, 3×, 5×, and 3× flip-flops are used in the TMR, QMR, and proposed structure groups. Therefore, their injected upset numbers per cycle are also multiplied by 3, 5, and 3 to take the increased sensitive areas into account for fair comparisons. Here, N indicates the number of upsets occurred in every 50 flip-flops per cycle, and thus it can be considered as a term to describe the intensity of the FI.

Four FI simulations with different intensities (N=1~4) are carried out and the results are summarized in Table 1. As we can see in this table, TMR, QMR, and the proposed technique provide obvious SER reductions compared to the regular group. In all four simulations, the SERs of the proposed technique are significantly lower (< 3%) than those of TMR, which should be attributed to its DCUs resilience. The proposed technique also provides better hardening performance than QMR, because these two solutions are both SCUs/DCUs tolerant while the proposed technique has a smaller sensitive area (3 rather than 5 regular flip-flops used).

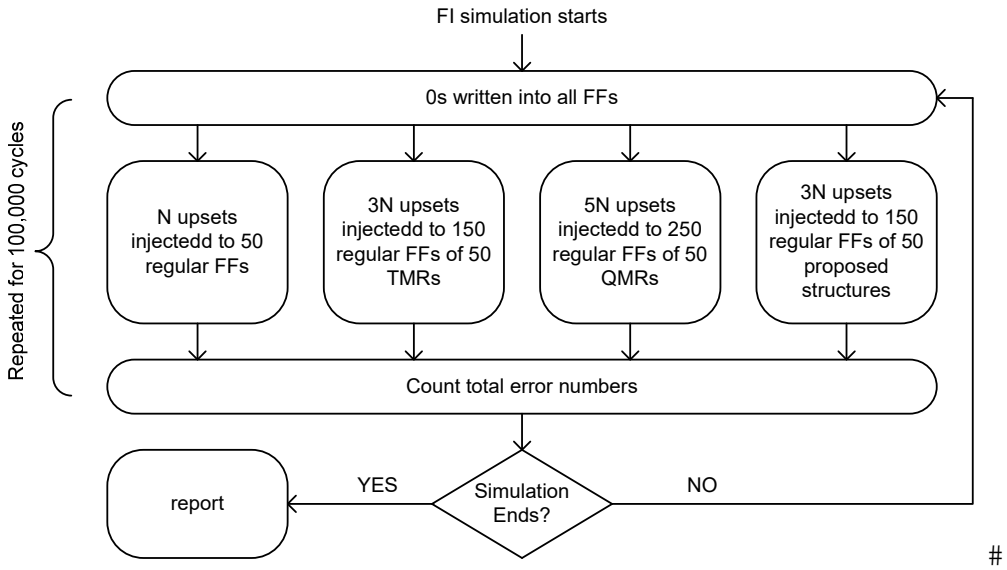


Fig. 3. Fault-injection simulation process.

Table 1. Fault-injection simulation results.

FI intensity N (upset #/50FFs/cycle)	Error #				SER_proposed / SER_TMR	SER_proposed / SER_QMR
	Regular	TMR	QMR	Proposed		
1	100,000	4,014	184	7	0.17%	3.80%
2	200,000	19,761	2,225	177	0.90%	7.96%
3	300,000	46,759	8,202	788	1.69%	9.61%
4	400,000	84,618	19,758	1,963	2.32%	9.94%

2.5. SET sensitivities of voters

Because more voter circuits are involved in the proposed technique, the single-event transient (SET) sensitivities of them need to be considered. The circuit topology shown in Fig. 1. (d) illustrates that an SET at the output of either one of Voter A, Voter B, and Voter C can be blocked by Voter D, however, SEMTs at those internal voters may propagate to the final output Q. An SET directly occurred at Voter D cannot change the outputs of the three internal voters but may propagate through its following combinational gates and get captured by flip-flops. Therefore, choosing a less SET sensitive voter circuit can help improve the overall resilience of the proposed technique. The heavy ion test results in [22] show that a voter built by NAND gates has the least SET sensitivity in 65 nm. Other radiation insensitive voter circuits [23], [24] developed before can also be considered.

3. Implementation

The proposed technique in Fig. 1. (d) can be implemented through custom-design. Although the SCUs and DCUs mitigation is guaranteed by its schematic, the critical distance guidelines (e.g., 2 μm) can still be applied in the layout design to avoid the triple cell upsets, which will further enhance its hardening capability. However, as discussed above, such a custom-designed cell needs to go through the experimental SER characterization first before its applications, which requires extra time and costs. In this paper, we mainly study the system-level implementation of the proposed method. As we can see in Fig. 1. (d), all components inside the proposed structure are available in any standard cell libraries. The regular flip-flops can be directly instantiated from a library, and the voter circuits can be constructed by using AO222 or other alternative gates. This suggests

that the proposed technique is compatible with the automatic digital design flow while some modifications are needed.

3.1. Cells constructions

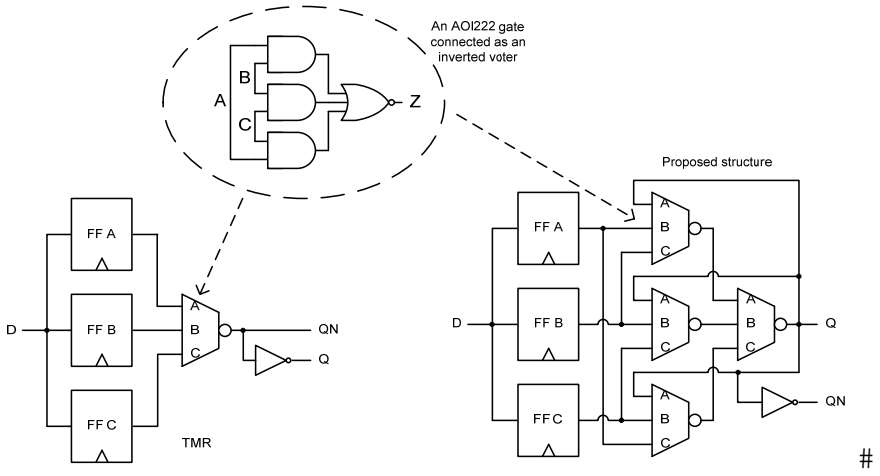


Fig. 4. Schematics of the voter, TMR, and the proposed structure.

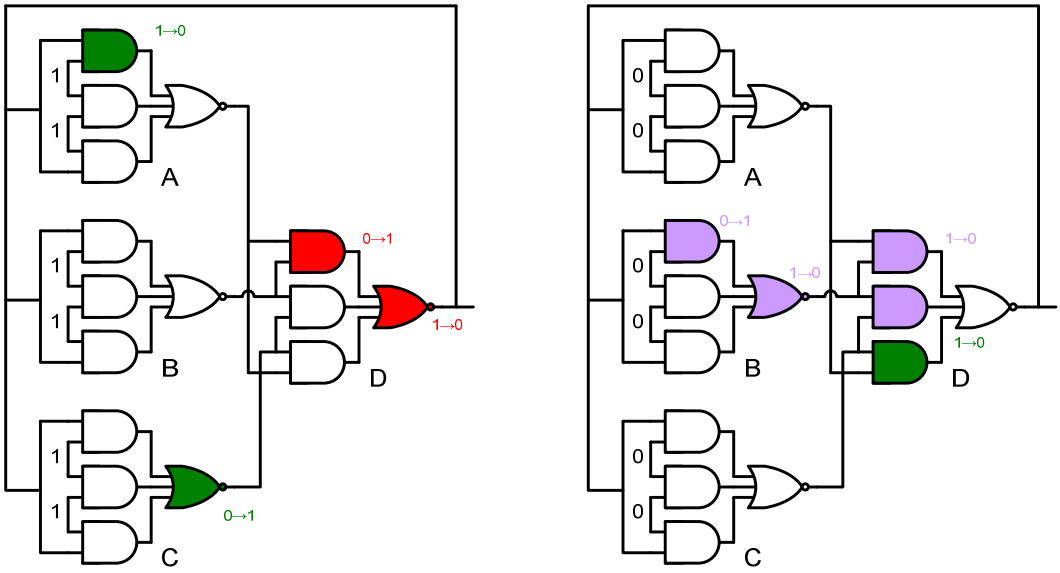
Table 2. Some of the available flip-flops in a commercial library and their areas of the regular, TMR, QMR, and the proposed technique versions.

Flip-Flop type	D-type	D-type with set	D-type with clear	D-type with set and clear
Area	1	1.20	1.15	1.35
Area of TMR	3.65	4.25	4.10	4.70
Area of QMR	7.85	8.85	8.60	9.60
Area of the proposed structure	5.15	5.75	5.60	6.20
Area_proposed / Area_TMR	1.41	1.35	1.37	1.32
Area_proposed / Area_QMR	0.66	0.65	0.65	0.65

In this paper, the applicability of the proposed technique is verified based on a commercial standard cell library. In this library, the AOI222 (And-Or-Invert) gate is available. Therefore, the exact schematics of TMR and the proposed technique can be built as what is shown in Fig. 4. The schematics in Fig. 4 are applicable for different types of flip-flops. Some of the available flip-flops of the library are listed in Table 2, and the areas of the regular flip-flops and their corresponding versions based on TMR, QMR, and the proposed technique are also given in this table (normalized to the area of the simplest D-type flip-flop). Compared to TMR, the ratios of area increasing of the proposed technique vary depending on the sequential elements to protect, and on average a 36% area increasing can be expected. One can also see in Table 2 that the proposed technique is more area effective than QMR in all cases. For QMR, besides the five flip-flop replicas, the complex voter circuit also contributes to the overall large areas.

It is noted that, in Fig.4, the logic gates used to construct the voters are radiation sensitive as well. Therefore, it is important to understand their sensitivities in the presence of particle strikes. This is discussed in two scenarios where all flip-flops are holding logic 1 (Fig.5(a)) and logic 0 (Fig.5(b)). In both scenarios, the SET at the final stage NOR gate of voter D may propagate through the following circuits and get captured. As a result,

this NOR gate is always considered as sensitive. In the first scenario, all AND gates of voters A, B, and C are not sensitive, because the negative SET at each of them cannot propagate through the following NOR gate. This is shown in Fig.5(a) by the AND gate colored in green of voter A. In this scenario, each of the NOR gates of voters A, B, and C are not sensitive either, because the positive SET will be block by voter D. This is shown in Fig.5(a) by the NOR gate colored in green of voter C. Any AND gate of voter D is sensitive, as its positive SET can travel through the following NOR gate and arrive at the output. This is shown in Fig.5(a) by the red AND and NOR gates of voter D. In the second scenario, any AND gate of voters A, B, and C are not sensitive. A positive SET at either of them can propagate through the following NOR gate and two AND gates of voter D, but it will then be blocked by the final stage NOR gate, as shown by purple gates in Fig.5(b). Similarly, any NOR gate of voters A, B, and C is not sensitive either. Any AND gate of voter D is not sensitive, because its negative SET will be blocked by the NOR gate, as shown by the green AND gate of voter D in Fig.5(b). Based on the analysis above, in the first scenario, all gates of voter D are radiation sensitive, while in the second scenario, only the last stage NOR gate of voter D is sensitive. This suggests that 1) making more registers (protected by the proposed scheme) staying in logic 0 may help improve the overall single event resilience and 2) selective SET hardening may only be needed for voter D.



(a) Logic 1 (b) Logic 0

Fig.5. Radiation sensitivities of voters

3.2. Design flow modification

The digital design flow needs to be modified to integrate the proposed technique. First, the gate-level Verilog netlist of the proposed structure for each type of flip-flop needs to be prepared. After the logic synthesis, all regular flip-flops instantiated in the synthesized netlist need to be replaced by their corresponding hardened netlists. Then the modified synthesized netlist can go through the P&R process, and the tool should be instructed to respect the hardened structures. The modified design flow is illustrated in Fig. 6.

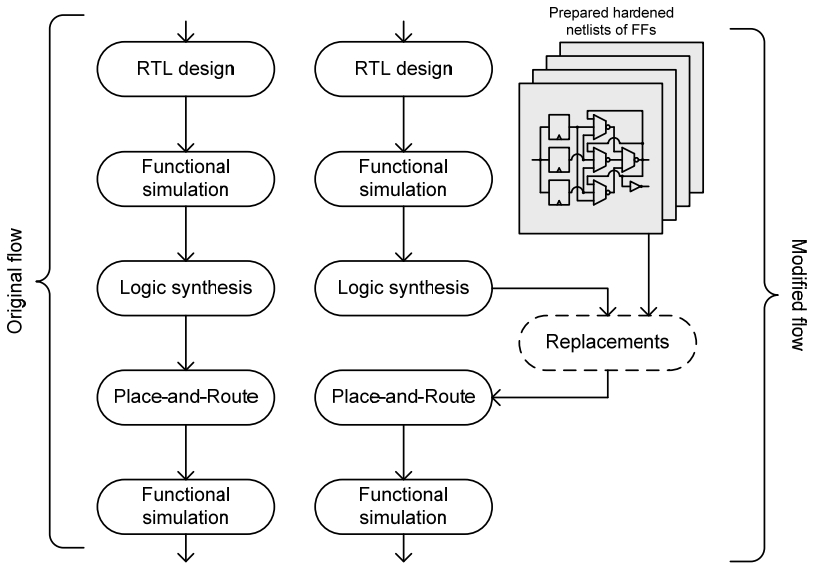
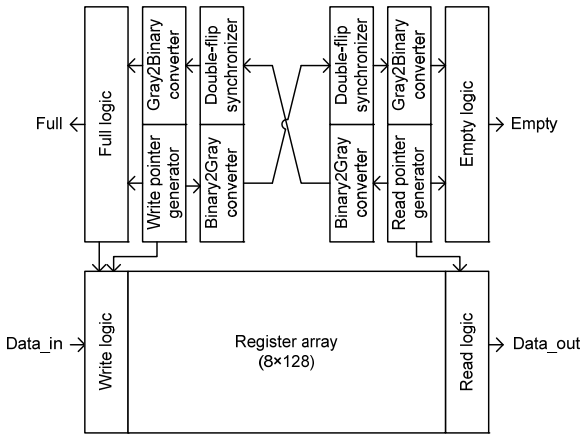


Fig. 6. Modified design flow for the proposed technique.

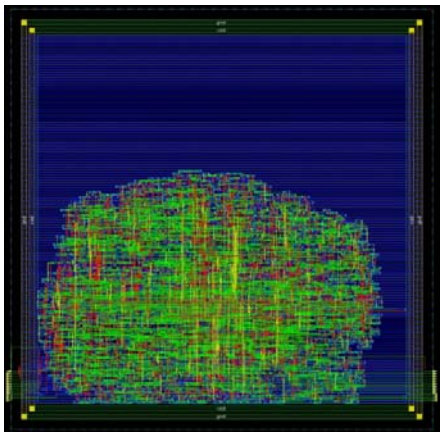
3.3. A case study

In this paper, an asynchronous first-in-first-out (FIFO) module is used as the example circuit to illustrate the applicability of the proposed technique. This FIFO circuit is designed for the SEPHY (Space Ethernet PHYsical layer transceiver) project [25], [26] and used to support data buffering and communication protocol conversions. The depth and width of this FIFO are configurable. This FIFO's structure is extracted from [27] and its structural diagram is shown in Fig. 7 (a).

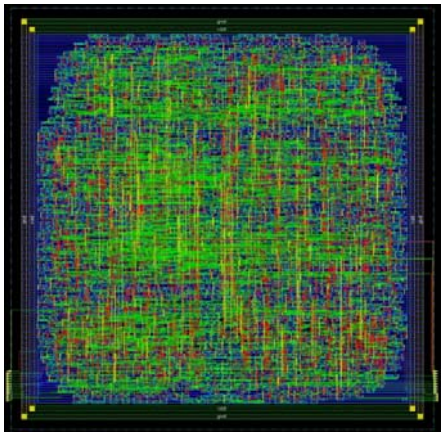
This FIFO module is described in fully synthesizable VHDL codes. After the synthesis, flip-flops will be used to realize the register array. In this case study, the width and depth of the FIFO are set as 8 and 128, respectively. So 8×128 = 1024 flip-flops are instantiated for the register array. The synthesized result tells that 1090 flip-flops in total are used, and the left 66 flip-flops are included in other submodules including the write/read pointer generators and synchronizers. This FIFO is implemented in three ways for comparison: 1) only using regular flip-flops, 2) only using TMR flip-flops, 3) only applying hardened flip-flops of the proposed structure. Cadence Encounter Digital Implementation System (EDI) is used for P&R. In the P&R, the same conditions (e.g., timing constraints, floorplan, power grid, I/O locations, etc.) are applied for these three versions and the result layouts are illustrated in Fig. 7. (b)-(d). After the P&R, the result netlists of the three versions all pass the functional post-layout simulations (delay annotated). The dumped signal waveform files from those simulations are then read back into EDI to perform the vector-based dynamic power analysis for the three versions.



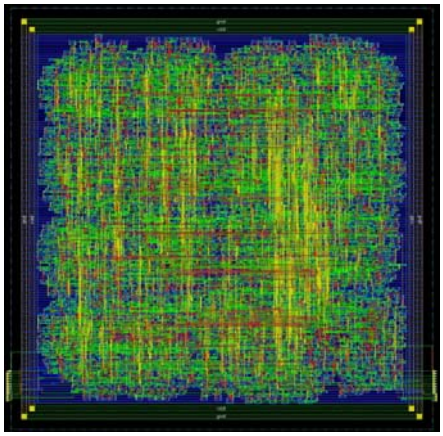
(a) Structural diagram



(b) Regular



(c) TMR



(d) Proposed

Fig. 7. Structural diagram (a) and P&R results of regular (b), TMR (c), and the proposed technique (d) versions of an FIFO.

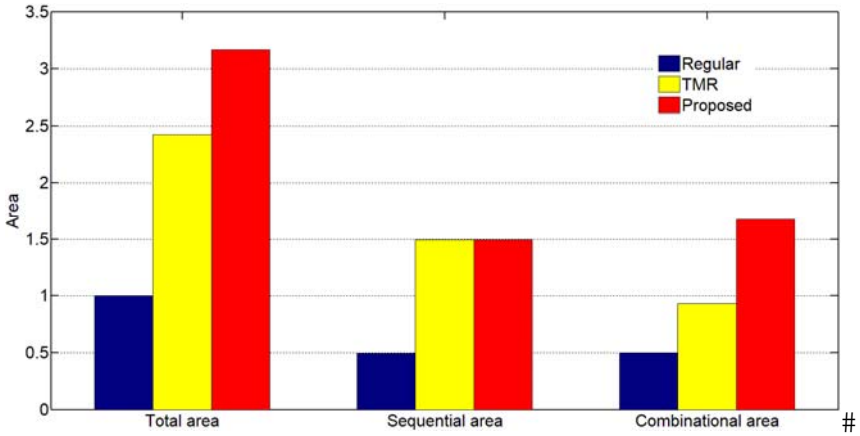


Fig. 8. Areas of the regular, TMR, and proposed technique versions of the FIFO. All data are normalized to the total area of the regular version.

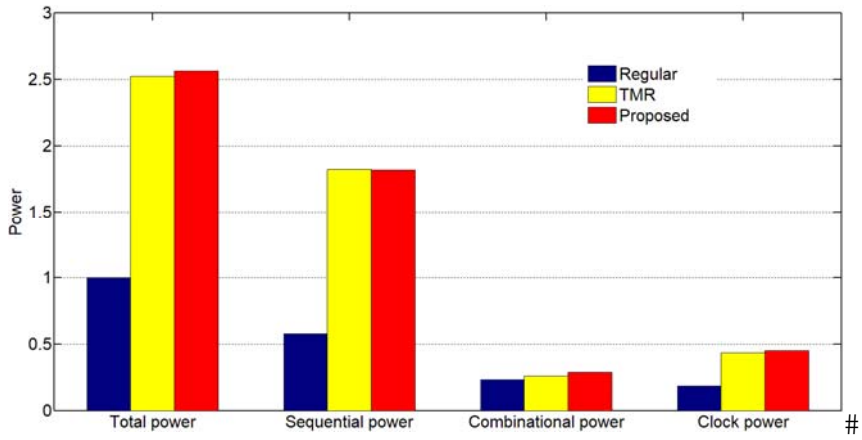


Fig. 9. Power consumptions of the regular, TMR, and proposed technique versions of the FIFO. All data are normalized to the total power of the regular version.

Areas of the three versions are depicted in Fig. 8. As one can see in this figure, the redundancies of TMR and the proposed technique introduce area overheads compared to the regular version (2.4× for TMR and 3.2× for the proposed technique). The sequential areas of the TMR and proposed technique are the same and 3 times of that of the regular version. The increases of the combinational areas of the two hardened versions should mainly come from the voters (one voter in each TMR cell and four in each proposed structure). The total area of the proposed technique is around 1/3 larger than that of TMR.

Power consumptions of the three solutions are shown in Fig. 9. Compared to the regular version, the power overheads of TMR and the proposed technique can be clearly seen. The sequential parts of these two solutions are the main contributors of the increased power. This is reasonable, since they both use 3× flip-flops inside. Their increased numbers of flip-flops also require more buffers to construct the clock trees, which consequently increase their clock switching related power, as shown in Fig. 9. Interestingly, in this case study, the power difference between TMR and the proposed technique is quite small. Actually, the proposed technique only consumes 1.6% higher total power than TMR. However, as we can see in Fig. 4, the proposed hardened structure of a single flip-flop uses three more voters than a TMR. These extra voters are expected to induce more data switching related power. The negligible power difference in this case study should be attributed to the operation of the FIFO. Although the FIFO possesses a register array consisted of 8×128 flip-flops, in each clock cycle, at most only 8 bits of the same address would have their states updated, while the other 8×127 flip-flops would have no data switching and only contribute the clocking related power. The flip-flops used in the write/read pointers and synchronizers can switch more frequently. However, they only form a very small part of the whole circuit (only 66 out of 1090 flip-flops are used in these submodules). Therefore, compared to TMR version, the FIFO implemented based on the proposed technique only has a very small portion of flip-flops in which the self-voters would induce extra data switching related power. This part of power is then inundated by the power from other major sources, including clock tree power, clocking related sequential power, and combinational power.

This case study verifies the applicability of the proposed technique and the design flow described in Section 3.2. The compatibility of the proposed technique with the digital design flow can enable high design efficiency and allow this technique to be developed into a soft error mitigation methodology for large scale systems.

4. Conclusion

A TMR based SCUs and DCUs mitigation design technique is investigated in this paper. Compared to the traditional TMR, three self-voter circuits are added into the proposed structure. The soft error mitigation

capability of the proposed technique is verified through fault-injection simulations and its superior hardening performance over TMR and QMR (at least 97% and 90% SER reductions achieved) is illustrated. The applicability of the system-level implementation of this technique is evaluated on an FIFO circuit. In this case study, it is shown that the proposed technique requires an area around 1/3 larger than that of TMR, while these two solutions consume almost the same power.

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