Considerations on the Design Methodology for an Integrated Gate Driver

Norbert Fiebig[1], Gunter Fischer[1], Pylyp Ostrovskyy[1], Dietmar Kissinger[1,2]
[1]IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany
[2]Technische Universität Berlin, Einsteinufer 17, 10587 Berlin, Germany
Email: fiebig@ihp-microelectronics.com

Abstract

Design considerations for a high-voltage output driver in a 0.13 µm 3.3 V BiCMOS technology are presented. The use of a stacked devices topology allows the driver to operate at three times the nominal supply voltage. Hot carrier degradation is reduced by operating within the voltage limits forced by the design rules. A design with only fully isolated transistors realizes negative supply domains which deliver a swing of -7.5 V with a peak current of 2.8 A at the switched output stage. Experiences during the different design phases are provided. Hints for using soft- and hardware, for the measurement and for the macro modelling are indicated.
Index Terms — Gate driver, CMOS integrated circuit, high-voltage techniques, methodology.

1 Introduction

In a world of demanding more and more energy, power electronics is the key technology to control the flow of electrical energy from the source to the load. Energy efficiency is one of the challenging tasks of today's power electronics. Distributed power supplies with a less number of conversion steps down from high-voltage AC and a final converter at the point-of-load (POL) deliver the power needed for a wide variety of applications. Non-isolated buck converters are widely used in such low-voltage POLs with output currents up to 10 amperes.

Multi-phase topologies combined with a smart control will enable optimized switching frequency, highest power density and lowest cost. The monolithic integration with CMOS leads to minimized parasitic inductances in the switching loop. Fig. 1 shows key components in the switching part of a buck converter.

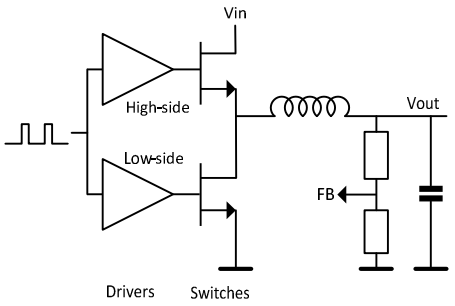

Figure 1 Simplified schematic of a buck converter output

For reasons of efficiency, modern switches are often built of an asymmetric GaN transistor pair with a larger low-side transistor. The optimization of the driver-switch combination therefore incorporates different designs in the low- and high-side branches of the gate driver.

This paper presents some aspects and considerations that appeared during the design phase of an integrated gate driver circuit for a 12-to-1-V DC-DC converter. Design tool configurations, measurement pitfalls, and model proposals are exemplarily demonstrated for the low-side driver section.

2 Gate Driver Design

2.1 Requirements

The design of the driver circuit is challenging mainly due to the properties of used GaN switches, the converter's operating frequency, and temperature dependencies. Our application uses depletion type GaN switches with a negative cut-off voltage of -7 V. The expected gate peak current was estimated to about 3 A. The operating frequency should reach 10 MHz.

In detail, the main challenges can be summarized as below:

- High swing on negative voltage potentials at the outputs
- Isolation of different negative and positive voltage domains on chip
- Fast transitions under determined timing constraints to reduce switching losses
- High peak current while having low quiescent currents

On the other side, a more research-oriented approach in order to prove the feasibility of using a standard-CMOS-

only concept has been followed. The circuit's high voltage and driver capability as well as the dynamic behavior should be evaluated. Such an approach is only known by academic publications so far [1], [2].

2.2 Technology and topology aspects

A large output swing of more than minus 7 volts has to be realized with a standard CMOS technology. Fig. 2 shows a typical breakdown characteristic of high-voltage (HV) NMOS transistors in our 0.13µm BiCMOS technology. A strong increase of the drain current appears for drain-source voltages larger than 4 V even for a short cut gate source.

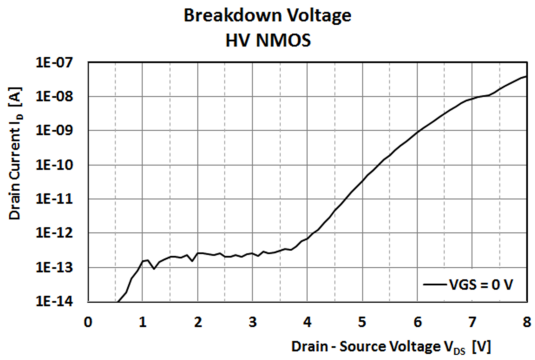

Figure 2 Typical breakdown characteristic of a HV NMOS transistor

Additionally, hot carrier injection (HCI) that occurs at higher voltages in small length transistors, reduces their life time as well as exceeding the breakdown voltages. Therefore transistors with a length of 0.5 µm are used and voltage drops of less than 3 V under operation across all terminals have to be guaranteed. A triple-stacked transistor approach in conjunction with the high voltage option (VDD = 3.3 V) of the 0.13 µm BiCMOS technology was chosen (Fig. 3).

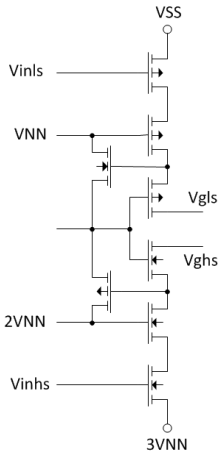

Figure 3 Triple-stacked output stage topology

A proper biasing paired with a smart level shifting provides for voltage drops smaller than 3 V across the terminals of each transistor used in the circuit. The upper- and lowermost transistors experience one voltage step (2.5 V) at their gates only. Unfortunately, in addition to VNN another two negative voltage supplies (2VNN, 3VNN) are required [1], [3], [4].

Since all NMOS transistors are working with negative voltages they need to be designed as isolated ones. By consistently using fully isolated voltage domains on chip with VSS as the floating reference against substrate, one can manage positive and negative supplies for the integrated circuits on one chip. Doing it this way it is furthermore possible to test this single driver chain also in bootstrapped supply mode as if it would be the high-side driver chain. A further integration of the controller functionality in standard CMOS is feasible as well.

2.3 Schematic design

After defining the technology used and the topology of the output stage from a perspective of the limits, the design of all circuit blocks started. Fig. 4 illustrates the building blocks of the low-side branch of the driver IC. It consists of tapered buffer stages in both branches, a level shifter in order to lower the input signal by two VNNs in the upper branch and the two complementary output stages.

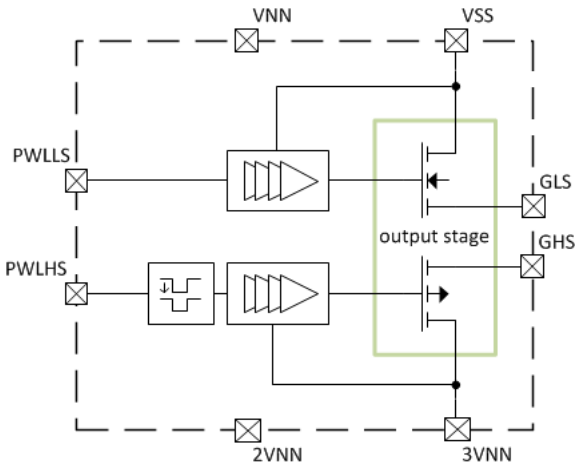

Figure 4 Low-side driver block diagram

Special care was taken of dimensioning the transistors in the output stage and its biasing circuitry for the ability to drive the peak gate current. Simulations were first done with the PDK models in order to prove the functionality of the developed circuits. The entire circuit was simulated in a temperature range from 0 to 125°C for application reasons.

The actual schematics of the circuit blocks in front of the output stage will not be discussed here in detail as they are state-of-the-art level shifter and buffer circuit designs. But let us consider some special circumstances in the

design of the output stage resulting from the peak current requirement and the stacked topology.

The NMOS part of the output stage includes three in series connected transistors each with 5120 gate fingers of 4 µm width in parallel in a separately isolated well. Because of the smaller mobility we need a two to three times larger PMOS transistor at the same current. Putting them together in the same well we have to take the body effect into account which increases the sizes of the two lower stacked PMOS transistors further. The PMOS transistors are sized by 16640, 25600, and 33280 gate fingers in parallel with the same width of 4 µm. It turned out that even with these larger dimensions in a common well the dynamic behavior was better than as having each PMOS transistor in its own well that has to be reloaded by the switching frequency.

As a result of simulations prior to parasitic extraction of the layout, the driver would operate up to 11 MHz at a duty cycle of 10% in a temperature range from 0 to 125°C. The output swing reaches almost -7.5 V at a peak current of about 2.8 A.

2.4 Layout

In order to achieve an evenly distribution of the currents within the individual transistors in the output stage we spent major effort in creating the layout. Multiple metal layer stacking in stripes on top of the MOS transistors regions combined with a meshed configuration of upper order traces care for a minimum of additional contact/via and interconnect resistances. The huge number of contacts to be connected with up to seven metal layers ended up in a complex layout pattern. Fig. 5 shows the layout of the low-side driver IC.

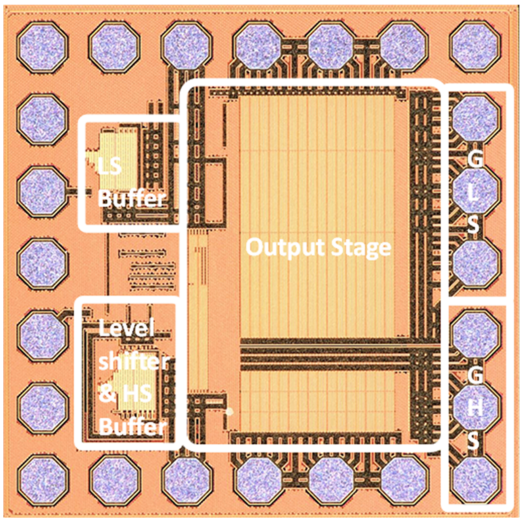

Figure 5 Layout of a low-side driver IC

The 2.1 by 2.1 mm^2 sized die is dominated by the output stage on the right half with the three NMOS transistors down. Three pads for each output distribute the current and reduce the series resistance.

2.5 Post layout extraction

Due to the complex metal structure in the output stage as explained in section 2.4, parasitic components of all kind affect the circuit performance. Therefore a parasitic extraction of the entire layout was executed. Depending on the chosen mode and options the size of the extracted netlist file spans from more than 2 gigabytes down to several hundreds of megabytes. Table 1 lists some file sizes for different options for our chip.

Usually, the file size has to be fitted to a convenient size in respect of the available hardware equipment and the kind of post layout simulations to be performed.

Table 1 Examples of extraction file sizes

Extraction parameters	File size of extracted netlist
RC only, default	2.1 GB
RC only, min R = 0.1, min C = 1f	540 MB
RC only, min R = 0.01, min C = 1f	725 MB

During the preparation of the simulation run a number of files with settings, options and netlist related data are created. Processing of all these simulation files, the interim produced operating point and result data blow up the memory requirements. The actual RAM size easily becomes a limiting factor in this game. That's why a reduction of the extracted netlist file to the minimum required accuracy rather than to the possible one is always a good method. Here are some simple steps one can go:

- Reduce the complexity of the extraction type from RLC to RC or R or C only depending on how seriously the different parasitic components impact the circuit performance.
- Omit layout regions for extraction that do not matter e.g. non connected pads, circuit blocks far away from the ones you want to observe.
- Coarsen the extracted components to an accuracy you can accept for your purpose.
- Try different extraction options for an optimum setting.

2.6 Post layout simulations

Post layout simulations can drive the requirements to hard and software up to their limits. A proper setup and adjustment of options helps to minimize trouble. Normally, it takes several iterations to find the optimum simulation conditions. Due to the huge file sizes it is wise to restrict the number of output data to a required minimum and to split different simulation types into separate runs. Working on servers helps for better distribution to a higher number of parallel processor

threads and usually having much more RAM available than on a single workstation. Additional reduction of the extracted netlist by the simulation software lowers the CPU times and memory usage (see Table 2).

Table 2 Used resources

	total CPU time	elapsed CPU time	used peak memory	Results folder size
HW1	aborted		>16 GB	
HW2	2:33 h	27:15min	8.6 GB	1.41 GB
HW3	1:57 h	24:21min	4.5 GB	0.92 GB

HW1: Local workstation, 4 CPUs, 16 GB RAM
HW2: Server with 32 CPUs (6 used on average), 128 GB RAM
HW3: as HW2 with additional parasitic reduction by software

Figure 6 proves the effect of this parasitic reduction with no degradation in the simulation results.

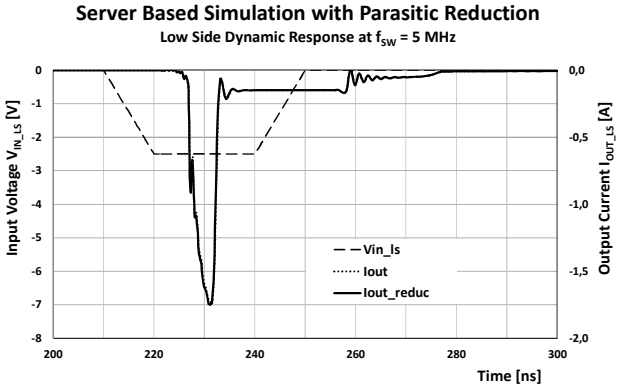

Figure 6 Post layout transient simulation

3 Measurements

Measurements of power devices request special care with respect to heat dissipation. Self-heating of the chip degrades the performance and provides false measurement values. In order to avoid such a misleading weak performance, measurements with pulses as short as necessary for no degradation need to be undertaken. In addition a force-sense configuration (cables, PCB tracks) of the high current leading connections is mandatory for an accurate feeding of the device under test.
In practice these two requirements are hard to realize in one measurement setup only. One can perform force-sense measurements at low DC currents under best heat dissipation and do short pulse measurements up to the maximum current (bold lines in Fig. 7).

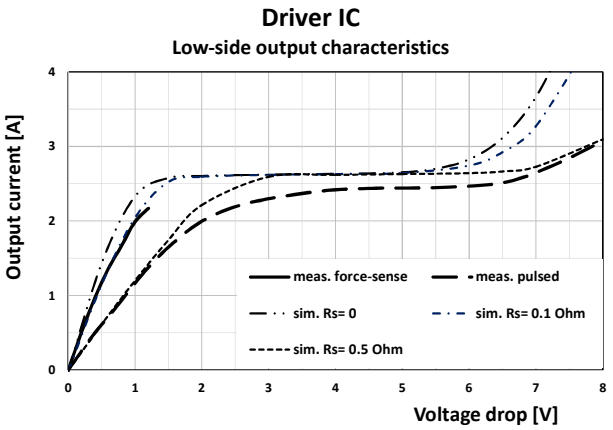

Figure 7 Comparison of measured and simulated DC output characteristics of the low-side branch

In designing the evaluation board, the same precautions must be applied in detail as for the entire converter application PCB. Unwanted current loops that degrade the efficiency have to be avoided [6].

4 Modelling

System simulations are mandatory to determine the performance of the entire DC-DC converter. It is a good idea to simplify the transistor level schematic of the driver into a much smaller macro model. Such a behavioral model consists of a mixture of analog and digital devices as well as of math description blocks. Some semi-conductor vendors deliver macro models of their driver circuits [5]. Fig. 8 shows an example of a driver IC macro model with few blocks only.

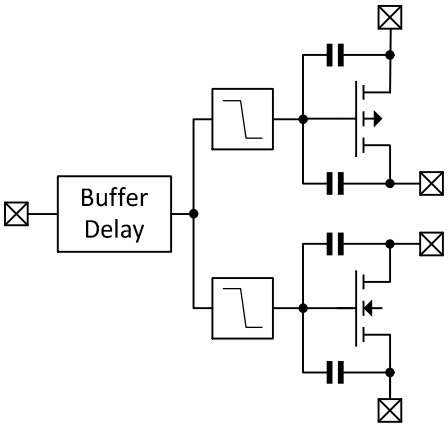

Figure 8 Simple driver macro model

The parameters of such a model are derived from measurements and cross-simulations (see also Fig. 7). Some dummy components like RC ladders should be added in order to relax convergence issues in the simulator due to steep signal steps.

5 Conclusions

We have presented some considerations concerning the design methodology of integrated driver circuits for DC-DC converters occurred during the different design phases. Some general thoughts from understanding the requirements to the driver circuit, determining the technology and architecture to the evaluation und modelling were figured out. Hints for parasitic extraction and simulation resulting from the handling of large data files were given.

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6 Literature

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