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Impact of SiGe HBT hot-carrier degradation on the broadband amplifier output supply current

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[1] ***Abstract*—The reliability of SiGe HBTs related to hot-carrier (HC) degradation is investigated using compact model including aging laws to quantify the output DC supply current variation of a driver amplifier. A physic-based aging compact model taking into account the reaction-diffusion model as well as the Fick hydrogen diffusion law is formulated and implemented in HICUM compact model. The model has been validated thanks to HBT aging tests results under several stress conditions allowing to extract its parameters. At circuit level, the reliability of the broadband amplifier has been investigated under dynamic operating conditions leading to locate and quantify the impact of HC degradation according to HBT load charge.**

***Index Terms*—SiGe HBTs, reliability, hot-carrier degradation, aging compact model, boradband amplifier**

I. Introduction

The continuous miniaturization of electronic devices, such as SiGe heterojunction bipolar transistors (HBTs) [1], has led to a significant safe-operating-area (SOA) reduction. As a consequence, the circuit designs are restrained in term of maximum output power due to a limited collector-emitter breakdown voltage (BV_{CEO}) values. Therefore, transistors operate now close to the SOA edges where impact ionization becomes unavoidable leading to HC degradation. A complete characterization and modeling of this failure mechanism and its consequences on the device and on the circuit reliability is recommended with the same methodology proposed in [2].

In this paper, we present the aging law related to the HC reaction-diffusion theory and its implementation in HICUM [3] compact model. The model parameters are extracted for the IHP's SG13S technology [4] which has been widely characterized from a reliability point of view in [5]–[7]. As an overall validation, the aging compact model is set in up for a broadband amplifier test vehicle allowing to identify the circuit weak points. The paper is organized as follows. Section II focuses on the aging compact model formulation and its parameter value extraction based on static stress conditions. Section III describes the aging test performed at circuit level. Subsequently, an analysis of the circuit degradation location is proposed.

II. Hot-carrier degradation at transistor level

A. Description

As pointed out in [5]–[9], the HC degradation leads to an increase of the base current and, therefore, to the degradation of the HBT current gain. This mechanism can be described as the creation of traps at the E-B spacer oxide interface [5] leading to the increase of an additional base current due to Shockley-Read-Hall (SRH) recombination. Indeed, the hot-carriers created by impact ionization mechanism can reach, with sufficient energy, the E-B spacer oxide interface leading to the dissociation of the passivated Si-H bonds. The interface traps are then associated with the silicon dangling bonds while the remaining hydrogen will diffuse away from the interface as sketched in figure 1.

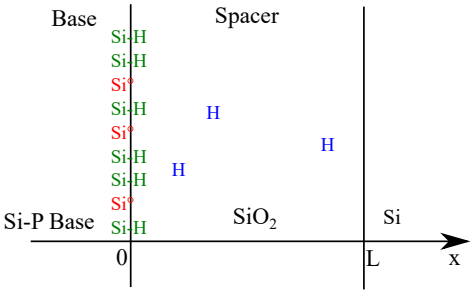

Fig. 1. Schematic of the hot-carrier degradation induced hydrogen diffusion in the E-B spacer

B. Model formulation

The rate at which the Si-H bonds break is governed by the reaction-diffusion theory as following

$$g_T(t) = K_F(N_F - N_T(t)) - K_R N_T(t) N_H(0,t) \quad (1)$$

where K_F is the rate constant of the forward reaction, i.e. generation of traps, K_R is the rate constant of trap annihilation by hydrogen atoms, N_H is the volumetric density of hydrogen at distance x from the Si/SiO_2 interface, N_T is the interface-trap density and N_F is the surface density of available bounds that can break. In addition with the reaction-diffusion model, the current aging model proposed an hydrogen diffusion model based on the diffusion Fick's law [10] as,

$$\phi_H(x,t) = -D_H \frac{\delta N_H(x,t)}{\delta x} \quad (2)$$

where ϕ_H(x,t) is the surface flow density of hydrogen and D_H is the hydrogen diffusion constant. This two-step aging law has been implemented in HICUM compact model through a two-part node as illustrated figure 2. The left part is related

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to the interface trap density $N_T(t)$ creation along the time as already proposed in [7]. The right part focuses on the hydrogen diffusion $N_H(0,t)$ from the interface through the E-B spacer thickness using a R-C ladder network commonly used, for instance, for thermal diffusion modeling [11]. Indeed, in order to obtain a time-invariant model, the time derivatives must appear as it is the case for R-C network. The number of poles (5 for this work) must be adapted to capture the hydrogen diffusion (as well as the annealing effect) for sufficient time decades. The interface trap density is then directly related to the additional recombination current through HICUM I_{REpS} parameter [12].

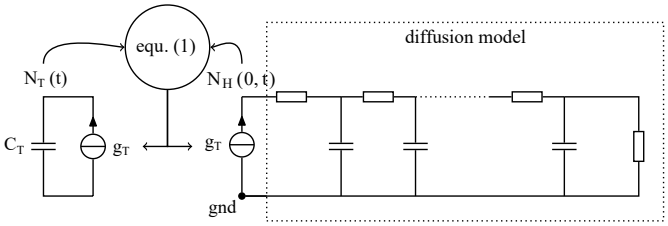

Fig. 2. Schematic of the implemented aging law in HICUM with the R-D and diffusion model

C. Aging compact model simulation results

From a large set of stress conditions [5], [6], the generation rate, K_F, have been extracted following multiple accelerating factors as presented in equation (3) [7]. The annealing rate K_R follows an Arrehnius law. The interface trap generation/annealing at the Si/SiO_2 interface is thus predicted for a wide range of stress conditions.

$$K_F = C_{MM} exp(\mu V_{CB}) \left[\frac{1}{|J_E|} + \frac{|J_E|}{J_{Ehc}} \right]^{\epsilon} \qquad (3)$$

A mixed-mode stress condition has been performed on IHP SG13S SiGe HBT technology with V_{BE} = 0.9V and V_{CE} = 2.5V during 7 hours with several in-between measurements allowing to extract the I_{REpS} parameter evolution as presented in the figure 3 inset. The extraction is compared to simulation results using the implemented aging model in HICUM. A very good prediction of the recombination current for low V_{BE} is achieved using this model parameter set.

Another validation is performed through Gummel plots simulations in figure 3 for different stress durations. Using a scalable model card and the extracted aging model parameters, a very good agreement is obtained between the measurements (solid symbols) and the simulations (solid lines).

III. Hot-carrier degradation analysis at circuit level

A. Broadband amplifier

The broadband amplifier [13] as presented figure 4 is composed of 11 transistors. The circuit is a 4-port system featuring differential input and output with GSSG probes configuration. It also requires three DC supply voltages, one for the common mode ICM, one for the input stage V_{CCi} and

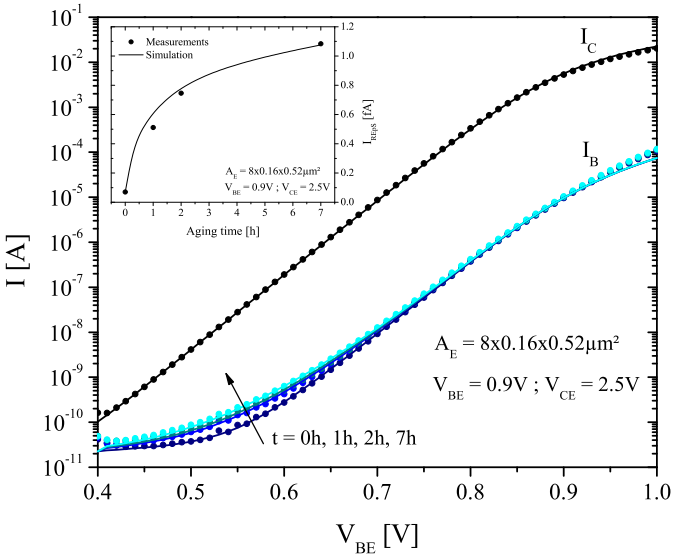

Fig. 3. Comparison between measurements (solid symbols) and simulation (solid lines) for Gummel plots at different stress duration for a static stress condition of V_{BE} = 0.9V and V_{CE} = 2.5V

one for the output stage V_{CCo}. In the output stage, inductive peaking implemented with T-Coil structures was used in order to increase the bandwidth. The transistor dimensions are summarized in table 1 featuring multiple emitter fingers N_X with a constant emitter width W_E of 0.16μm and constant emitter length L_E of 0.88μm. The factor m represents the number of transistor in parallel.

TABLE I
Circuit Transistor Dimensions

T	T1 - T2	T3 - T6	T4 - T5 - T7 - T8	T9	T10 - T11
N_X	4	2	2	2	8
m	1	1	2	16	1

The circuit exhibits a maximum gain of 8.8dB at f=25GHz associated with a bandwidth of 20GHz as illustrated figure 5. A comparison of this figure of merit (f.o.m) with the one simulated using HICUM compact model is then performed using a SiGe HBTs scalable model card (as done in part II.C). T-Coil structures were also modelled following [14] allowing an accurate reproduction of the differential gain within the circuit bandwidth. The differential gain simulation result (solid lines) is presented together with the measurements (solid symbols). An excellent accuracy is achieved for all frequencies up to 40GHz, in particular for the maximum gain around the associated peak value.

B. Reliability investigation

Dynamic stress tests was performed on the boradband amplifier by applying an input RF power of -15dBm and standard DC operating conditions, e.g. ICM=3V, V_{CCi}=3.3V, V_{CC0}=3.7V and T_{AMB}=25°C. The operating conditions of the 11 transistors are summarized in figure 6. Note that,

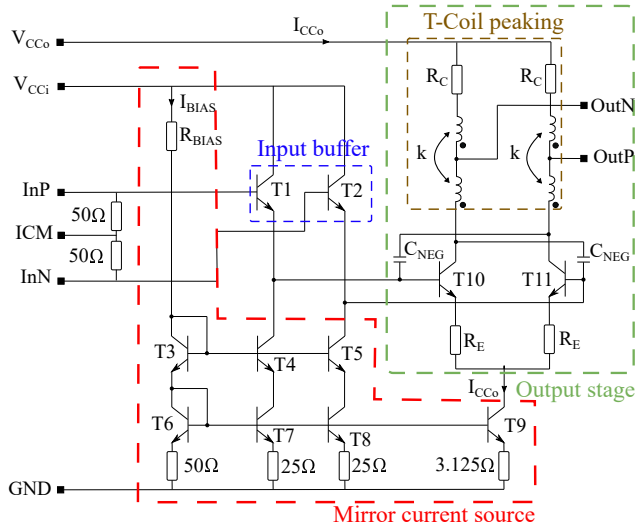

Fig. 4. Driver amplifier schematic [13]

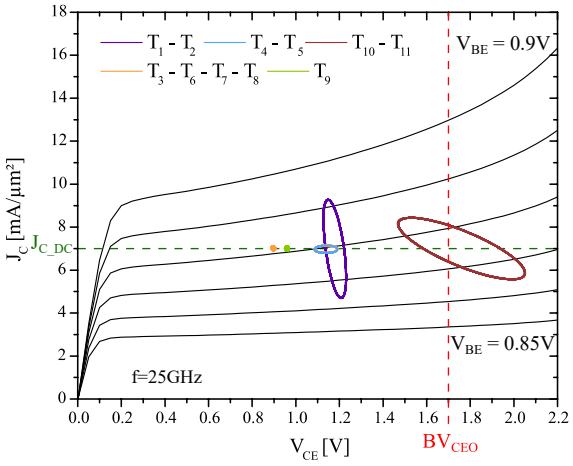

Fig. 6. J_C vs V_{CE} output characteristics for V_{BE} ranging from 850mV to 900mV with a step of 10mV superimpose with the bias conditions of the 11 transistors and the corresponding voltage excursion due to RF condition at f=25GHz

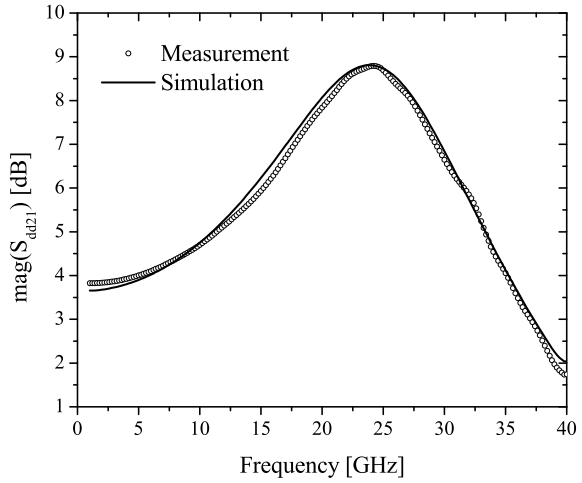

Fig. 5. Comparison between measurement and simulation for differential gain using HICUM L2 compact model at an ambient temperature of 25°C

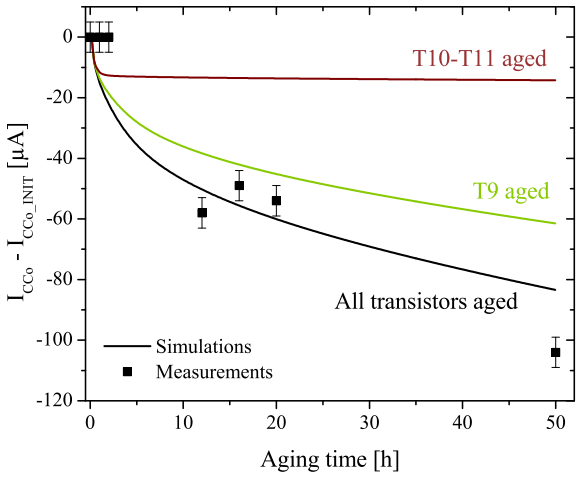

Fig. 7. Time evolution of the output supply current in measurements (solid symbols) and under several simulation conditions (solid lines): with only T10-T11 transistors aging virtually activated (in brown), only T9 transistor virtually activated (in green) and all transistors aging virtually activated (in black)

all transistors, excepted T10 and T11, are biased below the BV_{CEO} value, meaning that HC degradation, if any, will not be activated by a large electric-field for these transistors. Therefore, the failure mechanism can only be activated through the current density which mean value equals to 7mA/μm^2 for all transistors. The voltage excursion of T10 and T11 results from the combination of DC and RF values. Indeed, the large input RF power will drive the T10-T11 bias conditions beyond BV_{CEO} as presented in brown (fig. 6).

During the stress measurement campaign, the slight reduction of the differential gain S_{dd21} which has been observed is mainly associated with the equipment calibration shift. The circuit overall output f.o.m are not altered by the HC degradation as predicted in simulation with only a 0.001dB reduction of S_{dd21} value. However, a degradation of the output supply current I_{CCo} was measured as presented figure 7 in solid symbols characterized by a 100μA maximum reduction after 50 hours. A deeper analysis of the circuit is required to point out the origin of this variation.

C. Circuit output supply current evolution analysis

I_{REpS} parameter evolution over the stress time duration for the 11 transistors is displayed figure 8 and can be explained through their respective bias conditions analysis presented figure 6. Since the current density is equivalent for each transistors, the maximum I_{REpS} variation is due to their respective different V_{CB} values : for very low V_{CB} close to 0V (e.g. for T3, T6, T7, T8 and T9), the maximum I_{REpS} variation is around 1fA. On the contrary, the output stage transistors (T10 and T11) featuring a large V_{CB} value of 0.88V leading to a 3fA variation of I_{REpS} value demonstrate a specific sensitivity to HC degradation.

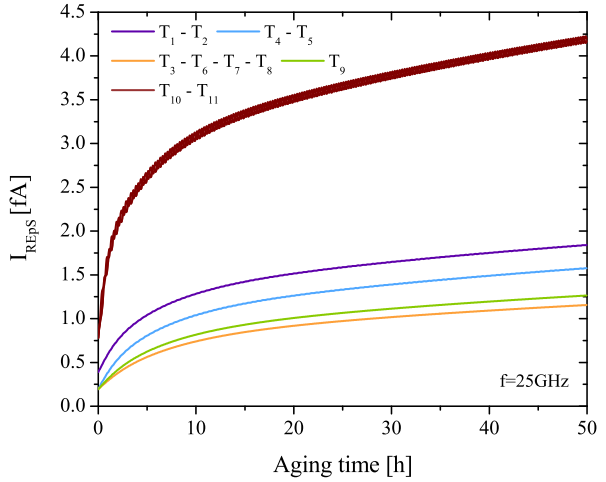

Fig. 8. I_{REpS} parameter evolution for all transistors in the driver amplifier for an ambient temperature of 25°C and dynamic stress conditions

Figure 7 present the output supply current I_{CCo} variation over the stress duration for several simulation conditions in order to locate the circuit weak points (i.e. more sensitive to HC degradation). In black, the aging flag was turn on for all circuit transistors leading to 80μA reduction of the output supply current compared to the initial value. This variation is close from the one measured during the aging test (see solid symbols). However, this reduction is not due to large bias conditions on T10-T11 transistors since if the aging flag is only activated for these two transistors, no significant degradation is observed on the output supply current. On the contrary, if the aging flag is only turn on for T9 transistor, a reduction of the sensitive parameter, i.e. I_{CCo}, appears with a maximum negative variation of 50μA. Indeed, the output supply current is governed by the current mirror stage (T3, T6 and T9) and can be expressed as following,

$$I_{CCo} = \frac{NI_{BIAS}}{1 + \frac{4N}{\beta}} \tag{4}$$

where β is the current gain and N is a scale factor between T6 and T9 transistors (which equals to 16). This equation demonstrates that the output supply current can only be impacted by a modification of β parameter. As a matter of fact, the input bias I_{BIAS} does not suffer from HC mechanism since it is created via a passive device R_{BIAS}. The current mirror source stage is then affected by HC degradation due to its dependency to β transistor parameter.

IV. Conclusion

A physic-based aging compact model has been formulated allowing to take into account for HC degradation. This aging model has been implemented in HICUM compact model including the interface trap generation as well as the hydrogen diffusion in the oxide. A very good accuracy between aging measurements and simulation results is achieved for static stress conditions at transistor level. The implemented aging compact model has been evaluated on a broadband amplifier leading to an accurate prediction of the circuit weakest points. Indeed, even if the maximum degradation is obtained on T10 and T11 devices as intended, the aging compact model allows to reveal that the relative low degradation on T9 will largely impact the β dependent stage and its electronic function.

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References

[1] P. Chevalier, M. Schrter, C. R. Bolognesi, V. d'Alessandro, M. Alexandrova, J. Bck, R. Flckiger, S. Fregonese, B. Heinemann, C. Jungemann, R. Lvblom, C. Maneux, O. Ostinelli, A. Pawlak, N. Rinaldi, H. Rcker, G. Wedel, and T. Zimmer, "Si/SiGe:C and InP/GaAsSb Heterojunction Bipolar Transistors for THz Applications," *Proceedings of the IEEE*, vol. 105, no. 6, pp. 1035–1050, Jun. 2017.

[2] C. Mukherjee, B. Ardouin, J. Y. Dupuy, V. Nodjiadjim, M. Riet, T. Zimmer, F. Marc, and C. Maneux, "Reliability-Aware Circuit Design Methodology for Beyond-5g Communication Systems," *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 3, pp. 490–506, Sep. 2017.

[3] M. Schrter and A. Chakravorty, *Compact Hierarchical Bipolar Transistor Modeling with HiCuM*. World Scientific, Nov. 2010.

[4] H. Rucker, B. Heinemann, W. Winkler, R. Barth, J. Borngraber, J. Drews, G. G. Fischer, A. Fox, T. Grabolla, U. Haak, D. Knoll, F. Korndorfer, A. Mai, S. Marschmeyer, P. Schley, D. Schmidt, J. Schmidt, M. A. Schubert, K. Schulz, B. Tillack, D. Wolansky, and Y. Yamamoto, "A 0.13m SiGe BiCMOS Technology Featuring ft/fmax of 240/330 GHz and Gate Delays Below 3 ps," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1678–1686, Sep. 2010.

[5] G. G. Fischer, "Analysis and modeling of the long-term ageing rate of SiGe HBTs under mixed-mode stress," in *2016 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sep. 2016, pp. 106–109.

[6] G. G. Fischer and G. Sasso, "Ageing and thermal recovery of advanced SiGe heterojunction bipolar transistors under long-term mixed-mode and reverse stress conditions," *Microelectronics Reliability*, vol. 55, pp. 498–507, Dec. 2014.

[7] C. Mukherjee, T. Jacquet, G. G. Fischer, T. Zimmer, and C. Maneux, "Hot-Carrier Degradation in SiGe HBTs: A Physical and Versatile Aging Compact Model," *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 4861–4867, Dec. 2017.

[8] H. Kamrani, D. Jabs, V. dAlessandro, N. Rinaldi, T. Jacquet, C. Maneux, T. Zimmer, K. Aufinger, and C. Jungemann, "Microscopic Hot-Carrier Degradation Modeling of SiGe HBTs Under Stress Conditions Close to the SOA Limit," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 923–929, Mar. 2017.

[9] B. R. Wier, U. S. Raghunathan, P. S. Chakraborty, H. Yasuda, P. Menz, and J. D. Cressler, "A Comparison of Field and Current-Driven Hot-Carrier Reliability in NPN SiGe HBTs," *IEEE Transactions on Electron Devices*, vol. 62, no. 7, pp. 2244–2250, Jul. 2015.

[10] J. R. Lowney and R. D. Larrabee, "The use of Fick's law in modeling diffusion processes," *IEEE Transactions on Electron Devices*, vol. 27, no. 9, pp. 1795–1798, Sep. 1980.

[11] M. Couret, G. G. Fischer, S. Fregonese, T. Zimmer, and C. Maneux, "Physical, small-signal and pulsed thermal impedance characterization of muti-finger SiGe HBTs close to the SOA edges," in *2019 International Conference on Microelectronic Test Structures (ICMTS)*, To be pusblished.

[12] M. Jaoul, D. Ney, D. Celi, C. Maneux, and T. Zimmer, "Analysis of a failure mechanism occurring in SiGe HBTs under mixed-mode stress conditions," in *2019 International Conference on Microelectronic Test Structures (ICMTS)*, To be pusblished.

[13] L. Iria Garcia, P. Rito, D. Micusik, A. Aimone, T. Brast, M. Gruner, G. Fiol, A. G. Steffan, J. Borngrber, L. Zimmerman, D. Kissinger, and A. C. Ulusoy, "High-Speed BiCMOS linear driver core for segmentd InP Mach-Zenhder modulators," *Analog Integrated Circuits and Signal Processing*, vol. 87, no. 2, pp. 105–115, May 2016.

[14] B. Razavi, "The Bridged T-Coil [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 4, pp. 9–13, 2015.