Physical, small-signal and pulsed thermal impedance characterization of multi-finger SiGe HBTs close to the SOA edges

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***Abstract*— A thermal impedance model of single-finger and multi-finger SiGe heterojunction bipolar transistors (HBTs) is presented. The heat flow analysis through the device has to be considered in two diffusion parts: the front-end-of-line (FEOL) diffusion and the back-end-of-line (BEOL) diffusion. Therefore, this new thermal impedance model features multi-poles network which has been incorporated in HiCuM L2 compact model. The HiCuM compact model simulation results are compared with on-wafer low-frequency S-parameters measurements at room temperature highlighting the device frequency dependence of self-heating mechanism. The simulation results are also compared to pulse measurements to improve reliability analysis.**

Keywords— SiGe HBTs, self-heating, multi-finger, safe-operating-area, pulse measurement, S-parameters measurements, thermal impedance modeling

I. Introduction

In order to satisfy the requirements of future THz applications, modern silicon-germanium heterojunction bipolar transistors (SiGe HBTs) operate now at frequencies up to 700GHz [1] thanks to a continuous miniaturization of electronic devices [2] and novel HBT architectures but to the cost of the Safe-Operating-Area (SOA) reduction. The SOA is limited by several transport mechanisms which are summarized in Fig.1: the avalanche at large V_{CB} and low J_C, the self-heating at medium V_{CB} and large J_C and the electro-migration at low V_{CB} and very large J_C.

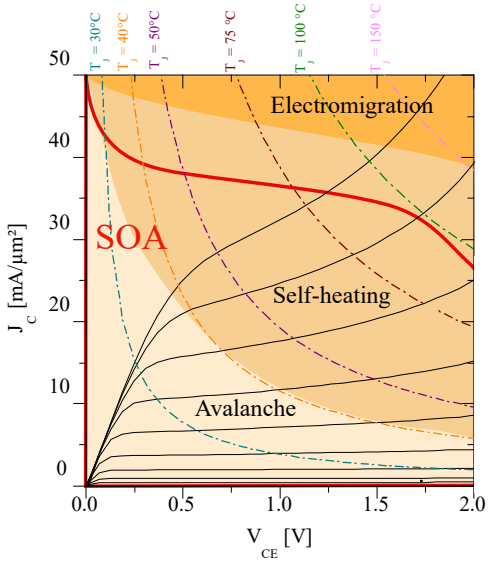

Fig.1 : Safe-Operating-Area definition for HBT

Yet, some studies have shown that the SOA can be extended beyond BV_{CEO} since open-base configuration is not commonly used by circuit designers. Accordingly, the HiCuM compact model has been extended beyond BV_{CEO} and up to BV_{CBO} in [3]. This extension must be deeply investigated since hot-carrier degradation appears beyond BV_{CEO} and leads to the DC transistor performance degradation [4]–[6]. Indeed, a high bias condition beyond the SOA edges leads to the base current degradation. Although, a recovery, due to traps annealing, of the degradation can be observed at high junction temperature [7] meaning that the hot-carrier degradation depends on both avalanche and self-heating effects.

An accurate modeling of the junction temperature rise using multi-pole network is then required to perform transient simulation involving a large V_{CE} range. Then, subsequently, annealing process could be deeply analyzed and characterized to be considered in aging model implementation. This work focuses on the thermal characterization and modeling of multi-finger high-speed SiGe HBTs from IHP SG13S technology [8] with reduced thermal constraints compared to competitive technologies. Investigated devices feature BEC configuration with a constant emitter width (0.12µm), two emitter lengths (0.48µm and 0.84µm) and two emitter fingers configurations (4 and 8 fingers) as summarized in Table 1 and Fig.2.

TABLE 1 : DEVICES UNDER TEST GEOMETRICAL FEATURES

Device	Drawn emitter W_E x L_E [µmxµm]	Number of fingers N_X	Effective emitter area A_E [µm²]
D22	0.12 x 0.48	4	0.53
D23	0.12 x 0.84	4	0.89
D32	0.12 x 0.48	8	1.06
D33	0.12 x 0.84	8	1.13

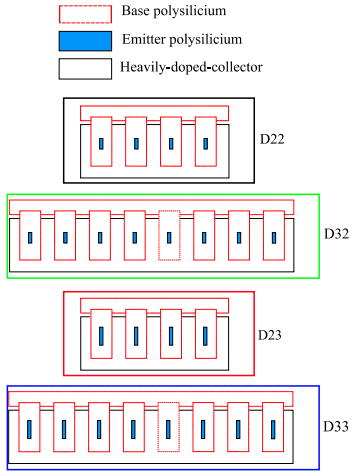

Fig.2 : Layout view for BEC configuration of DUTs

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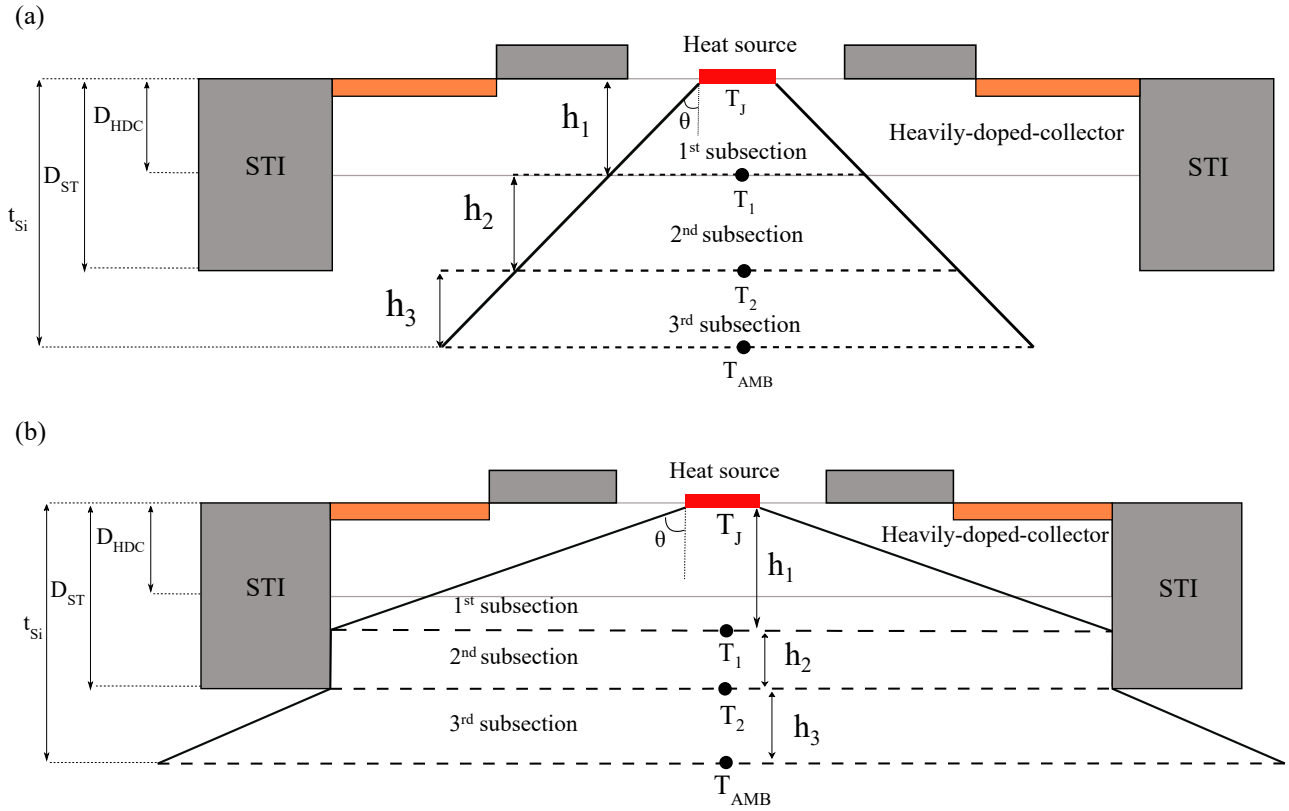

Fig.3 : Downward heat flow diffusion for a single finger transistor with (a) θ<65° and (b) θ>65°

The paper is organized as follows: Section II illustrates the model formulation and implementation of the physics based thermal network into HiCuM compact model; Section III presents the model simulation results compared to low-frequency S-parameters measurements and pulse measurements followed by a conclusion.

II. Model Formulation

A. Front-end-of-line heat diffusion

As presented in [9], the downward heat flow featuring a diffusion angle θ can be modeled by the superposition of N subsections leading to a distributed electro-thermal network. The heat source is located at the B-C junction [10] with an effective area of $W_E x L_E$. Each subsection is characterized by one thermal resistance R_{THi} and one thermal capacitance C_{THi} as following:

$$\begin{cases} R_{THi} = \int_{hi-1}^{h_i} \frac{1}{\kappa A_i(z)} dz \\ C_{THi} = \int_0^{h_i} \frac{\kappa}{\alpha} A_i(z) dz \end{cases} \quad (1)$$

where i is the subsection number ranging from 1 to N, A(z) is the cross-sectional area, h_i is the subsection thickness, κ is the temperature-dependent thermal conductivity and α is the silicon heat diffusion coefficient.

B. Single-finger transistor analysis

Physics based scalable model for thermal impedance have been mostly developed for complex transistor architecture featuring both deep trench isolations (DTI) and shallow trench isolations (STI). Indeed, the heat diffusion process in those technologies is confined by these isolations. Since IHP technology does not feature DTI, it leads to a reduced thermal budget [11] and a more efficient heat diffusion through the device which depends mainly on the value of the heat diffusion angle as presented fig.3 (a) and (b).

For a heat diffusion angle θ<65°, the heat flow is not stopped by the shallow trench isolations and the diffusion is pyramidal along the semiconductor (see fig.3 (a)). On the contrary, for a heat diffusion angle θ>65°, the heat flow will be surrounded by the shallow trench isolations, leading to a uniform heat diffusion in one subsection (see fig.3 (b)).

In the literature, the heat diffusion angle is always lower than 65° [12], leading to a heat flow as proposed fig.3 (a). In this manner, the shallow trench does not interfere with the heat diffusion through the device. For the rest of the paper, the heat diffusion angle θ is set to 45° as proposed in [9].

C. Thermal conductivity

Considering a heat diffusion flow as illustrated fig.3 (a), the downward heat flow has been divided into three subsections (N=3) considering the thermal conductivity of each layers. Indeed, the material thermal conductivity value depends of its doping level or composition profile values [10] as well as the temperature. Therefore, some reductions are considered compared to the reference substrate thermal conductivity k_{Si} following the work in [13].

The first subsection is located in the heavily-doped-collector with a corresponding thickness D_{HDC}. The high layer doping value leads to the reduction of the thermal conductivity of about 40% compared to the substrate. The second subsection is based outside the heavily-doped collector layer into the shallow trench isolation thickness D_{ST}. A gradual change in the doping profile from the high doped layer to the substrate is considered in this subsection leading to a 20% k_{Si} reduction. Finally, the last subsection is located in the substrate with the corresponding thickness t_{Si} and the original thermal conductivity k_{Si}. The value of t_{si} must be low enough since a large thickness will lead to a very low-frequency pole. After optimization, the hold value is 1.250µm which is three times higher than D_{ST}. The values of each section thickness h_i with the corresponding thermal conductivity are summarized Table 2.

TABLE 2 : SUBSECTION DESCRIPTION CONSIDERING THE MATERIAL, THE THICKNESS AND THE THERMAL CONDUCTIVITY

Sub.	Material	Thickness h_i [µm]	Thermal conductivity k_i @300K [$Wm^{-1}K^{-1}$]
1	High-doped silicon	0.2	90
2	Low-doped silicon	0.2	120
3	Silicon	0.75	150

D. Back-end-of line heat diffusion

The back-end-of-line is also modeled through a thermal resistance R_{TH_BEOL} which is calculated using the extracted thermal resistance R_{TH} and the calculated front-end-of-line thermal resistance R_{TH_FEOL} [14] as following:

$$R_{TH} = \frac{R_{TH\_FEOL} R_{TH\_BEOL}}{R_{TH\_FEOL} + R_{TH\_BEOL}} \quad (2)$$

The entire thermal resistance R_{TH} is extracted using the intersection technique [15] whereas the FEOL thermal resistance R_{TH_FEOL} corresponds to the combination of subsection thermal resistance R_{THi} divided by the associated number of fingers N_X:

$$R_{TH\_FEOL} = \sum_{i=1}^{i=N} \frac{R_{THi}}{N_x} \quad (3)$$

The different contributions of the thermal resistance are reported in Table 3 for the four transistors under test.

TABLE 3 : THERMAL RESISTANCE CONTRIBUTION INCLUDING BEOL AND FEOL FOR THE DUTS

Device	R_{TH} [K/W]	$R_{TH\ FEOL}$[K/W]	$R_{TH\ BEOL}$[K/W]
D22	3250	3900	20k
D23	2600	2800	19k
D32	1700	1950	13k
D33	1200	1300	13k

E. Multi-fingers transistors

The layout view of the device under tests presented Table 1 is illustrated fig.2. The emitter is divided into 4 or 8 parts in order to increase the available output power but also in order to reduce the thermal constraint. Indeed, the emitter partitioning leads to an important reduction of the self-heating phenomenon. Yet, the use of a thermal network for each finger requires an accurate model for one finger transistor together with coupling coefficients and will lead to the simulation time increase.

To avoid this constraint, a dedicated model card using HiCuM L2 compact model has been provided for all DUTs by IHP. Also, to consider multi-finger transistor without emitter partitioning, two scaling factors a_R and a_C are added to the equivalent electro-thermal network (see Fig.4). In the case of one-finger device, these scaling factors are set to 1. For multi-finger devices, the fingers are sufficiently spaced from the others to have negligible thermal coupling effect leading to $a_R=1/N_X$ and $a_C = 10N_X$. The electro-thermal network has been connected to the junction temperature equivalent node of the HiCuM L2 compact model.

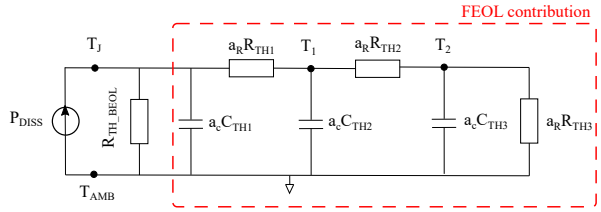

Fig.4 : Equivalent electro-thermal network implemented in HiCuM L2 compact model

III. COMPACT MODEL VALIDATION

A. Low-frequency S-parameters measurements

AC measurements were performed using a semiconductor parameter analyzer HP 4155 to set the DC bias points and a vector network analyzer Agilent E5061B (5Hz-3GHz) is used for RF inputs power as illustrated Fig.5. In order to provide RF and DC bias, bias tees were added to the base and collector port featuring a bandwidth between 30kHz and 3GHz. The VNA was calibrated using the SOLT calibration technique and a dembedding procedure has been applied on open test structures.

From an analysis point of view, only Y_{12} and Y_{22} parameters are presented since they are the most sensitive to self-heating effects [15]. The DC bias point was chosen to exhibit self-heating effects with enough accuracy, basically with large base-emitter voltage V_{BE}. The bias condition presented in this paper correspond to V_{BE}=0.95V and V_{CE}=1.5V.

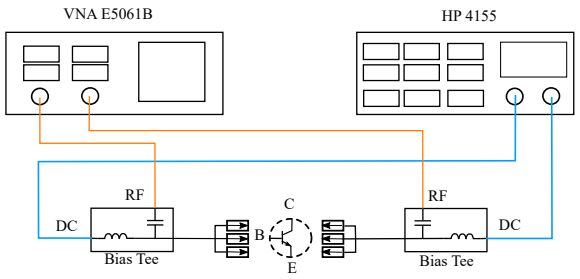

Fig.5 : Low-frequency S-parameters measurement bench

Fig.6 compares Y-parameters measurement to the simulation results using the single pole network from the HiCuM compact model and the simulation results using the multi-pole network for the smallest device D22. As it is observed, the single pole network is not accurate enough contrary to the extended model demonstrating a good accuracy for both Y-parameters in the lower frequency range, where dynamic self-heating is typically observed.

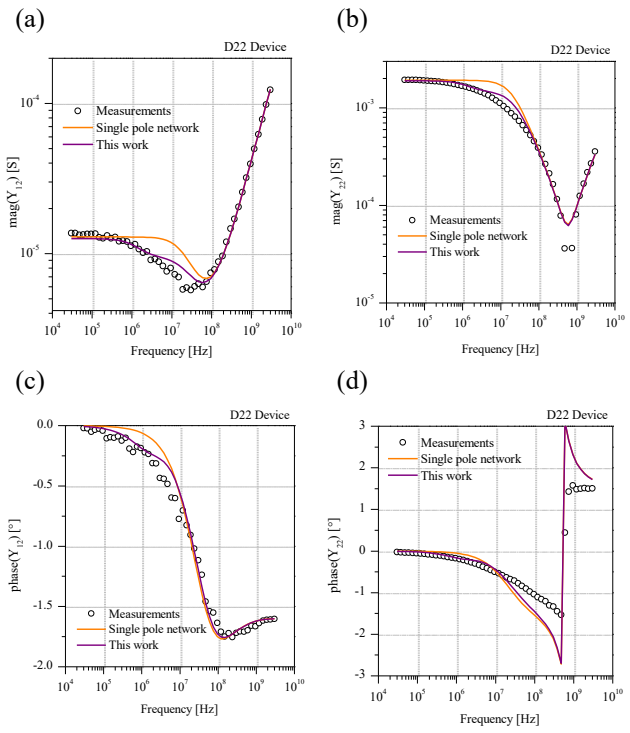

Fig.6 : D22 device comparison between measurements (symbols) and HiCuM compact model simulation results using single pole network (orange lines) and physics based multi-pole network (purple lines) for (a) Y_{12} magnitude, (b) Y_{22} magnitude, (c) Y_{12} phase and (d) Y_{22} phase at V_{BE}=0.95V and V_{CE}=1.5V

Indeed, the single pole network will only separate the dynamic self-heating part from the pure electrical part. The boundary between these two elements is called the maximum thermal cut-off frequency f_{TH} and is located around 150 MHz, i.e. where the Y_{12} phase is minimum, leading to a unique thermal time constant value τ_{TH} of 7ns. It is important to note that τ_{TH} is obtained through the combination of $R_{TH}C_{TH}$. On the contrary, the multi-node network will also allow to model the dynamic self-heating part (in the lower frequency range) with multiple thermal time constants τ_{THi} related to each device subsection.

The improved model is also validated for all geometry configurations (Table 1) as shown in Fig.7. A very good accuracy is achieved for all devices. The associated thermal resistances and capacitances are presented Table 4 for all DUTs. The analysis of Table 4 shows that, as intended, the largest thermal resistance contribution comes from the first subsection with R_{TH1} which represents more than 75% of the R_{TH_FEOL} for all devices. The corresponding thermal capacitance C_{TH1} is quite low meaning that it will set the minimum thermal time constant value, i.e. the maximum cut-off frequency f_{TH}. Concerning the other subsections, the most important parameter is the thermal capacitance. Indeed, each of them are separated by a decade meaning that each subsection will be characterize in a specified frequency range in the entire spectrum. For example, the substrate thermal capacitance C_{TH3} is very high, meaning that this subsection will model the lower frequency range, i.e. from 100 kHz to 1 MHz.

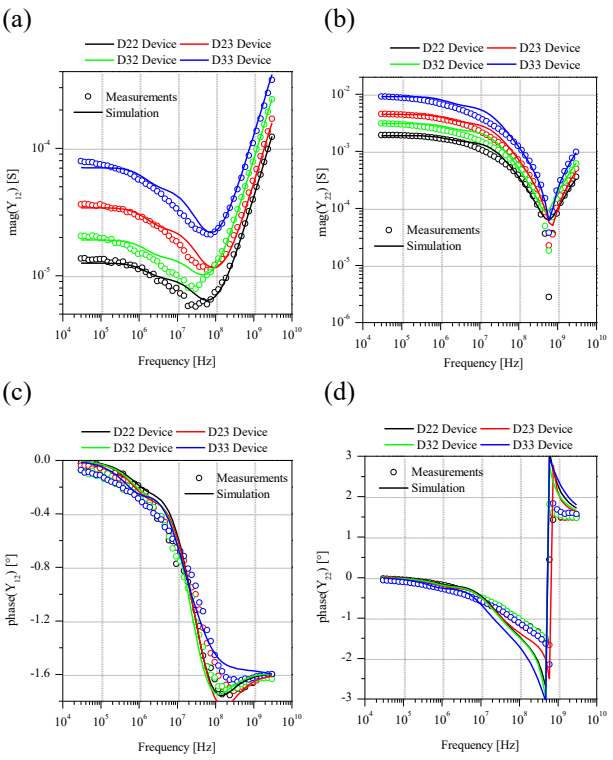

Fig.7 : All DUTs comparison between measurements (symbols) and HiCuM compact model simulation results (solid lines) for (a) Y_{12} magnitude, (b) Y_{22} magnitude, (c) Y_{12} phase and (d) Y_{22} phase at V_{BE}=0.95V and V_{CE}=1.5V

TABLE 4 : THERMAL RESISTANCES AND CAPACITANCES EXTRACTED FOR THE FEOL CONTRIBUTION USING THE PHYSICS BASED SCALABLE MODEL

Device	R_{TH1} [K/W]	R_{TH2} [K/W]	R_{TH3} [K/W]	C_{TH1} [J/K]	C_{TH2} [J/K]	C_{TH3} [J/K]
D22	2553	500	840	2p	9.4p	147p
D23	1732	379	682	3p	12p	298p
D32	1335	252	397	4.1p	18.7p	294p
D33	821	187	309	6.5p	25.3p	358p

B. *Pulse measurements*

Pulse measurements have also been achieved using a dedicated measurement bench described in Fig.8. The DC pulsed DC analyzer Keithley 4200-SCS consists of two pulse measurements units (PMUs). The pulse train (CH1) is applied to the transistor base port whereas the collector port (CH2) is biased at a constant voltage. In order to compare transient simulation to measurements, the parasitic components associated with the coaxial cables as presented Fig.9 must be considered as explained in [17].

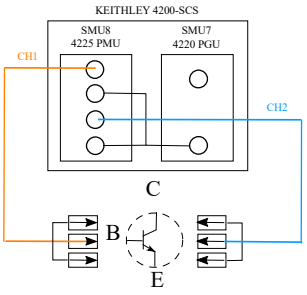

Fig.8 : Measurement test bench for pulse measurements

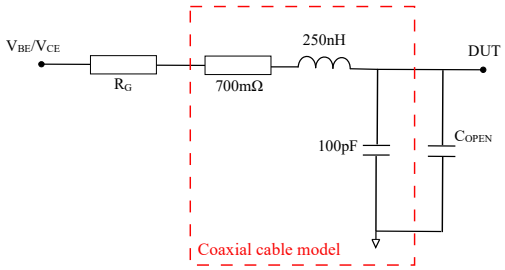

Fig.9: Passive network including coaxial cables, generator resistance R_G and device open capacitance C_{OPEN}

Furthermore, the electro-thermal network model including the coaxial cable allows to perform transient simulation with an accurate prediction of the I_C waveform, as shown in Fig.10 for D33 device. Indeed, this figure presents a comparison between a pulse measurement (considering a pulse width of 500ns and the following bias point V_{BE}=0.95V and V_{CE}=1.5V) and the HiCuM compact model simulation with the proposed thermal node. Overshoots that are visible in measurements are correctly reproduce due to the introduction of the passive network. The use of a single pole network (see Fig.10 in orange) during transient simulation will lead to a very fast steady-state temperature whereas the more complex multi-node network (see Fig.10 in purple) allows an excellent accuracy between measurements and simulation [17].

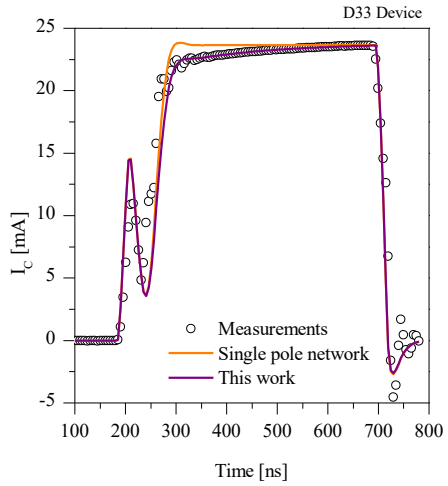

Fig.10 : D33 device comparison between measurements (symbols) and HiCuM compact model simulation results using single pole network (orange lines) and physics based multi-pole network (purple lines) at T_W=500ns, V_{BE}=0.95V and V_{CE}=1.5V

Fig.11 illustrates the collector current waveform for all DUTs at a given bias point V_{BE}=0.95V and V_{CE}=1.5V. As for Fig.10, a very good accuracy is achieved between measurements and HiCuM compact model simulation integrating the multi-pole thermal network. The proper estimation of the junction temperature is then validated following two approaches: the frequency domain and the time domain.

IV. Conclusion

A physics based scalable thermal impedance model has been developed for the SiGe HBT technology from IHP having an innovative architecture facilitating thermal dissipation. The model has been adapted to multi-finger transistors and evaluated over a wide range of device geometries. Both frequency and transient simulations have been compared to the compact model simulation results for all geometries. A very good accuracy can be observed demonstrating the requirement for a more complex thermal network compared to the single pole network as implemented today in the HiCuM compact model. The multi-node thermal network will lead to an accurate estimation of the junction temperature close to the SOA edges and will allow the analysis of annealing effects during reliability simulation.

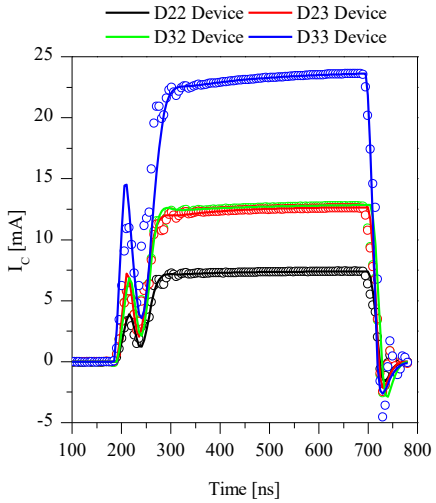

Fig.11 : Comparison between HiCuM compact model transient simulation and waveform captures for at T_W=500ns, V_{BE}=950mV and V_{CE}=1.5V the collector current IC for all device geometries

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