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A Unified Aging Compact Model for Hot Carrier Degradation under Mixed-mode and Reverse E-B stress in Complementary SiGe HBTs

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Abstract

This paper presents an accurate, comprehensive and physics-based aging compact model for stress-induced degradation due to hot-carrier generation and oxide trapping in advanced complementary NPN and PNP SiGe HBTs. The analytical model equations are derived from the solution of reaction-diffusion theory and Fick's law of diffusion combined with oxide trapping mechanism under accelerated stress conditions. The model accuracy has been validated against results from long-term aging tests performed close to the safe-operating-areas of an advanced complementary 0.25 µm BiCMOS technology. Degradation asymmetry observed between NPN and PNP devices is accurately captured by this unified aging compact model. This study highlights the challenges of predicting degradation of complementary circuits and thereby improving its functionalities by designing better-matched NPN and PNP HBTs.

Keywords: Aging, compact model, complementary SiGe HBTs, hot-carrier degradation, safe operating area

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1. Introduction

Long-term reliability of modern SiGe heterojunction bipolar transistors (HBTs) is increasingly becoming a major concern for circuit designers. Continuous improvement of the maximum operating frequency leads to an increase of operating current density and a reduction of breakdown voltages [1]. Moreover, advance circuit applications require the transistors to operate closer and even beyond their classical safe-operating areas (SOA). Hence, reliability-aware circuit design has become a mandatory approach [2] employing accurate aging models [3] to facilitate time and cost-effective circuit design. Complementary circuit functionalities employing both NPN and PNP bipolar transistors are of particular interest owing to their large variety of RF, analog and high speed digital applications [4]. However, performance mismatch between the NPN and PNP devices, due to their different architectures and mode of technological integration, are particularly detrimental for both DC and AC operation of complimentary circuits. Added to these concerns, reliability issues such as bias temperature instability are more severe for complementary circuits because of nonequivalent degradation in either type of devices. More precisely, as supported by experimental evidence, hot carrier induced damage is more aggressive and accelerated in PNP devices over their NPN counterpart, which not only significantly impedes symmetric circuit operation, it also poses major challenges for high performance circuit design. Only a few previous studies have illustrated the impact of bias-dependent mismatch on the aging of complementary devices [5]. Investigation of degradation physics in complementary devices has also been studied using TCAD simulation [6]. From the circuit designers' point of view, the major degradation mechanism that needs to be accurately incorporated in SPICE compact models is hot-carrier degradation (HCD) that predominantly limits the lifetimes of modern SiGe HBTs [3, 5-10]. The principal physical degradation mechanism is the generation of hot carriers, through impact ionization under high field or current conditions at the collector base junction, which are accelerated toward the emitter-base (EB) spacer oxide interface where they create traps via Si-H bond-breaking. The formation of these traps can be identified by the degradation of non-ideal base current [3]. There have been many forms of the reaction-diffusion (R-D) formalism adapted for describing HCD physics in SiGe bipolar transistors [3, 6, 9-10] each with their application specific limitations. One of the more versatile and unified closed form solutions has been proposed in [3]. This model (HiCuM AL V1) has been further enhanced in an upgraded version, HiCuM AL V2, and a more accurate compact model implementation that also accounts for dynamic stress conditions, ensuring time-invariance of the compact model [11].

This paper aims to provide a detailed compact modeling approach for studying the aging-induced degradation asymmetry in advanced complementary SiGe HBT technologies under both

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mixed-mode and reverse E-B stress conditions, based on the aging compact model developed in [3, 11]. With the accuracy of the model in [11] validated for a wide range of advanced industrial SiGe HBT technologies under diverse stress conditions close to their safe-operating areas, the aging compact model is adapted for analyzing the degradation behavior of a complementary BiCMOS technology from IHP [12]. Mixed-mode (MM) aging tests for the complementary NPN and PNP HBTs show the expected asymmetry in the degradation depicting more aggressive degradation in PNP devices. An additional component of degradation is observed in case of the PNP devices at higher stress bias that cannot be captured by R-D based HCD compact models such as the one in [11]. While this component is not observed in case of NPN HBTs under MM stress within the maximum of 1000h stress duration, both transistors exhibit this additional component under high E-B reverse stress conditions. The stress bias-dependence of this component, attributed to fast oxide trapping, is analyzed and modeled using HiCuM AL V3.1, which extends the previous aging compact model in [11].

The rest of this paper is organized as follows: Section 2 illustrates the model formulation and the derivation of bias-dependence of aging model parameters along with model implementation; Section 3 describes the SiGe HBT technology under test and the stress bias conditions, the aging test results, model validation followed by the conclusion.

2. Aging Model Formulation: Premise and Derivation

To illustrate the electrical signature of the aforementioned additional oxide trapping mechanism, Fig. 1 shows the base current degradation for an NPN SG25H3P HBT from IHP's complementary 0.25 µm BiCMOS technology [12] under mixed mode (1 (a)) and reverse emitter-base (1 (b)) stress conditions. While for the reverse E-B stress conditions it is much more significant, both stress conditions exhibit that at longer stress time, there exists an additional contribution to the base current degradation that cannot be accurately captured by the previous version of our aging model HiCuM AL V2 [11]. In contrast, the improved model formulation presented in this work, HiCuM AL V3.1 (detailed in the next section), can accurately capture this additional mechanism (Fig. 1). In effect, the oxide trapping mechanism is evidently more significant under reverse E-B stress, which can be explained by the fact that regardless of the presence of large electric fields, the origin of the hot carriers are somewhere in the E-B region under reverse E-B stress compared to that of the C-B junction under mixed-mode stress [6]. While the hot carriers under E-B stress have a lower transport loss and smaller distance to cover (relative to the scattering length/mean free path) to reach the E-B spacer, more significant degradation can be observed in this case. In case of PNP transistors, as we will show later on, this effect is more pronounced even in mixed-mode conditions. This additional effect can be attributed to the oxide trapping (OT) mechanism which appears to intensify at higher stress bias at long stress time. The dynamics of this mechanism is similar to the phenomenon of bulk trap generation in MOS transistors, responsible for its dielectric breakdown [13]. To the best of knowledge, this is the first notable observation of this effect in modern SiGe HBTs.

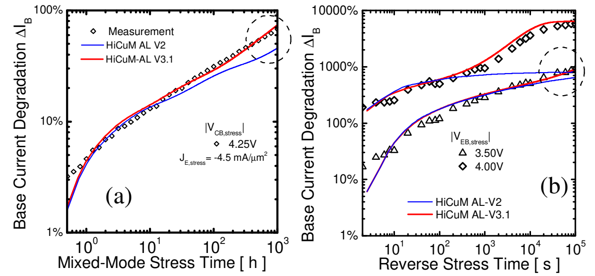

Fig. 1: Base current degradation of an NPN SG25H3P HBT under (a) mixed mode and (b) reverse emitter-base stress depicting the additional oxide trapping component at longer stress time.

While the oxide trapping component starts to dominate at longer stress time, HiCuM AL V2 [11] can accurately describe the degradation in the earlier stress time. For reverse E-B stress, on the other hand, specifically at a stress voltage of 4 V, the excess degradation component (OT) depicts a significant deviation from what the HiCuM AL V2 predicts. HiCuM AL V2 has been adapted to incorporate modeling of this effect in a newer version, HiCuM AL V3.1, where the OT mechanism has also been introduced.

HiCuM AL V2 has been developed principally based on the R-D theory [10]. Hence the initial phase of modeling concerns the derivation of the analytical model equations governing the physics of hot-carrier degradation (HCD). In HCD, the rate of bond

dissociation is governed by a chemical interaction between the carriers and the passivated Si-H bond through generation and annihilation of traps. The interface-trap density, $N_T\ (t)$, increases with the net rate of reaction described by the R-D model [3, 10-11] as,

$$\frac{dN_T}{dt} = K_F\big(N_F - N_T(t)\big) - K_R N_T(t) N_H(0,t) = g_T \quad (1)$$

Here, K_F is the rate constant of the forward reaction, *i.e.*, generation of traps, K_R is the rate constant of trap annihilation by hydrogen atoms, $N_H(x,t)$ is the volumetric density of hydrogen at distance x of the Si/SiO$_2$ interface and N_F is the total number of available bonds that can break. To support the simulation under dynamic stress conditions and to ensure time-invariance of the compact model compared to [3], HiCuM AL V2 employs an R-C ladder network for modeling hydrogen diffusion within the E-B spacer (Fig. 2c), similar to the architectures commonly used for modeling heat diffusion in vertical HBT structures. While (1) can be directly embedded in a Verilog-A model, the R-C ladder network represents the diffusion equations in the oxide volume including the interface. Though these equations cannot be directly implemented in the Verilog-A code, the implementation can be done by simply identifying the relation between $N_H(0,t)$ and $g_T(t)$, in order to link the diffusion sub-circuit with the rest of the aging module. In order to reduce the number of parameters of the aging model, the values of the R-C network elements, R_n and C_n, follow two geometrical sequences [11]:

$$R_n = R_1 \alpha_R^{n-1}, \quad C_n = C_1 \alpha_C^{n-1} \quad (2)$$

Here, α_R, α_C, R_1 and C_1 are compact model parameters governing the H-diffusion. In addition to this setup, HiCuM AL V3.1 employs an additional fictitious transistor node for the oxide trap generation through the total oxide trap density $N_{OX}(t)$ which is governed by an exponential stress time dependence similar to the implementation of bulk trap in [13]. In our model the following differential form is incorporated in the compact model with two additional model parameters, N_{OXMAX} and τ_{OX} for the maximum oxide trap density and oxide time constant, respectively, as,

$$\frac{dN_{OX}(t)}{dt} = \frac{N_{OXMAX} - N_{OX}(t)}{\tau_{OX}} \quad (3)$$

Eq. (3) is represented by a single pole network shown in Fig. 2(b), consisting of a resistor of value τ_{OX} and a capacitor of value 1F, along with a current source of magnitude N_{OXMAX}/τ_{OX}. It is theorized that thicker oxides are more prone to exhibit the OT mechanism owing to their higher capacity of oxide trap generation, as indicated in [14]. This could also present a comparative perspective for the different topographies of spacer oxides integrated within their respective process flows of the SiGe HBT technologies [15]. In other words, this could explain the absence of this component in our earlier works [3, 11]. Interestingly though, the presence of this component can also be seen in case of previous aging tests performed on the same technology [Fig. 6, ref. 5], which was left unaddressed due to absence of sufficient data for analysis.

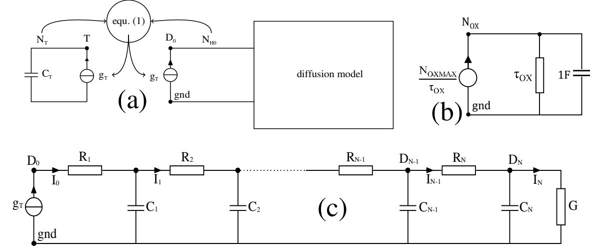

Fig. 2: Organization of the (a) R-D, (b) OT and (c) Diffusion model implementations.

Similar to the previous versions of the aging model, HiCuM-AL V1 [3], and HiCuM-AL V2 [11], the base current degradation has been implemented in HiCuM compact model through the recombination current parameter in the periphery, I_{REpS}. In the current version of the aging model (HiCuM-AL V3.1), the evolution of I_{REpS} is translated from the combined evolution of the trap densities $N_T\ (t)$ and $N_{OX}\ (t)$. K$_F$ (s^{-1}), K$_R$ (cm^{3}s^{-1}) of (1) are represented by their corresponding compact model parameters $K_{F,I}$ (s^{-1}), $K_{R,I}$ (cm.A^{-1}.s^{-1}), respectively, and N$_F$ by I_F (A) which is the final value of ΔI_{REpS}, (A). Similarly, for oxide trap generation related parameters in (4) N_{OXMAX} is represented by I_{OX} (A) and τ_{OX} (s) by $\tau_{OX,I}$ (s). While I_F and I_{OX} remain model parameters pertaining to the process, the parameters $K_{F,I}$, $K_{R,I}$ and $\tau_{OX,I}$ are represented as function of the stress bias. This results in a revised model parameter set that can be efficiently exploited for analysis of circuit aging.

Firstly, under mixed-mode stress the forward rate constant, $K_{F,I}$, increases with $V_{CB,stress}$ following an exponential dependence while $J_{E,stress}$ is kept constant. On the other hand, while $V_{CB,stress}$ is kept constant, $K_{F,I}$ demonstrates a peak value before starting to roll off [3, 7, 11]. This has been explained by a decrease in the C-

B electric field at the onset of the Kirk effect at such high stress current densities [3, 16], resulting in a reduction in ΔI_B. The decrease of the impact ionization mechanism at high current densities has been demonstrated in [16], which can be held responsible for the decline of the avalanche current density, J_{AVL}, at large emitter stress current densities [16]. Taking this into account, the expression for $K_{F,I}$ under mixed-mode stress has been simplified by introducing the J_{AVL} parameter obtained using the new avalanche model [16]. For reverse E-B stress, however, $K_{F,I}$ is only an exponential function of the reverse E-B stress bias, $V_{EB,stress}$. Additionally, an Arrhenius-like temperature dependence is added to the expressions of $K_{F,I}$. The activation energy, E_0, is identical (0.24 eV) to the values for previously reported SiGe HBT technologies [11] which governs the temperature dependence of the rate constants. The expressions of $K_{F,I}$ under mixed mode and reverse E-B stress, respectively, can thus be written as,

$$K_{F,I}\big|_{MM} = g_{rate} J_{AVL} \exp\left(\mu_F V_{CB,stress}\right) \exp\left[-\frac{E_0}{k_B T}\right] \qquad (4)$$

$$K_{F,I}\big|_{EB} = K_{F,I0} \exp\left(\mu_F V_{EB,stress}\right) \exp\left[-\frac{E_0}{k_B T}\right] \qquad (5)$$

Here, the new aging compact model parameters are g_{rate} ($\mu m^2 A^{-1} s^{-1}$), which is the fraction of the avalanche current density that reaches the spacer oxide interface [15] and μ_F (V^{-1}) which is the exponential factor that governs acceleration of hot carriers under the applied electric field. The use of J_{AVL} instead of $J_{E,stress}$ simplifies the previous expression proposed in [11].

On the other hand, the trap annihilation rate strongly depends on the junction temperature and follows an Arrhenius law. Additionally, the stress bias dependences are introduced similar to that of $K_{F,I}$, although the bias-dependence is relatively weaker. The expressions of $K_{R,I}$ under mixed mode and reverse E-B stress, respectively, can thus be written as,

$$K_{R,I}\big|_{MM} = K_{R0} \exp\left(\mu_R V_{CB,stress}\right) \exp\left[-\frac{E_0}{k_B T}\right] \qquad (6)$$

$$K_{R,I}\big|_{EB} = K_{R0} \exp\left(\mu_R V_{EB,stress}\right) \exp\left[-\frac{E_0}{k_B T}\right] \qquad (7)$$

Here, the new aging model parameters are K_{R0} , which is the magnitude of $K_{R,I}$ in $cmA^{-1}s^{-1}$, μ_R is the exponential factor in V^{-1}.

Finally, the temperature and stress bias-dependence of $\tau_{OX,I}$ was found to be of inverse nature as that of $K_{F,I}$ and $K_{R,I}$. Hence, to maintain modular expressions, the following equations can be written for $\tau_{OX,I}$ under mixed mode and reverse E-B stress, respectively,

$$\tau_{OX,I}\big|_{MM} = \tau_{OX0} \exp\left(-\mu_{OX} V_{CB,stress}\right) \exp\left[\frac{E_0}{k_B T}\right] \qquad (8)$$

$$\tau_{OX,I}\big|_{EB} = \tau_{OX0} \exp\left(-\mu_{OX} V_{EB,stress}\right) \exp\left[\frac{E_0}{k_B T}\right] \qquad (9)$$

Here, the new aging model parameters are τ_{OX0} , which is the magnitude of $\tau_{OX,I}$ in s and μ_{OX} is the exponential factor inV^{-1}. Further analyses on the three aging model parameters are presented at the end of section 3 which demonstrate the validity of the equations (4-9) against experimental results.

The temperature dependence of the H-diffusion coefficient, D_H, is also governed by an Arrhenius law, for which the value of the activation energy E_A used in our model is roughly 0.48 eV, which is consistent with the values reported in [3]. Additionally, the temperature dependence of the H-diffusion R-C network directly stems from the temperature dependence of D_H. The resistance R_1, which is inversely linked to the velocity at which the H-diffusion front diffuses, is the only temperature dependent quantity; whereas, C_1 signifies the lateral incremental length of the subsequent cells of the R-C network and is only geometry dependent. Hence the equations governing these two quantities read,

$$D_H = D_{H0} \exp\left[-\frac{E_A}{k_B T}\right], \; R_1 = \frac{C_1}{D_H} \qquad (10)$$

Here, the aging model parameters are D_{H0} and E_A.

3. Model Validation

In this section, we test the validity of the model under various aging conditions, close to the SOA of the NPN and PNP HBTs from IHP's complementary 0.25 µm BiCMOS technology [12]. The mixed mode aging tests were performed up to 1000h of stress time, whereas the aging tests under reverse E-B stress were performed up to 10^5 s of stress time.

The aging compact model was validated on both NPN and PNP HBTs featuring transistors in BEC configuration with effective emitter areas of 0.3×0.92 and 0.22×0.84 μm^2, respectively. Aging tests were performed under various mixed-mode stress conditions as illustrated on the output characteristics in Fig. 3 (a) for both type of HBTs. Base current degradation under mixed mode stress conditions is governed by the two accelerating factors of stress: V_{CB} and J_E, which are chosen around peak-f_T so that the operating points are above the open base breakdown voltages $B_{VCEO,\,NPN}$ = 2.2 V and $B_{VCEO,\,PNP}$ = 2.8 V. The open-emitter break-down voltages of these HBTs are $B_{VCBO,PNP}$ = 4.0 V and $B_{VCBO,NPN}$ = 6.0 V, which already indicates that the PNP HBT will be more prone to base current degradation under the same stress voltages.

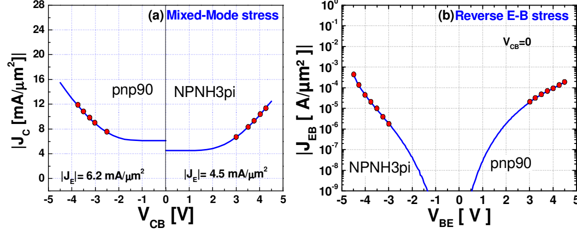

Fig. 3: Aging test bias conditions for both NPN and PNP HBTs under (a) mixed-mode, (b) reverse E-B stress.

In case of reverse E-B stress, degradation occurs under reverse biased E-B diode stress with a shorted CB junction (V_{CB} = 0V). The stress conditions chosen in our study are highlighted in Fig. 3(b) for the two HBTs. Here, the junction tunneling current is the major source of the highly energetic carriers which are able to create traps at the E-B spacer oxide interface [6]. Since the distance these carriers have to travel is much shorter than for MM stress [6], an immediate and more pronounced increase of the non-ideal base current is expected in case of reverse E-B stress.

The asymmetry of the degradation in the NPN and PNP HBTs is evident from the results of the evolution of the normalized excess base current ($\Delta I_B/I_{B0}$) as a function of aging time, as demonstrated in Figs. 4 (a) and (b) for both HBTs under mixed-mode stress. Fig. 4 (a) depicts the results for different $V_{CB,stress}$ (3 - 4.25 V) under constant $J_{E,stress}$ (4.5 mA/μm^2) for the NPN HBTs, while Fig. 4 (b) shows the results for the PNP HBTs under different $V_{CB,stress}$ (2.5 - 3.75 V) with constant $J_{E,stress}$ (6.2 mA/μm^2). The different values of $J_{E,stress}$ are used to maintain similar junction temperature values for both NPN and PNP HBTs during aging. In fact, the effect of oxide trapping starts to dominate from a $V_{CB,stress}$ of 3.25V for the PNP HBTs whereas the oxide trapping effect is not at all prominent in case of the NPN HBTs under mixed-mode stress.

The principal reason that the PNP HBTs (Fig. 4 (b)) show much more pronounced oxide trapping compare to the NPN HBTs under MM stress is that there is more impact ionization in the PNP HBTs at high V_{CB} due to its lower B_{VCBO} compared to that of the NPN HBTs that depict more gradual degradation. Also, PNP HBTs have a smaller open-emitter breakdown voltages thus having its degradation accelerated. Apart from the different generation rates of hot carriers in the two device types, the dynamics of hot carrier trapping depends on carrier types [6]. While secondary hot holes are dominant carriers in NPN devices, the hot electrons are the major force behind the degradation in PNP HBTs that have superior scattering lengths and thus higher retention of energy [6]. Due to the proximity of the E-B spacer region compared to the NPN devices, significantly more trap formation is expected in PNP devices. Added to this, the complexity of complementary device degradation increases due to the different activation energies associated to the E-B spacer traps with relevant polarities involved in the degradation. With lower activation energies in case of PNP transistors [6], the Si-H bonds are easier to break in these devices, making them more susceptible to degradation. The limits of the base current degradation, estimated following [13], is also shown in Fig. 4 highlighting the cases what only the R-D model predicts and where both R-D model and oxide trapping effects govern the degradation. While for PNP HBTs, the R-D model limit has already been crossed, for NPN HBTs the base current degradation is still below the R-D limits and thus there are no significant oxide trapping effects. In both cases excellent accuracy is observed.

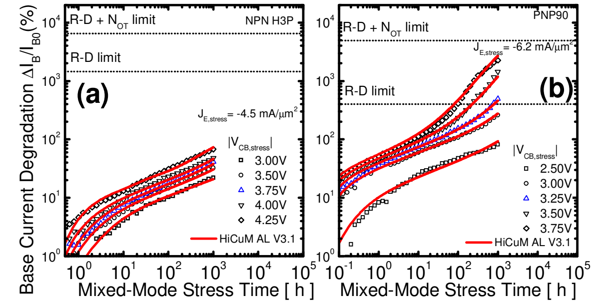

Fig. 4: Comparison between measurement and HiCuM-AL-V3.1 simulation: Evolution of excess base current at V_{BE}= 0.7 V for (a) NPN HBTs under $J_{E,stress}$ of 4.5 mA/μm² for different $V_{CB,stress}$ and (b) PNP HBTs under $J_{E,stress}$ of 6.2 mA/μm² for different $V_{CB,stress}$.

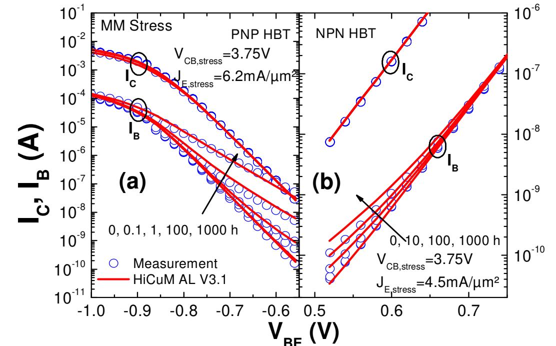

Fig. 5: Comparison between measurement and HiCuM-AL-V3.1 simulation: Gummel plots at different aging intervals for (a) PNP HBTs under $J_{E,stress}$ of 6.2 mA/μm² and $V_{CB,stress}$ of 3.75V and (b) NPN HBTs under $J_{E,stress}$ of 4.5 mA/μm² and $V_{CB,stress}$ of 3.75V.

As a validation, Gummel plots at different stress intervals under a $V_{CB,stress}$ of 3.75V and $J_{E,stress}$ of (a) 6.2 and (b) 4.5 mA/μm² for the PNP and NPN HBTs, respectively, are compared with measurements, as shown in Fig. 5. Initial simulation is performed using a foundry-generated scalable model card followed by re-simulations using extracted HiCuM AL V3.1 aging model parameters, for different aging intervals. Excellent agreement between model and measurement is observed.

In contrast with the results obtained under MM stress, reverse E-B stress shows rather symmetric degradation for both NPN and PNP HBTs, owing to the proximity of hot carriers to the E-B spacer in both cases. Hot carriers generated under reverse E-B stress are quite close to the E-B spacer region compared to that of the C-B junction in mixed-mode stress, thus implying much shorter transit time of hot carriers in the former case. Thus, Figs. 6 (a) and (b) show rather equivalent evolution of the normalized excess base current ($\Delta I_B/I_{B0}$) as a function of aging time for both NPN and PNP HBTs under different reverse E-B stress (3 - 4.5 V), respectively. The limits of the base current degradation are shown here which indicates that in both cases the R-D limit is crossed for a stress voltage of 3.75V and eventually the limit due to R-D and oxide trapping is reached. In both cases good model accuracy is observed.

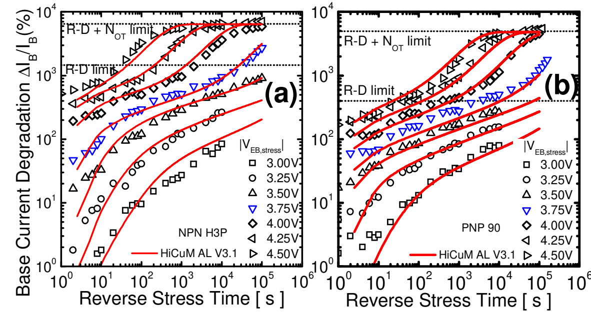

Fig. 6: Comparison between measurement and HiCuM-AL-V3.1 simulation: Evolution of excess base current extracted at V_{BE}= 0.7 V for (a) NPN HBTs and (b) PNP HBTs under different $V_{EB,stress}$ (3 - 4.5V).

The simulation of Gummel plots at different stress intervals under a $V_{EB,stress}$ of 4V for both HBTs are compared with measurements, as shown in Fig. 7. Excellent agreement between model and measurement is also observed for all stress conditions.

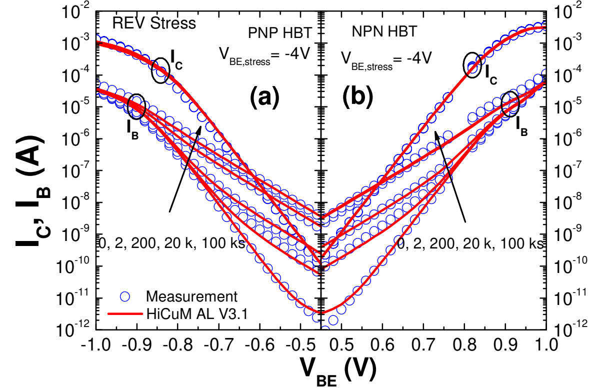

Fig. 7: Comparison between measurement and HiCuM-AL-V3.1 simulation: Gummel plots at different aging intervals for (a) PNP HBTs and (b) NPN HBTs under $V_{EB,stress}$ of 4V.

Finally, the accuracy of bias-dependence captured in the aging model parameter equations (4-9) is validated through comparison between the extracted values (from experimental data) and model simulations for the generation ($K_{F,I}$) and annihilation ($K_{R,I}$) rate constants as well as the oxide trapping time constant ($\tau_{OX,I}$), under different stress conditions studied in this work. It has to be noted that all of these three parameters are simultaneous functions of both stress bias and temperature.

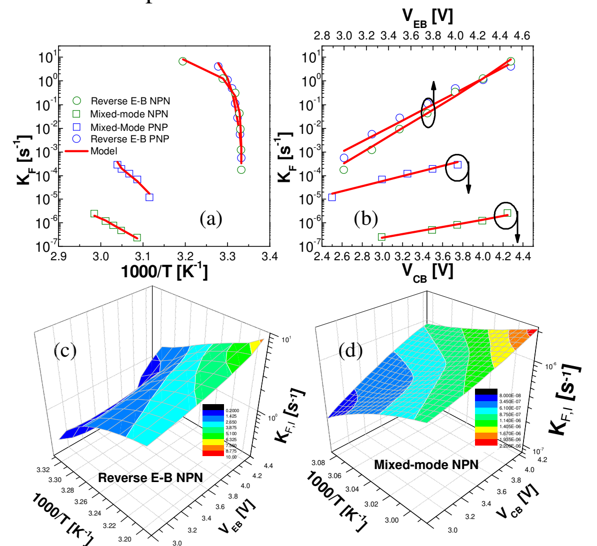

Fig. 8: Evolution of $K_{F,I}$ as an explicit function of (a) inverse of junction temperature and (b) stress bias; Surface plot of $K_{F,I}$ as function of inverse junction temperature and stress bias, under (c) reverse E-B and (d) mixed mode stress.

This dual dependence is shown for $K_{F,I}$ (based on the analytical eqs. (4) - (5)) in Figs. 8 (a) and (b) which depict the comparison between the measurement and

model as explicit functions of (a) inverse of temperature and (b) stress bias, depicting good agreement. To further aid the visualization of the quantity, Figs. 8 (c) and (d) show the 3D surface representation of $K_{F,I}$ as simultaneous functions of both the inverse of temperature and stress bias for an NPN HBT, under reverse E-B and mixed-mode stress conditions, respectively. The higher curvature of the surface in case of the reverse E-B stress highlights the difference between MM and reverse E-B stress, particularly observed for NPN HBTs.

Similarly, Figs. 9 and 10 show the evolution of $K_{R,I}$ and $\tau_{OX,I}$ exhibiting similar dual dependence on bias and temperature. In all cases excellent model accuracy can be observed. Note that the trap annihilation rate, $K_{R,I}$, shows a much weaker stress bias dependence under mixed-mode stress compared to under reverse E-B stress. This disparity is less evident in case of PNP transistors. However, the bias dependence of $K_{R,I}$ is weaker in all cases compared to that of $K_{F,I}$ and $\tau_{OX,I}$ and its evolution is principally governed by its junction temperature dependence.

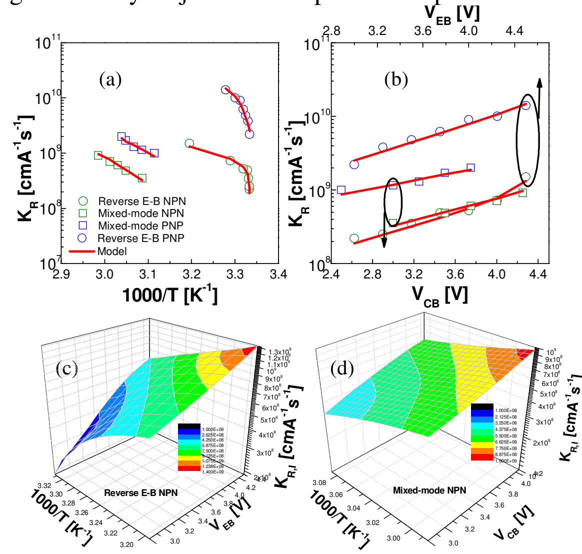

Fig. 9: Evolution of $K_{R,I}$ as an explicit function of (a) inverse of junction temperature and (b) stress bias; Surface plot of $K_{R,I}$ as function of inverse junction temperature and stress bias, under (c) reverse E-B and (d) mixed mode stress.

Interestingly, the magnitudes of $K_{F,I}$ and $\tau_{OX,I}$, which basically signify generation rates of interface and oxide traps, respectively, are quite similar for both type of HBTs under reverse stress, even though they largely differ under mixed-mode stress. Table I lists the extracted aging model parameters for the rate constants depicted in equations (4) - (9). Significantly higher values of the trap generation rate for the PNP HBTs under mixed-mode stress further validates the degradation asymmetry between the two HBT types, owing to different breakdown voltages and the polarity of hot carriers.

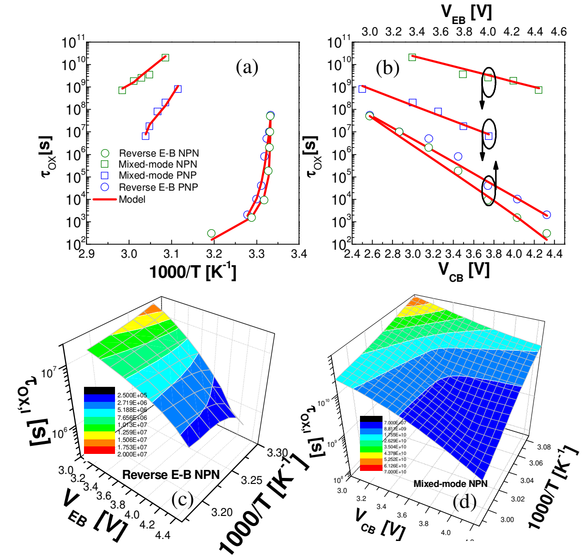

Fig. 10: Evolution of $\tau_{OX,I}$ as an explicit function of (a) inverse of junction temperature and (b) stress bias; Surface plot of $\tau_{OX,I}$ as function of inverse junction temperature and stress bias, under (c) reverse E-B and (d) mixed mode stress.

The elements of the H-diffusion R-C network, however, are only functions of temperature (R_1) or geometry (C_1) and show no evolution with stress bias. The new parameter values E_A, R_{10} are identical regardless of the HBT type and stress conditions. The new set of aging parameters are much more convenient for circuit aging simulations and reliability-aware circuit design.

TABLE I: AGING PARAMETERS OF THE RATE CONSTANTS UNDER DIFFERENT STRESS CONDITIONS

HBT Type	Stress type	K_{F0} (s^{-1})	μ_F (V^{-1})	g_{rate} ($\mu m^2A^{-1}s^{-1}$)	K_{R0} ($cmA^{-1}s^{-1}$)	μ_R (V^{-1})	τ_{OX0} (s)	μ_{OX} (V^{-1})	E_0 (eV)
NPN	Mixed-mode	-	0.95	0.02	1.95×10^{11}	0.65	4.5×10^{10}	2.95	0.24
	Reverse E-B	9×10^{-9}	6.5	-	6.55×10^{10}	1.05	3×10^{14}	8.2	0.24
PNP	Mixed-mode	-	1.2	2.3	1.32×10^{12}	0.45	3.6×10^{9}	3.8	0.24
	Reverse E-B	4.5×10^{-7}	5.6	-	8.0×10^{11}	1.08	5.2×10^{12}	6.8	0.24

4. Conclusion

In this work, we have presented a unified physical and accurate aging compact model implementation, compatible with existing circuit design framework, developed for modern SiGe HBT technologies based on the reaction-diffusion theory of hot-carrier degradation combined with oxide trapping mechanism and a differential form of Fick's law of diffusion. Significant oxide trapping has been observed under accelerated stress bias conditions, particularly under reverse E-B stress, which has been taken into account in the current modeling framework. To the best of knowledge, this is the first notable observation and systematic modeling of this effect in advanced SiGe HBTs. The model implementation is time-invariant and predictive. Moreover, the aging rate constants are implemented as function of stress bias conditions, enabling circuit aging simulation capabilities. The aging model has been validated against long-term aging tests on a complementary 0.25 µm SiGe BiCMOS technology from IHP, yielding very good agreement thus confirming its accuracy and versatility. Significant asymmetry in degradation behavior between NPN and PNP HBTs have been observed under mixed-mode stress conditions that are close to the realistic long-term degradation scenarios in contrast with the reverse E-B stress. The different dynamics of degradation can be attributed to the origin of the hot carriers in the two cases of stress conditions. The fundamental difference between the degradation in NPN and PNP transistors can be attributed to hot carrier polarity and trap activation energy pertaining to each case, demonstrating significantly faster degradation in PNP HBTs. This needs to be taken into account when evaluating the long-term performance of circuits sensitive to HBT mismatch. With its strong physical basis, the proposed aging compact model, HiCuM AL V3.1, is indispensable for ensuring stable circuit operation close to the SOA of the technology, through prediction of reliability-aware circuit architectures.

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References

[1] P. Chevalier, M. Schröter, C. R. Bolognesi, V. d'Alessandro, M. Alexandrova, J. Böck, R. Flückiger, S. Fregonese, B. Heinemann, C. Jungemann, R. Lövblom, C. Maneux, O. Ostinelli, A. Pawlak, N. Rinaldi, H. Rücker, G Wedel and T. Zimmer, "Si/SiGe:C and InP/GaAsSb Heterojunction Bipolar Transistors for THz Applications," *Proc. IEEE*, vol. 105, no. 6, pp. 1035-1050, June 2017, DOI: 10.1109/JPROC.2017.2669087.

[2] C. Mukherjee, B. Ardouin, J. Y. Dupuy, V. Nodjiadjim, M. Riet, T. Zimmer, F. Marc, and C. Maneux, "Reliability-Aware Circuit Design Methodology for Beyond-5G Communication Systems," *IEEE Trans. Device Mater. Rel.*vol. 17, no. 3, pp. 490-506*, Sept. 2017*, DOI: 10.1109/TDMR.2017.2710303.

[3] C. Mukherjee, T. Jacquet, G. G. Fischer, T. Zimmer, and C. Maneux, " Hot Carrier Degradation in SiGeHBTs: A Physical and Versatile Aging Compact Model," IEEE Transactions on Electron Devices, vol. 64, no. 12, pp. 4861-4867, Dec. 2017.DOI: 10.1109/TED.2017.2766457.

[4] J. D. Cressler, *Circuits and Applications Using Silicon Heterostructure Devices,* CRC press 2018. ISBN: 1351834754, 9781351834759.

[5] G. G. Fischer, J. Molina and B. Tillack, "Comparative study of HBT ageing in a complementary SiGe:C BiCMOS technology," *IEEE BCTM*, 2013, pp. 167-170. doi: 10.1109/BCTM.2013.6798167.

[6] U. S. Raghunathan, H. Ying, B. R. Wier, A. P. Omprakash, P. S. Chakraborty, T. G. Bantu, H. Yasuda, P. Menz, and J. D. Cressler, "Physical Differences in Hot Carrier Degradation of Oxide Interfaces in Complementary (n-p-n+p-n-p) SiGe HBTs," *IEEE Trans. Electron Dev.* vol. 64, no. 1, pp. 37-44, Jan. 2017. doi: 10.1109/TED.2016.2631982.

[7] G. G. Fischer and G. Sasso, "Ageing and thermal recovery of advanced SiGe heterojunction bipolar transistors under long-term mixed-mode and reverse stress conditions," *Microelectron. Reliab*. vol. 55, no. 3, pp. 498–507, Mar. 2015, DOI: 10.1016/j.microrel.2014.12.014.

[8] G. G. Fischer, "Analysis and modeling of the long-term ageing rate of SiGe HBTs under mixed-mode stress," 2016 *IEEE Bipolar/BiCMOS Circuits and Technology Meeting* (BCTM), NJ, 2016, pp. 106-109, DOI: 10.1109/BCTM.2016.7738958.

[9] T. Jacquet, G. Sasso, A. Chakravorty, N. Rinaldi, K. Aufinger, T. Zimmer, V. d'Alessandro and C.Maneux, "Reliability of high-speed SiGe: C HBT under electrical stress close to the SOA limit," *Microelectron. Reliab*. vol. 55, no. 9, pp. 1433–1437, 2015, DOI: 10.1016/j.microrel.2015.06.092.

[10] K. O. Jeppson and C. M. Svensson, "Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices," *J. Appl. Phys*., vol. 48,

no. 5, pp. 2004–2014, May 1977, DOI: 10.1063/1.323909.

[11] C. Mukherjee, F. Marc, M. Couret, G. G. Fischer, M. Jaoul, D. Céli, K. Aufinger, T. Zimmer and C. Maneux, “A Physical and Versatile Aging Compact Model for Hot Carrier Degradation in SiGe HBTs under Dynamic Operating Conditions”, *Solid State Electron*. Vol. 163, pp. 107635, 2020. https://doi.org/10.1016/j.sse.2019.107635.

[12] B. Heinemann, R. Barth, D. Knoll, H. Rucker, B. Tillack and W. Winkler, “High-performance BiCMOS technologies without epitaxially-buried subcollectors and deep trenches”, *Semicond. Sci. Technol.* Vol. 22, pp. S153–S157, 2017. DOI:10.1088/0268-1242/22/1/S36.

[13] S. Mahapatra, N. Goel, S. Desai, S. Gupta, B. Jose, S. Mukhopadhyay, K. Joshi, A. Jain, A. E. Islam, and M. A. Alam, "A Comparative Study of Different Physics-Based NBTI Models," *IEEE Trans. Electron Dev.*, vol. 60, no. 3, pp. 901-916, 2013, DOI: 10.1109/TED.2013.2238237.

[14] M.A. Alam, S. Mahapatra, “A comprehensive model of PMOS NBTI degradation”, Microelectronics Reliability, vol. 45, pp. 71-81, 2005, DOI: 10.1016/j.microrel.2004.03.019.

[15] M. Couret, M. Jaoul, F. Marc, C. Mukherjee, D. Céli and C. Maneux, “Scaled formulation for trap generation near the EB spacer oxide interface in SiGe HBTs”, *Solid State Electron*. 2019 (Submitted).

[16] M. Jaoul, C. Maneux, D. Celi, M. Schroter, T. Zimmer, “A compact formulation for avalanche multiplication in sige hbts at high injection levels”, *IEEE Trans. Electron Dev.* Vol. 66**,** pp. 264–270, 2019.