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Vector Modulator Phase Shifters in 130-nm SiGe BiCMOS Technology for 5G Applications

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***Abstract*—This paper presents two approaches for designing vector modulators (VMs) implemented in SiGe BiCMOS technology for 5G applications with 26.5-29.5 GHz band of interest. The first solution exploits reactive matching networks to achieve a peak gain of 7.5 dB, while the second minimizes the area occupation with a core size of $0.32\times0.38\,\text{mm}^2$. Phase shifts from 0° to 360° are achieved with a low phase and gain error.**

***Index Terms*—Vector modulator, phase shifter, 5G, SiGe, BiCMOS.**

I. Introduction

With the introduction of the fifth-generation (5G) network, around the world, several mm-wave bands have been released for commercial use. Compared to the ones used within the fourth generation (4G), these bands provide wider bandwidths and increase spatial reuse. Furthermore, the improved aperture to wavelength ratio allows the implementation of phased array antenna systems (PhAA) in a reduced form factor [1]. All these aspects will help to accommodate the envisioned need for ever-increasing data throughput. In particular, phased arrays allow focusing the wave in a very narrow beam. The beam can be steered electronically by controlling the single-phase shifts. The bottleneck for these systems is the difficulty in providing precise phase shifts. So, the design of accurate phase shifters with low consumption, adequate area occupation, and relevant gain is currently of keen interest. Several designs have been proposed in literature, and they have been implemented in different ways; however, the main distinction is between the passive and the active ones. Passive phase shifters [2]–[4] achieve high linearity at the expenses of high insertion loss and area overhead. Instead, the active ones have lower linearity [5]–[9], nevertheless, the possibility of compact solutions, low losses (or perhaps gain), and gain tuning, which can be used for amplitude tapering [10], make the latter favorite candidates for mm-wave PhAAs. In this paper, the designs of two active phase shifters fabricated in IHP BiCMOS technology, one designed for high gain and the other for low area occupation, are presented. The remainder of this paper is organized as follows. Section II describes the architecture of the two VMs. Section III analyzes the two designs. Section IV comments on the measurement results, and Section V concludes the paper.

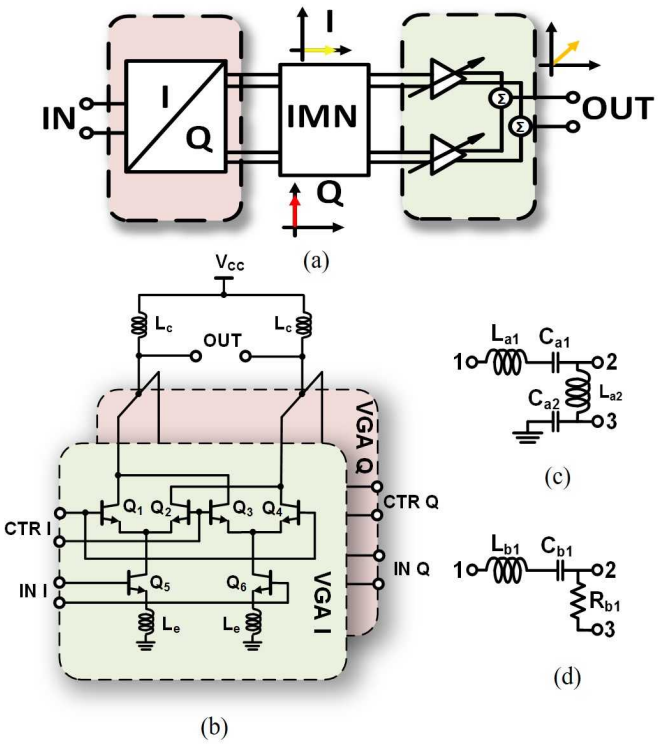

Fig. 1: VMs block diagram (a) with the adder schematic (b), an IMN for high gain (c) and compact (d) solutions.

II. Vector Modulator Architecture

The block diagram of the VMs is presented in Fig. 1a, where an in-phase/in-quadrature (I/Q) splitter and a differential adder are separated through an interstage matching network (IMN). A differential signal feeds the I/Q splitter based on a differential RC-CR poly-phase-filter (PPF). The PPF is made of a 100 Ω resistor and a 45 fF capacitor, while the differential adder consists of two variable gain amplifiers (VGAs), shown in Fig. 1b. The VGAs are made of a differential current steering topology based on Gilbert-cell. The quadrature signals are then summed vectorially in the current domain at the output nodes, generating the desired gain and phase shift.

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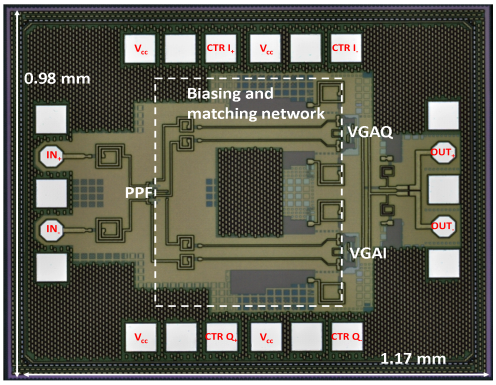
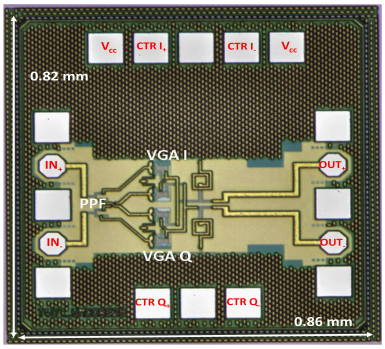


(a)



(b)

Fig. 2: Micrograph of the chips, (a) the high gain VM and (b) the compact VM.

III. Vector Modulators Design

The proposed VMs have been designed to target high gain and low area occupation respectively. For this reason, the IMNs are different while other components are identical. The input matching network, not shown in Fig. 1a, consists of series inductors and it is not present in the low area occupation design. For linearity purposes, a 20 pH degeneration inductor (L_e) is present on the emitters of the differential input pair. The current steering transistors of each VGA are biased from the outside by means of a voltage divider. The control voltages are swept in a differential fashion, dictating the gain weight at the single VGA output. In order to decrease the noise figure of the overall vector modulator, the input transistors have been split into two heterojunction bipolar transistors (HBTs) [11] , each of them having eight fingers. Moreover, each transistor of the steering stage consists of a single eight fingers HBT.

A. High gain vector modulator

To improve the vector modulator gain, we propose an input matching network before the PPF consisting of a series inductor and, more importantly, a reactive IMN. The latter is reported in Fig. 1c, where node 1 is the PPF output, node 2 the input of the VGA's differential pair (namely IN in Fig. 1), and node 3 is attached to the biasing network. This IMN includes two inductors, L_{a1}=360 pH and L_{a2}=200 pH, and a metal-insulator-metal capacitor (MIM) C_{a1}=100 fF. The capacitor C_{a2}=10.5 pF serves as RF ground on the node 3.

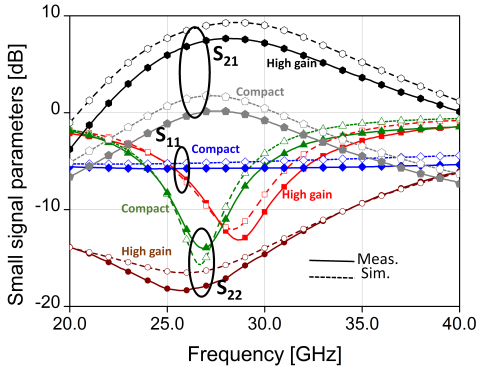


Fig. 3: Small signal peak gain: measurements and simulations.

B. Compact vector modulator

On the system level, the reduction of the area is a crucial challenge. Thus, a compact solution has been designed, shrinking the dimensions and without matching the input. The IMN is shown in Fig. 1c, where C_{b1} has been placed as DC-block. Instead, the inductance L_{b1} embeds the interconnection parasitic given by the path from the PPF to the VGA. R_{b1} is a 2 kΩ resistor, which acts as an open circuit for the high frequencies and isolates the biasing network from the RF. The nodes have consistent naming with subsection A.

IV. Measurement Results

The two circuits have been fabricated in IHP BiCMOS SG13S 130 nm technology and are presented in Fig. 2; In Fig. 2a the high gain VM is depicted where the matching and biasing network occupies an area of $0.4 \times 0.6\,\mathrm{mm}^2$, increasing the total area to $0.98 \times 1.17\,\mathrm{mm}^2$. Fig. 2b shows the compact VM where the absence of input matching and IMN makes the design compact. The core size is $0.32 \times 0.38\,\mathrm{mm}^2$ comprehensive of the PPF; while, the chip size is limited by the pads and it arises to $0.82 \times 0.86\,\mathrm{mm}^2$. Small signal measurements have been performed using two differential probes with 100 µm pitch and a R&S® vector network analyzer ZVA67. In order to control the gain of the single VGAs, on-chip resistive voltage dividers are used, controlled by an external programmable voltage source. Both designs are supplied with 2.5 V. The high gain consumes 42.5 mW as opposed to the compact design which consumes 27.5 mW. The small signal peak gain is shown in Fig. 3, where the simulated and measured results match closely. The high gain solution is showing a peak gain 7.5 dB higher than the compact solution. The return losses have been shown in Fig. 3, where the high gain VM presents return losses better than 10 dB in input and 15 dB in output within the interest band; instead, the compact solution presents an input return loss better than 5 dB and the output return loss is still better than 8 dB. Fig. 4 presents the polar plot of both circuits; the high gain VM has a max

TABLE I: Perfomances and comparison with the state-of-the-art VMs.

	This Work		[5]	[6]	[7]	[8]	[9]
	High gain	**Compact**					
Technology	130 nm SiGe	130 nm SiGe	130 nm SiGe	180 nm SiGe	180 nm CMOS	55 nm CMOS	28 nm CMOS
Frequency band [GHz]	26.5-29.5	26.5-29.5	60-80	6-18	27-33	26-30	78.8-92.8
Power consumption [mW]	42.5	27.5	34.8	10.56	6.6	2.3	21.6
rms phase error [deg]	<4.2	<3.5	<6	<5.6	<4	-	<11.9
rms gain error [dB]	<0.7	<1	<1	<1	<1.3	<0.42	<2
Average gain [dB]	2.3	-4.4	-	16.5-19.5[1]	-5.17	-7.3	2.3[2]
Number of bits	4	4	4	5	4	-	4
Area [mm^2]	1.15	0.71	-	0.9	0.45[3]	0.86	0.12[4]

[1] at 7.5-12.5 GHz with active balun, [2] at center frequency, [3] without pads, [4] core

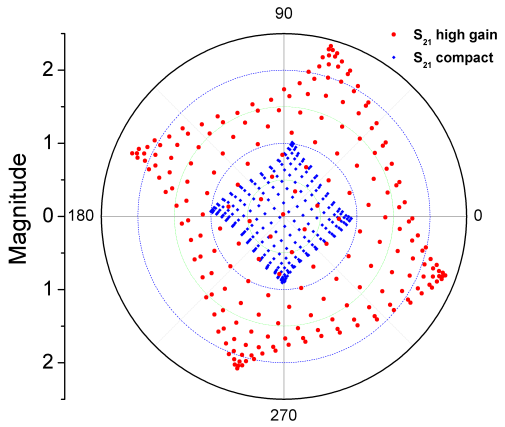


Fig. 4: High gain and compact VM polar plot at 28 GHz.

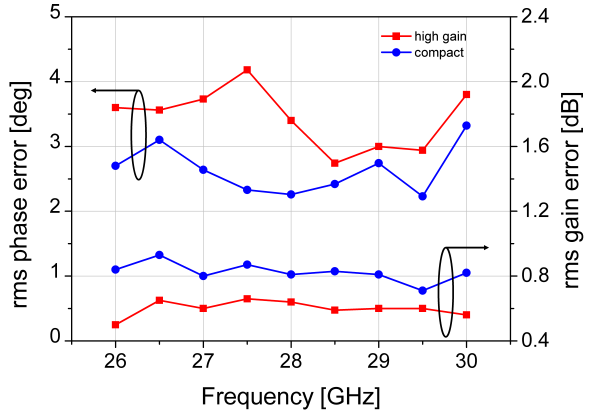


Fig. 5: Gain and phase error of the proposed VMs.

average gain circle radius of 1.3 in magnitude; while, for the compact solution the radius is 0.6. As shown in Fig. 5, the high gain VM exhibits a max root-mean-square (rms) phase and gain error across frequency better than 4.2° and 0.7 dB respectively, while the compact one shows a max rms phase error of 3.5° and a max rms gain error of 0.92 dB. Table I shows the comparison between the state-of-the-art VMs.

V. Conclusion

This work presents two different approaches for realizing VMs for 5G applications with 26.5-29.5 GHz band of interest. The first reaches 7.5 dB peak gain at expenses of area occupation, while the second minimizes the area occupation with a core dimension of $0.32 \times 0.38\,\mathrm{mm}^2$, even if its peak gain is only 0 dB. The results are in line with state of the art, with a better rms phase error and a comparable gain error.

Acknowledgment

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