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3.2-mW Ultra-Low-Power 173–207-GHz Amplifier With 130-nm SiGe HBTs Operating in Saturation

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***Abstract*— This article presents an ultra-low-power silicon germanium heterojunction bipolar transistor (SiGe HBT) amplifier operating at 200 GHz. The amplifier consists of three cascaded gain-cell stages and was implemented in an experimental 130-nm SiGe HBT technology with peak f_T/f_{max} of 460/600 GHz. In order to achieve the demonstrated extremely low dc power dissipation, the circuit was designed with transistors operating at forward-biased base–collector junction voltage (V_{BC}). With 1.3-V supply voltage ($V_{BC} \approx 0.2$ V), this amplifier exhibits a peak gain of 23.5 dB at 180 and 205 GHz with 34-GHz 3-dB bandwidth (BW) from 173 to 207 GHz, consuming 3.2-mW static dc power. Even with a supply voltage of 0.7 V ($V_{BC} \approx 0.5$ V), this amplifier still operates with a peak gain of 18.3 dB at 175 GHz, dissipating an extremely low dc power of 1.73 mW. Compared with the previously reported low-power amplifiers operating around 200 GHz, this article achieves the highest linear gain relative to the dc power consumption with an improvement factor of ten, as well as highly competitive performances in terms of noise figure and 3-dB BW.**

***Index Terms*— Amplifier, low power, millimeter (mm)-wave (*G*-band), saturation, silicon germanium heterojunction bipolar transistor (SiGe HBT).**

I. Introduction

THERE has been a steadily increasing interest in millimeter (mm-) and sub-mm-wave frequency applications, such as security imaging, high-speed wireless communication links, health, and space exploration [1], which are predicted to play vital roles in modern society. The continuous development of silicon germanium heterojunction bipolar transistors (SiGe HBTs) and the corresponding BiCMOS technology has led to transistors with a peak power gain related maximum oscillation frequency f_{max} of 720 GHz [2] and the integration with 55-nm CMOS [3]. This and the prediction of beyond THz cutoff frequencies in [4] have made SiGe HBT technology a competitive candidate for mm- and sub-mm-wave circuit and system design [5]. One of the core demands for future wireless communication circuits and systems will be the low dc power consumption, which requires a sufficient reduction of the supply voltage (V_{supply}) and current. Since operating SiGe HBTs up to a moderately forward-biased base–collector voltage (V_{BC}) does not necessarily result in significant excess charge in the collector, the current gain cutoff frequency (f_T) still remains at several hundreds of GHz. Hence, the investigation of mm- and sub-mm-wave SiGe HBT-based low-power circuits operating in saturation appears intriguing.

Some low-power mm-wave SiGe HBT-based circuits have been reported recently. In the W-band, several circuits with forward-biased V_{BC} were realized: a tripler with −3.8-dB conversion gain (CG) and 6.4-mW dc power [6]; a downconversion mixer with 9.6-dB CG and 12-mW dc power [7]; two amplifiers with 14.3- and 12-dB gain, consuming 2.8- and 12-mW dc power, respectively [8]. The transistors of these circuits were biased close to peak f_T at medium-to-high collector current density (J_c). For the G-band, a 40-mW downconversion mixer with 5.5-dB CG was designed in [9], and several G-band amplifiers were reported in [10]–[12] with 10–17-dB gain and a minimum dc power consumption of 6.4 mW. However, these G-band circuits were still biased at reverse V_{BC}. To the best of our knowledge, amplifiers with forward-biased V_{BC} operating beyond 110 GHz have not yet been reported.

This article presents a 173–207-GHz low-power amplifier based on an experimental 130-nm SiGe technology, which features high-speed n-p-n-HBTs with peak (f_T, f_{max}) = (460, 600) GHz. For significantly reducing the dc power dissipation (P_{dc}) and investigating the low-power performance of circuits with transistors operating in saturation, this amplifier is designed with forwarded-biased V_{BC} and also at relatively low J_c region. The first-pass success of fabricating this circuit and the detailed analysis given in this article are possible thanks

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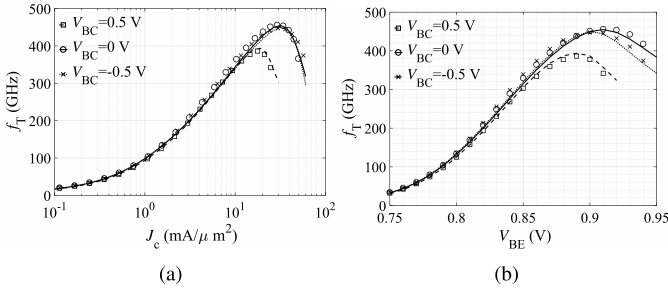

Fig. 1. Measured (marker) and simulated (line) f_T versus (a) J_c and (b) V_{BE} with different V_{BC} values for the transistor with the emitter window area of $A_{E0} = 2 \times 1\ \mu m \times 0.1\ \mu m$.

to the accuracy of the compact model HICUM/L2 [13] in the saturation region.

This article is organized as follows. In Section II, the key features and improvements of the fabrication process are introduced. In Section III, the gain-cell design is described, including the bias and size selection of the transistor, the analysis of G_m-boosting inductors, the gain-cell stabilization, as well as the noise reduction. Circuit design and implementation are presented in Section IV, which consists of the layer selection, the G_m-boosting inductor realization, and the design of wideband matching networks, as well as the zero-ohm impedance transmission line (ZTL). Measurement results are compared with simulation data and also with the existing state of the art in Section V. Summary and conclusion are provided in Section VI. All data are shown for a chuck temperature of 22 °C.

II. Technology

The circuit described in this article was fabricated in an experimental SiGe BiCMOS technology run at IHP. Starting from IHP's standard 130-nm BiCMOS technology SG13G2 [14], several HBT related improvements developed during the EU DOTSEVEN project [5] were employed to boost the high-speed performance. First, an optimized vertical profile was utilized, including new processes for the emitter formation and for the selectively implanted collector. Furthermore, the reduction of the emitter–base spacer width, the emitter window width, and the resistivity of the external base regions, as well as a low-temperature back end with NiSi contribute to a lower base resistance. In contrast to [2], where peak f_T/f_{max} values of 505/720 GHz were shown, no millisecond annealing was applied here. Fig. 1(a) demonstrates the measured and simulated f_T versus J_c with different V_{BC} values for the test devices with the an emitter window area of $A_{E0} = 2 \times 1\ \mu m \times 0.1\ \mu m$ fabricated on the same die as the circuit. As shown in Fig. 1, the peak f_T is around 460 GHz at $V_{BC} = 0$ V and remains beyond 380 GHz even at $V_{BC} = 0.5$ V, which enables the low-power design of this article.

The back-end process of this technology offers seven metal layers in total, providing a high degree of freedom for routing the microstrip lines (MLs), striplines (SLs), and coplanar waveguides (CPWs) with different dielectric thicknesses. For sustaining higher current densities and the fabrication of high-quality passives, two thick top metal layers are available. Moreover, the essential passive components, such as the metal–insulator–metal (MIM) capacitors between TM1 and M5 with 1.5-fF/μm^2 density and three poly-silicon resistors, are well modeled.

III. Gain-Cell Design

A. Bias and Transistor Selection

The cascode configuration has been chosen in this article due to its lower Miller-effect [15], higher isolation, and higher gain [16]. The first challenge in designing this amplifier is the bias and size selection of the transistor. For maximizing performance, small-signal amplifiers are typically biased close to peak f_T with negative V_{BC}. However, the tradeoff between the best possible performance and the lowest possible dc power dissipation requires either V_{supply} or the collector current (I_c) to be reduced. Fortunately, SiGe HBTs still provide several hundreds of GHz peak f_T even with moderately forward-biased V_{BC}, which makes a substantial reduction of V_{supply} feasible. In addition, the position of peak f_T shifts with positive V_{BC} toward lower J_c (see Fig. 1), which is also advantageous for the decrease of I_c. Nevertheless, this reduction might not suffice if I_c at peak f_T (and minimum A_{E0}) is still too high for minimizing P_{dc}. By biasing the transistors of this technology at around 270 GHz, corresponding to a shift of J_c from 30 to 6 mA/μm^2, P_{dc} can indeed be further reduced. Apart from that, f_T decrease with positive V_{BC} is also somewhat alleviated in this region, which enables a possibly even lower V_{supply} (i.e., larger V_{BC}). According to simulations with only a single noise source turned on in the HBT compact model, transfer current shot noise turned out to be by far the dominating component. Thus, a lower selected J_c (i.e., lower I_c) is beneficial for reducing the noise figure. Eventually, the bias conditions were chosen as $V_{supply} = 1.3$ V, bottom base $V_{BB} = 0.84$ V, and upper base $V_{UB} = 1.5$ V in order to minimize P_{dc} while maintaining the competitive performances.

At the time of design, the process offered SiGe HBTs with just a single emitter area, which was extendable to a larger transistor by multiplying the same layout N_x times up to 10, i.e., $A_{E0} = N_x \times 1\ \mu m \times 0.1\ \mu m$. A larger N_x and, thus, an increase of I_c directly lead to an increase of P_{dc} at the same V_{supply}. To determine the optimum size of the device, a figure of merit M is defined as

$$\mathrm{M} = \frac{\mathrm{MAG/MSG}(1) \cdot oP_{1\,\mathrm{dB}}(\mathrm{mW})}{F_{\min}(1) \cdot P_{\mathrm{dc}}(\mathrm{mW})} \tag{1}$$

considering besides P_{dc} also the maximum available gain/maximum stable gain (MAG/MSG), the minimum noise factor F_{min}, and the output 1-dB compression point $oP_{1\,dB}$.

M is calculated based on the simulation of the ideal cascode stage with devices having a different N_x at 200 GHz and with the previously selected bias conditions. As shown in Fig. 2(a), M is highest for transistors with N_x between 1 and 4, indicating a better tradeoff among the various circuit parameters. As for the front-end amplifier, noise, dc, and small-signal performances are more critical, the large-signal performance is regarded as a secondary goal. Therefore, a smaller device size is preferred due to its lower P_{dc} and noise.

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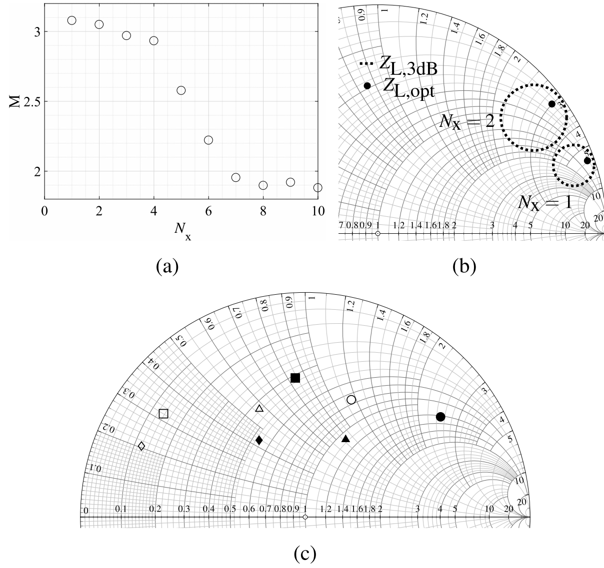

Fig. 2. Ideal cascode stage. (a) Simulated figure of merit M with different N_x. (b) Optimum $Z_{L,\text{opt}}$ and −3-dB contours of constant available gain of devices with $N_x = 1$ and $N_x = 2$. (c) Optimum source impedances for conjugate (open symbols) and minimum noise (filled symbols) matching devices with $N_x = 1$ (circle), 2 (triangle), 3 (square), and 4 (diamond). The simulation frequency is 200 GHz and the bias conditions are the same as specified before.

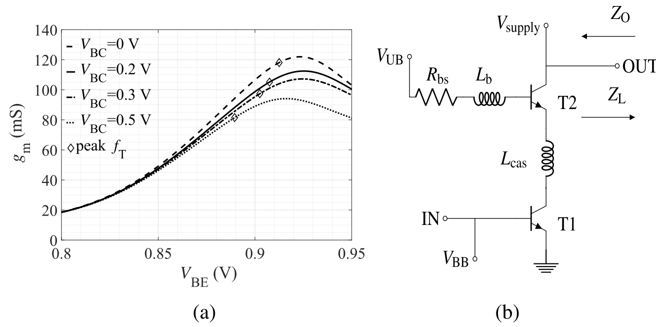

Fig. 3. (a) Simulated g_m versus V_{BE} with different V_{BC} values for the transistor with chosen emitter area. (b) Simplified circuit schematic of the proposed gain-cell.

However, the single-finger device provides a fairly large imaginary part of the output impedance Im$\{Z_O\}$, making the realization of broadband matching around $Z_{L,\text{opt}}$ (Z_O^*) quite difficult, as can be implied by the small size of the simulated −3-dB contour of constant available gain at 200 GHz in Fig. 2(c). Besides, Fig. 2(c) demonstrates the optimum source impedance for both conjugate (power) matching and minimum noise matching of the devices with N_x between 1 and 4. As can be seen, $N_x = 2$ is the best choice because the conjugate and minimum noise matching points are closest to each other and the real part of both points is close to 50 Ω, which simplifies the input matching network. Hence, $N_x = 2$ has been employed in this article.

B. G_m-Boosting L_{cas} and L_b

Fig. 3(a) demonstrates the simulated transconductance g_m of the previously selected device with different V_{BC} values. Due to the aggressive reduction of J_c, the transconductance g_m of

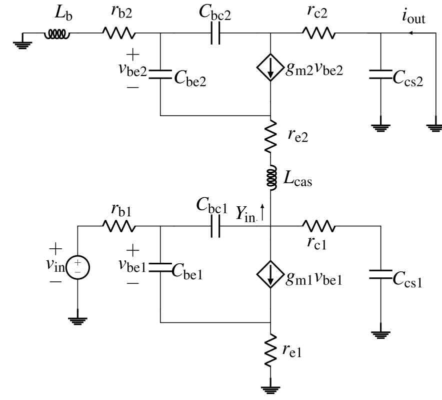

Fig. 4. Simplified small-signal equivalent circuit of the gain-cell with L_{cas} and L_b.

the transistor with the selected bias conditions is decreased. Thus, the MAG/MSG of the traditional cascode stage becomes insufficient and has to be enhanced by special measures. In this article, two inductors L_{cas} and L_b are utilized simultaneously to boost the small-signal short-circuit transconductance G_m of the gain-cell and, in turn, also its MAG/MSG [17], [18]. Besides, a small resistance R_{bs} is implemented for stability reasons. The circuit schematic of the proposed gain-cell is presented in Fig. 3(b), where the bias network is omitted.

Aiming to evaluate the impact of the two G_m-boosting inductors, the simplified small-signal equivalent circuit for the conventional cascode stage with L_{cas} and L_b is shown in Fig. 4. For analysis purposes, the simplified equivalent circuit retains only the most important elements: total base–collector capacitance C_{bc}; total base–emitter capacitance C_{be}; total collector-substrate capacitance C_{cs}; and total base–collector and emitter resistances r_{bs}, r_c, and r_e, respectively. G_m of the stage is defined as the ratio of output current i_{out} to input voltage v_{in} under the condition of zero output voltage v_{out} (shorted)

$$G_m = \left.\frac{i_{\text{out}}}{v_{\text{in}}}\right|_{v_{\text{out}}=0}. \tag{2}$$

The loaded voltage gain v_g of the cascode stage is approximated by [15]

$$|v_g| \approx G_m(Z_{\text{O}} \| Z_{\text{L}}) \tag{3}$$

where Z_{O} is the output impedance looking into the cascode stage and Z_{L} is the load impedance [see Fig. 3(b)]. As shown, v_g can be enhanced by either boosting G_m or Z_{O}. Compared with the CE stage, the higher gain of the cascode stage is mainly achieved by increasing Z_{O} with a factor of β_0, where β_0 is the small-signal current gain of the first CE transistor. The stacked cascode configuration with one or two additional CB transistors as implemented in [19] further enhances Z_{O} but consumes more dc power due to the required higher supply voltage. As a result, G_m should be boosted in order to improve v_g while keeping P_{dc} as low as possible.

Based on Fig. 4 and neglecting all the resistance elements and two inductors, G_m of the conventional cascode can be

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TABLE I
VALUE OF PARAMETERS AT SELECTED BIAS CONDITIONS

g_{m1}	g_{m2}	C_{bc1}	C_{bc2}	C_{be2}	C_{cs1}
40.5 mS	48 mS	3.9 fF	4.05 fF	18.4 fF	2.7 fF

expressed as

$$G_m = \frac{g_{m2}(g_{m1} - j\omega C_{bc1})}{g_{m2} + j\omega(C_{bc1} + C_{be2} + C_{cs1})} \tag{4}$$

where ω is the angular operating frequency. Adding only L_{cas} to the calculation changes (4) to

$$G_m = \frac{g_{m2}(g_{m1} - j\omega C_{bc1})}{g_{m2}\left[1 - (\frac{\omega}{\omega_{r1}})^2\right] + j\omega\left[C_{bc1} + C_{cs1} + C_{be2}\left[1 - (\frac{\omega}{\omega_{r1}})^2\right]\right]} \tag{5}$$

with

$$\omega_{r1} = \frac{1}{\sqrt{L_{cas}(C_{cs1} + C_{bc1})}}. \tag{6}$$

As can be seen by comparing (4) with (5), for sufficiently small values of L_{cas} (i.e., for $\omega_{r1} > \omega$), the resonance at ω_{r1} leads to a reduction of the denominator in (5), and thus, results in an enhancement of G_m and a higher voltage gain.

Similarly, including L_b only in the calculation, (4) changes to

$$G_m = \frac{\left(g_{m2} + j\omega\frac{C_{be2}}{1-(\omega_{r3}/\omega)^2}\right)(g_{m1} - j\omega C_{bc1})}{g_{m2} + j\omega\left[C_{be2} + \frac{C_{bc1}+C_{cs1}-(\omega/\omega_{r2})^2}{1-(\omega/\omega_{r3})^2}\right]} \tag{7}$$

with

$$\omega_{r2} = \frac{1}{\sqrt{L_b(C_{be2} + C_{bc2})(C_{bc1} + C_{cs1})}} \tag{8a}$$

$$\omega_{r3} = \frac{1}{\sqrt{L_b C_{bc2}}}. \tag{8b}$$

In order to observe the contribution of two inductors quantitatively, (5) and (7) are evaluated using the parameter values listed in Table I, which are extracted based on previously selected bias conditions. Calculated $|G_m|$ with varying L_{cas} and L_b is shown in Fig. 5(a) and (b), respectively. As demonstrated, the resonances between the two inductors and the corresponding capacitances enable the improvement of $|G_m|$ by about a factor 3 and 1.5 at 200 GHz, respectively, if the resonance is adjusted slightly beyond 200 GHz. Similar improvements can also be observed in Fig. 5(c) and (d) by simulating $|G_m|$ of an ideal cascode stage with varying L_{cas} and L_b using transistors with $N_x = 2$ and previously specified bias conditions. Similarly, an enhancement of $|G_m|$ by a factor around two at 200 GHz is achieved with L_{cas} and L_b. Compared with the simulation, the numerical evaluation of (5) and (7) presents a reasonable estimation for the variation of $|G_m|$ and is a good starting point for selecting the two inductor values in the complete gain-cell design.

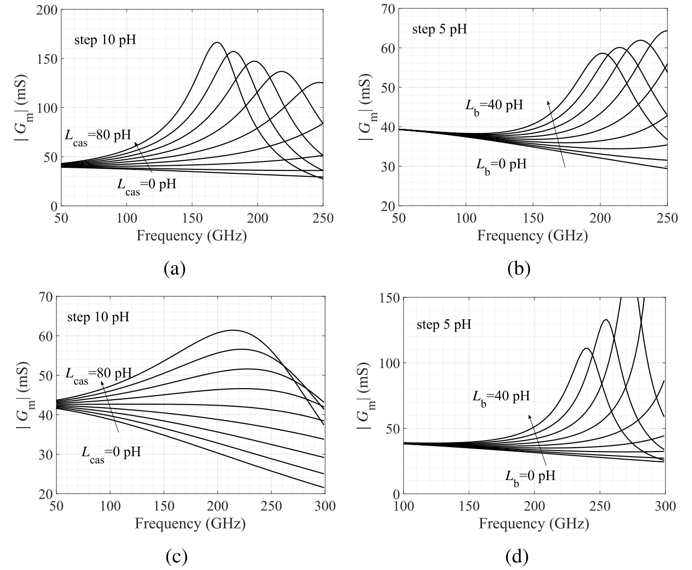

Fig. 5. (a) and (b) Calculated $|G_m|$ of (5) and (7) and (c) and (d) simulated $|G_m|$ for ideal cascode stage with L_{cas} and L_b varied from 0 to 80 and 0 to 40 pH, respectively. Device size of the stage and bias conditions is the same as specified before.

C. Stability Analysis

The instability of gain-cell may occur due to the positive feedback caused by L_b [20], which can be explained by analyzing the input admittance Y_{in} looking into the base of the upper transistor (see Fig. 4). Y_{in} can be expressed after neglecting resistive components, as

$$Y_{in} = \frac{(g_{m2} + j\omega C_{be2})[1 - (\omega/\omega_{r3})^2]}{[1 - (\omega/\omega_{r4})^2]} \tag{9}$$

with

$$\omega_{r4} = \frac{1}{\sqrt{L_b(C_{be2} + C_{bc2})}}. \tag{10}$$

The boundary condition of the real part of Y_{in} can be written as

$$\begin{cases} Re\{Y_{in}\} > 0, & \omega_{r3} > \omega_{r4} > \omega \\ Re\{Y_{in}\} < 0, & \omega_{r3} > \omega > \omega_{r4} \\ Re\{Y_{in}\} > 0, & \omega > \omega_{r3} > \omega_{r4}. \end{cases} \tag{11}$$

As shown, Y_{in} becomes negative if L_b is large enough to make $\omega_{r3} > \omega > \omega_{r4}$, which predicts the potential instability. On the other hand, L_b cannot be too large since $|G_m|$ will rapidly decrease after resonance, as can be seen in Fig. 5(b) and (d). As a result, the value of L_b should be sufficiently small, so that the condition $\omega_{r3} > \omega_{r4} > \omega$ is fulfilled to simultaneously boost the gain and make Y_{in} positive. Fig. 6 demonstrates the simulated real part of Y_{in} of the ideal cascode stage with L_b varied from 0 to 30 pH. As shown, a small resistor R_{bs} is helpful to avoid Y_{in} from becoming negative. Aiming to overcome the gain degradation due to a forward-biased V_{BC}, L_b needs to be carefully selected. Therefore, R_{bs} is added to mitigate potential instability due to fabrication tolerances.

D. Noise Analysis

In SiGe HBTs, the thermal noise of the resistive components, especially the base resistance, and the shot noise of

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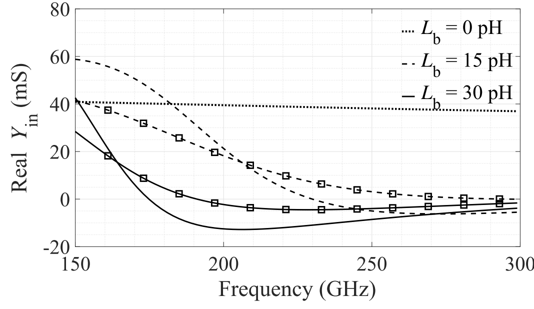

Fig. 6. Simulated real part of Y_{in} versus frequency of the ideal cascode stage with L_b varied from 0 to 30 pH and with (marker) and without (line) $R_{\text{bs}} = 4\Omega$. Device size of the stage and bias conditions is the same as specified before.

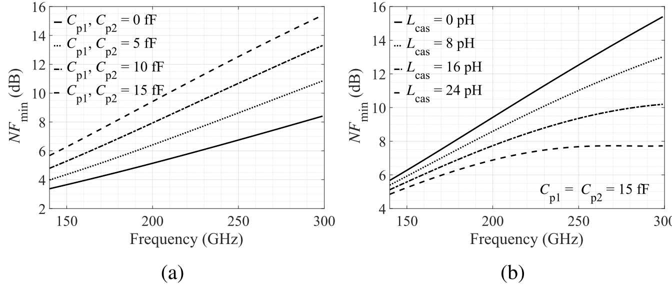

Fig. 7. Simulated NF_{min} versus frequency for the ideal cascode stage with (a) C_{p1} and C_{p2} varied from 0 to 15 fF and (b) L_{cas} varied from 0 to 24 pH with 15 fF for C_{p1} and C_{p2}. Device size and bias conditions are the same as specified before.

the transfer current source are the main contributors. The noise factor of the cascode stage with stabilizer R_{bs} can be approximately expressed as [21]

$$F = 1 + F_{\text{CE}} + (F_{\text{CB}} + F_{\text{Rbsn}})\left(1 + \left(\frac{\omega(C_{p1} + C_{p2})}{g_m}\right)^2\right) \tag{12}$$

where C_{p1} and C_{p2}, respectively, are the sum of the parasitic capacitances at the collector of the CE transistor and the emitter of the CB transistor, respectively; F_{Rbsn} is the noise term of R_{bs}; and F_{CE} and F_{CB}, respectively, represent the sum of the thermal noise of base and emitter resistances and the shot noise of the transfer current of the CE and CB transistors, respectively. According to (12), the noise contributions from the upper CB transistor and R_{bs} are amplified by $(C_{p1}+C_{p2})$. Fortunately, the impact from the parasitic capacitances can be reduced by forming a resonance with L_{cas} at the operating frequency with a maximal reduction for [22]

$$L_{\text{cas,opt}} = \frac{C_{p1} + C_{p2}}{\omega^2 C_{p1} C_{p2}}. \tag{13}$$

As shown in Fig. 7(a), the minimum noise figure NF_{min} for an ideal cascode stage with different values of C_{p1} and C_{p2} under the same bias condition as mentioned previously degrades with frequency. At 200 GHz, approximately 4.5-dB degradation of NF_{min} is observed with 15 fF for C_{p1} and C_{p2}. This degradation can be alleviated by introducing L_{cas}. At 200 GHz, around 3-dB compensation of NF_{min} is observed in Fig. 7(b) for $L_{\text{cas}} = 24$ pH.

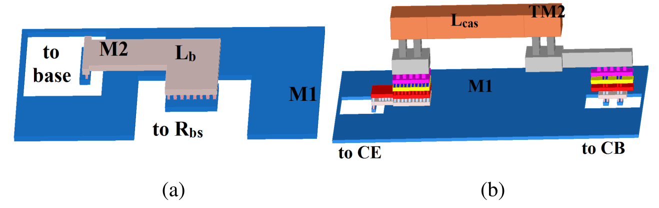

Fig. 8. 3-D views of (a) L_b and (b) L_{cas} together with via transitions.

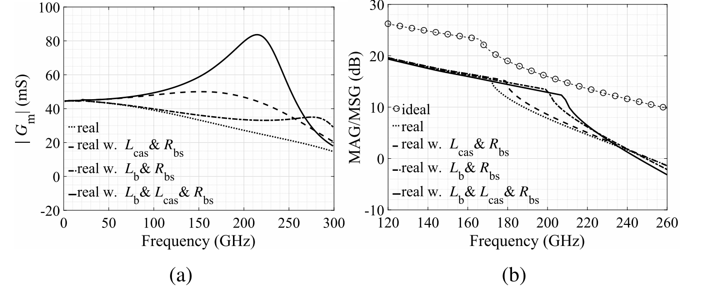

Fig. 9. Simulated (a) $|G_m|$ and (b) MSG/MAG of the complete gain-cell with and without L_{cas} and L_b. Device size of the stage and bias conditions is the same as specified before.

IV. Circuit Design and Implementation

The layout scheme needs to be considered first. The topmost and thickest metal layer TM2 with 3-μm thickness and the lowest sheet resistance is selected as the main routing layer for reducing the overall propagation loss at high frequencies. The bottommost layer M1 is used as a ground plane to minimize the ratio W/d of transmission line (TL) width W to distance d between signal and ground layers. A smaller W/d results in a wider range for the characteristic TL impedance (Z_c), which, in turn, increases the degree of freedom for designing wideband matching networks as discussed later.

A. Design of L_{cas} and L_b

The two inductors L_b and L_{cas} are realized here as a short TL with a specific length. In the process technology used, a transition from M1 to TM2 introduces around 1–4-fF shunt capacitance, 2–5-pH series inductance, and 1–4-Ω series resistance, depending on the number of vias used [16]. These parasitics have a significant impact on the frequency range of interest here. Thus, during circuit design and optimization, they have been taken into account by electromagnetic (EM) simulation.

The 3-D view of L_b and L_{cas} together with their connections to the transistor terminals is shown in Fig. 8. Since L_b is very sensitive to the above-mentioned parasitics, it is realized by M2 using only the via the transition from M1 to M2 [see Fig. 8(a)]. In contrast, as shown in Fig. 8(b), L_{cas} has been realized with TM2 due to the requirements for a high maximum current density and low loss (voltage drop) in the collector current path. The actual size of the two inductors was optimized by EM simulation of the entire gain-cell, including the two inductors and all connection structures.

Fig. 9(a) and (b) presents the simulated $|G_m|$, as well as MSG/MAG of the complete gain-cell for various scenarios.

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Compared with the ideal cascode stage, the involved parasitics of the metal layer and via transitions decreases MSG/MAG by around 6–8 dB. As the gain performance of the amplifier is very critical, the value of these two inductors was selected with particular emphasis on G_m and the corresponding MSG/MAG enhancement, while the NF was regarded as the secondary goal. As discussed before, since the choice of L_b is sensitive and L_b needs to be sufficiently small, L_{cas} is selected first with a relatively large value and as close to $L_{\text{cas,opt}}$ as possible.

After optimization, for L_b, an M2 TL with 2-μm width and 35-μm length gave a value of 10 pH, while for L_{cas}, a TL of TM2 with 3-μm width and 35-μm length resulted in a value of 21 pH, improving the $|G_m|$ from 27 to 80 mS by adjusting the peak at around 210 GHz [see Fig. 9(a)]. Because of the extra parasitic capacitance introduced by via transitions and metal layers, smaller values for L_b and L_{cas} are required to achieve the resonance frequencies of interest, as compared with the estimations from Fig. 5. According to Fig. 9(b), implementing the two inductors improves the MSG/MAG of the complete gain-cell significantly by around 3 dB up to 210 GHz, which is the targeted upper side of the 3-dB bandwidth (BW). Moreover, $NF_{\min}$ is reduced by approximately 1.5 dB through L_{cas}. Larger values of the two inductors would further improve the gain at higher frequency range but at the expense of extra measures for ensuring stability and an increase in noise figure. Furthermore, R_{bs} is chosen as 4 Ω.

B. Wideband Matching Network

For achieving the wideband performance, a dual-band matching network is typically utilized in mm- and sub-mm-wave circuit design [10]–[12]. Such an approach achieves a much wider BW, because it enables simultaneous match at two frequency points while keeping an acceptable mismatch in the middle of the desired frequency band. In this article, the dual-band matching network is designed based on the method described in [23]. As shown in Fig. 10(a), two L-type matching networks (TL1 and TL2, and TL5 and TL6) at both sides are joined by an impedance transformer consisting of series lines (TL3 and TL4) with a high and a low Z_c. The two L-type networks are used to compensate the reactance $\text{Im}\{Z_{\text{out,1}}\}$ of the output impedance of stage 1, and the reactance $\text{Im}\{Z_{\text{in,2}}\}$ of the input impedance of stage 2 at the two frequency points 175 and 205 GHz. The transformer between the resistances $\text{Re}\{Z_{\text{out,1}}\}$ and $\text{Re}\{Z_{\text{in,2}}\}$ is realized by two lines TL3 and TL4 instead of using a single TL with just a single Z_c as in [23]. Since the gain-cell presents a large output resistance, a relatively large resistive mismatch between two stages exists. As a result, Z_3 and Z_4 of TL3 and TL4 are selected with a resistance value close to that of the respective stage, thus achieving a better transformation performance.

For improving circuit optimization efficiency, TLs with different TM2 widths from 2 to 25 μm were EM simulated using Momentum in Keysight Advanced Design System (ADS). Based on the data, a two-port compact model was created, which was parameterized in Z_c and loss with width and length. Such a compact model enables rapid design and initial optimization prior to the time-consuming EM simulation. Fig. 10(b) and (c) shows the output reflection coefficient $\Gamma_{\text{out,1}}$ and the load reflection coefficient $\Gamma_{L,1}$ of the first stage gain-cell provided by the matching network. Due to the large magnitude of $\Gamma_{\text{out,1}}$ and the loss in the matching network, a perfect conjugate matching would require a more complicated network, which, in turn, would lead to an extra loss of the delivered power. Therefore, $|\Gamma_{L,1}| \approx 0.7$–$0.8$ is selected for three stages for higher power gain.

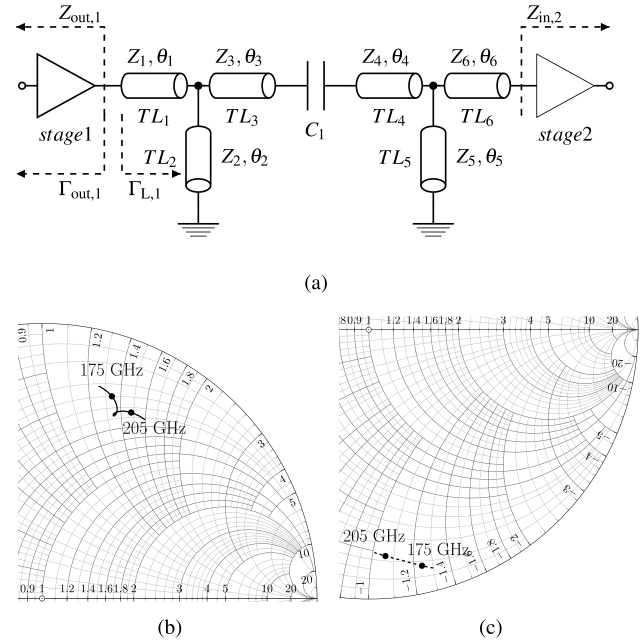

Fig. 10. (a) Proposed dual-band inter-stage matching network, and Smith chart representation of (b) $\Gamma_{L,1}$ and (c) $\Gamma_{\text{out,1}}$ with the frequency range of 160–220 GHz. Dots indicate the values at frequencies 175 and 205 GHz.

C. Circuit Implementation

Fig. 11 shows the circuit schematic of the amplifier. As mentioned in Section III-A, the optimum noise impedance and the conjugate match source impedance are not far apart from each other, and their real parts are close to the input impedance of the gain-cell. Hence, the input matching can be easily realized by a conventional T-type network to save chip area. Dual-band matching networks are implemented for interstage matching, transforming the input impedance of the subsequent stage to the desired load impedance of the previous stage. The dual-band output matching network is designed in a similar way due to the high output impedance of the gain-cell.

The bias networks are combined with the matching networks using a ZTL after each shunt ML (TL2, TL5, TL8, TL11, TL14, and TL17), which provide an ac ground with an impedance close to 0. The cross-sectional and 3-D views of the implemented ZTL are presented in Fig. 12(a) and (b), respectively. The ZTL is designed with a multiconductor from M1 to TM2. Counting from the bottommost layer M1, the even number of layers is connected together in the middle as the conductor line. The odd number of layers, however, is designed as grounded boundaries, which surround the

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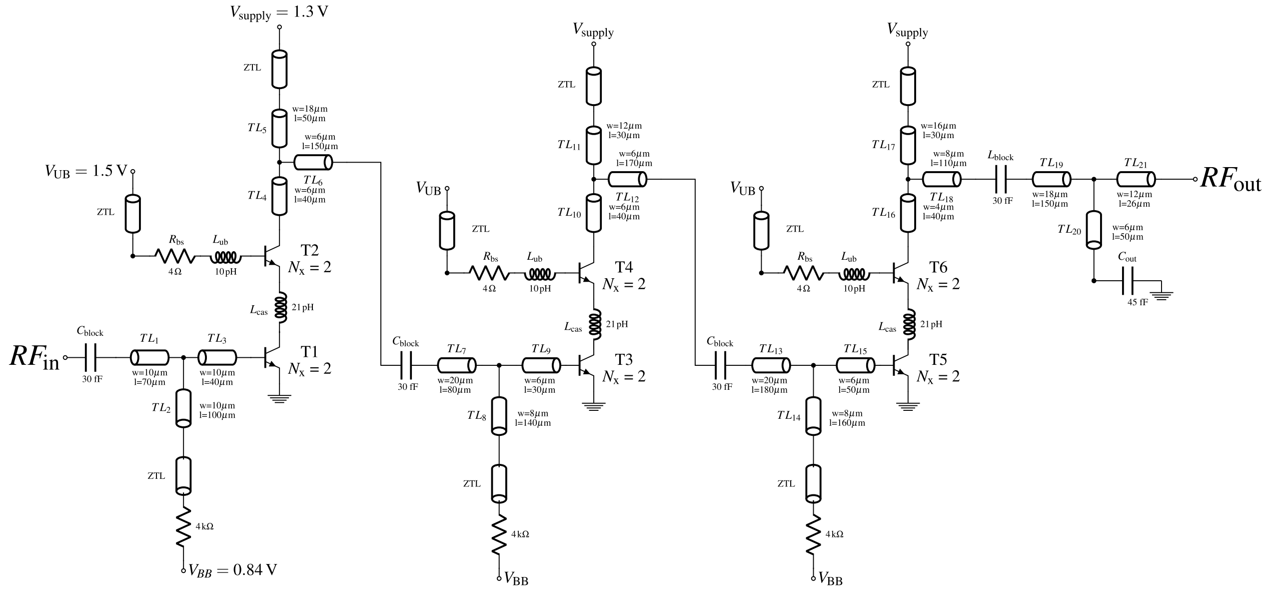

Fig. 11. Circuit schematic of the amplifier, including the selected element values and dimensions of each ML.

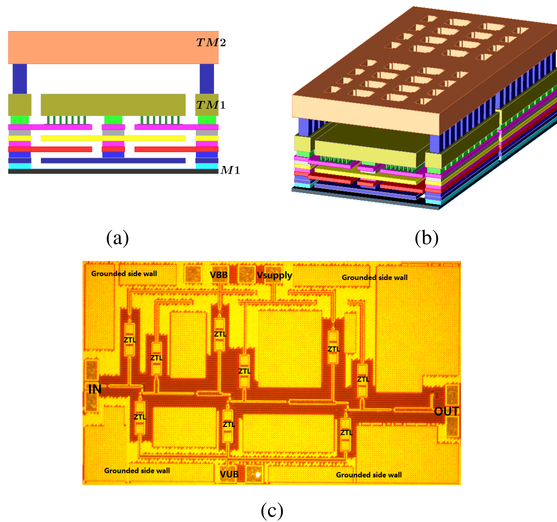

Fig. 12. (a) Cross-sectional and (b) 3-D views of ZTL. (c) Micrograph of the fabricated amplifier. The chip size is 0.7 mm × 1.5 mm, including pads.

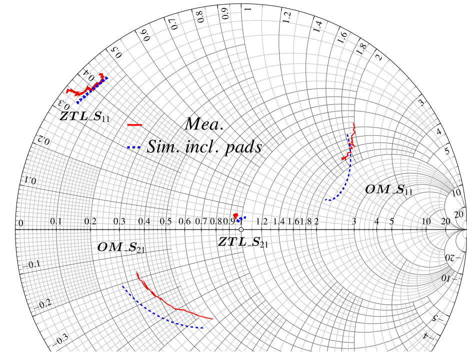

Fig. 13. Measured and simulated S_{11} and S_{21} of the ZTL and the output matching (OM) network from 160 to 210 GHz, where port 1 is connected with circuit/third gain-cell and port 2 is connected with dc/output pad, respectively. Pads are included in the simulation.

conductor line from all sides. Furthermore, the interleaved configuration enables the compensation between generated capacitance and parasitic inductance, while keeping the low impedance characteristics even when the frequency increases up to 220 GHz. Large numbers of small MIM capacitors are added along with the ZTL to further improve the low-impedance performance. Grounded sidewalls, which consist of grounded metals from M1 to TM2, are implemented around the MLs to prevent a crosstalk of adjacent devices and networks. 30-fF MIM series capacitors with a self-resonant frequency of about 275 GHz are utilized as a dc block both at the input and output ports, as well as between stages.

The micrograph of the fabricated circuit is shown in Fig. 12(c); the chip area is 0.7 mm × 1.5 mm, including all pads. An individual ZTL block and an output matching network block were also fabricated for the purpose of verifying their performance.

V. Results and Discussion

A. Measurement Setup

This amplifier was measured on-wafer. The G-band signal was generated from a VNA (Keysight PNA N5242A) and extended to the 140–220-GHz range using a VDI WR5.1 frequency extender both for the S-parameter measurement and the large-signal characterization. A VDI Erickson PM5 power meter was used for calibration first at an off-wafer reference plane (at the output port of the extenders, after TRL calibration) and then on-wafer after subtracting the loss of waveguides and probes. MMWAVE STUDIO was used to guide the calibration process and to automatically control the S-parameter, as well as the large-signal measurements.

B. Results

The S-parameters of the separately fabricated ZTL block and the output matching network block are shown in Fig. 13.

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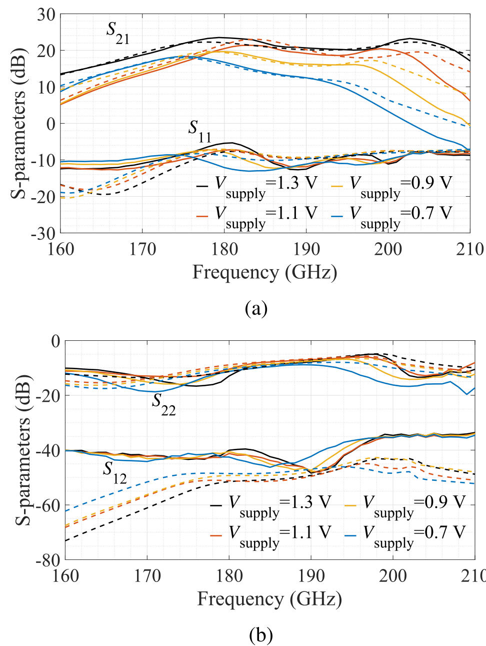


Fig. 14. Simulated (dashed lines) and measured (solid lines) S-parameters of this amplifier with V_{supply}/V = 1.3, 1.1, 0.9, 0.7. V_{UB} is 1.5 V for the former two and 1.3 V for the last two values of V_{supply}, and V_{BB} is 0.84 V for four bias cases.

For this comparison, the simulation includes also the pads. Overall, good agreement is shown between measured and simulated results both for the ZTL and the output matching network, which confirms the accuracy of EM simulation and the proper operation of two blocks in the circuit.

The measured and simulated S-parameters of the complete amplifier with four different bias conditions are shown in Fig. 14. At first, this amplifier is biased with $V_{supply} = 1.3$ V and $V_{UB} = 1.5$ V. Thanks to the dual-band matching networks, the circuit provides peak power gain points of 23.5 dB at both 179 and 203 GHz, consuming 3.2-mW static dc power. From 173 to 207 GHz, the gain is above 20.5 dB, yielding a 3-dB BW of 34 GHz. Keeping V_{UB} the same and reducing V_{supply} to 1.1 V, a peak gain of 21.3 dB at 183 GHz with a 3-dB BW of 26 GHz from 178 to 204 GHz is obtained with a reduced dc power of 2.7 mW. When V_{supply} is further reduced to 0.9 V and V_{UB} is tuned to 1.3 V, a peak gain of 19.6 dB is observed at 180 GHz along with 2.22-mW dc power and the overall gain above 15 dB from 172 to 198 GHz. Even with an ultralow V_{supply} of 0.7 V and V_{UB} of 1.3 V, this circuit still operates with a peak gain of 18.3 dB at 175 GHz, dissipating an extremely low dc power of 1.73 mW. The in-band input and output reflection coefficients S_{11} and S_{22} for these four bias cases are measured to be below -8 and -5 dB, respectively, and the S_{12} is measured to be below -35 dB, which indicates a good output-to-input isolation of this amplifier. Overall, good agreement between simulation and measurement is observed for S_{21}, S_{11}, and S_{22} under all bias conditions. The observed deviation for S_{12} may be attributed to substrate coupling.

The stability factor μ is calculated based on the measured S-parameters and is shown in Fig. 15. The minimum value for the four bias conditions is observed to be 1.22 at 203 GHz,

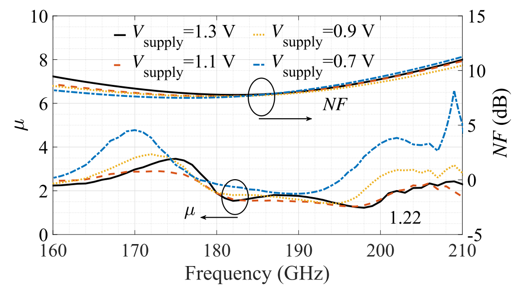
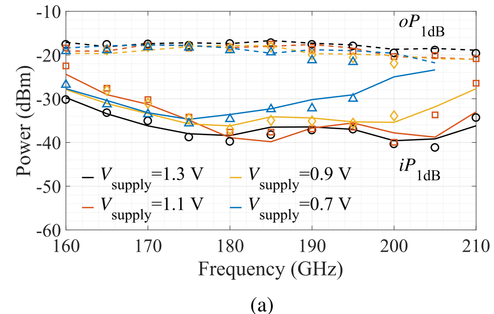


Fig. 15. Calculated μ-factor (left) based on the measured S-parameters, and the simulated NF (right) for four bias cases.



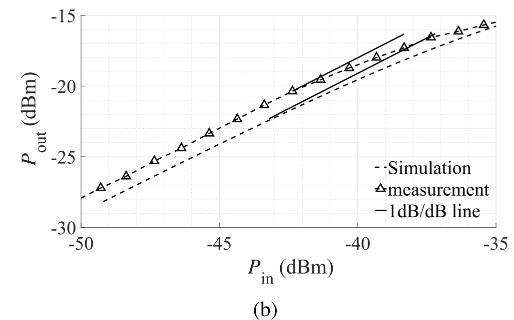


Fig. 16. (a) Simulated (lines) and measured (symbols) $oP_{1\,dB}$ and $iP_{1\,dB}$ from 160 to 210 GHz for four bias conditions. (b) Simulated and measured 1-dB output power compression curve at 185 GHz with $V_{supply} = 1.3$ V.

1.28 at 196 GHz, 1.43 at 194 GHz, and 1.8 at 189 GHz, respectively, which indicates the in-band stability of this amplifier. Since suitable equipment for accurate noise measurements was not available, NF of the circuit was simulated. The simulated NF is shown in Fig. 15 over the frequency range of interest, yielding a minimum of 7.7, 7.65, 7.6, and 7.5 dB at 181, 180, 178.5, and 177 GHz for V_{supply} between 1.3 and 0.7 V. Although V_{UB} is maintained, J_c (and I_c) still slightly decreases with decreasing V_{supply}, which results in a slight reduction of NF. Based on previous work [35] on high-frequency noise modeling for various HBT technologies, the authors believe that the simulation results represent the actual results reasonably well. In [35], HICUM was shown to accurately match both experimental data up to 50 GHz and the Boltzmann transport equation simulation based data up to 500 GHz. Furthermore, in [8], NF measurement data of two LNAs agree reasonably well with simulations at W-band.

The large-signal simulations and measurements for the four V_{supply} cases are shown in Fig. 16. With $V_{supply} = 1.3$ V, the measured peak $oP_{1\,dB}$ of this amplifier is -17.2 dBm

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TABLE II
COMPARISON WITH PUBLISHED AMPLIFIERS OPERATING AROUND 200 GHz

Reference	Technology	f_T/f_{max} (GHz)	Center frequency (GHz)	Gain (dB)	3-dB BW (GHz)	P_{dc} (mW)	oP_{1dB} (dBm)	*NF* (dB)	Gain/P_{dc} (1/mW)	FoM
MWCL2017 [10]	130 nm SiGe HBT	300/500	182.5	10	55	16.8	-10	10.5*	0.6	0.32
MWCL2014 [11]	130 nm SiGe HBT	300/500	190	16.9	44	18	-4.1	9.6*	2.72	5.7
MWCL2018 [12]	130 nm SiGe HBT	300/500	187.5	16	25	6.4	-14.3	11*	6.22	0.49
T-MTT2016 [16]	130 nm SiGe HBT	300/500	183	17.2	22	16.1	-9.6	7.6	3.3	1.65
T-MTT2012 [24]	130 nm SiGe HBT	300/500	210	15	20	150	-	13*	0.21	-
EuMIC2014 [25]	130 nm SiGe HBT	300/500	233	27	10	68	-	12.5*	7.4	-
EuMIC2017 [26]	130 nm SiGe HBT	300/500	190	24.7	16	37.2	-6.5	9.8*	7.9	3.3
This work (1.3 V)	**130 nm SiGe HBT**	**460/600**	**190**	**23.5**	**34**	**3.2**	**-17.2**	**7.7***	**70**	**9.2**
This work (1.1 V)	**130 nm SiGe HBT**	**460/600**	**191**	**21.3**	**26**	**2.7**	**-17.5**	**7.65***	**50**	**4.8**
This work (0.9 V)	**130 nm SiGe HBT**	**460/600**	**180**	**19.6**	**17**	**2.22**	**-18**	**7.6***	**41.8**	**2.35**
This work (0.7 V)	**130 nm SiGe HBT**	**460/600**	**175**	**18.3**	**15**	**1.73**	**-18.3**	**7.5***	**39.1**	**1.9**
MWCL2015 [27]	50 nm GaAs mHEMT	370/670	180	24.5	7	24	-	3.5	11.7	-
T-TST2014 [28]	50 nm GaAs mHEMT	370/670	184	22	17	41	-	6.7	4	-
JSSC2014 [29]	32 nm SOI CMOS	250/320	210	18	20	44.5	-	11	1.4	-
EL2016 [30]	32 nm SOI CMOS	250/320	184	25	20	33	-	9	9.6	-
T-TST2016 [31]	35 nm InP HEMT	400/1100	220	15	120	36	-	5.2	0.87	-
IMS2010 [32]	35 nm InP HEMT	400/1100	175	21	28	12	-	-	10.5	-
T-TST2014 [33]	250 nm InP DHBT	370/650	255	24	20	81.7	-	10.4	3.1	-
EuMIC2018 [34]	500 nm InP DHBT	350/400	120	10	110	96	-	8	0.1	-

*Simulated; - not presented

at 185 GHz, and the corresponding input 1-dB compression point $iP_{1\,\mathrm{dB}}$ is −38.2 dBm. When V_{supply} is decreased to 1.1 V, the peak $oP_{1\,\mathrm{dB}}$ and $iP_{1\,\mathrm{dB}}$ drop slightly to −17.5 and −37.6 dBm, respectively, at 185 GHz with in-band $oP_{1\,\mathrm{dB}}$ variation of 2.85 dB. Even with V_{supply} of 0.9 and 0.7 V, respectively, this amplifier still provides a peak $oP_{1\,\mathrm{dB}}$ of at least −18 and −18.3 dBm, while the corresponding $iP_{1\,\mathrm{dB}}$ is −37.2 and −35.6 dBm, respectively. The slightly reduced $oP_{1\,\mathrm{dB}}$ is mainly due to the slightly decreased J_c (and I_c). As shown in the figures, the large-signal measurement results are well approximated by simulations.

The performance of this amplifier is summarized in Table II and compared with recently reported amplifiers operating around 200 GHz. The 3.2-mW dc power consumption is the lowest value and just half of that of the latest presented state-of-the-art low-power amplifier [12], whereas the gain, *NF*, and BW are highly competitive. Besides, this amplifier achieves the highest gain per dc power consumption, and this ratio is higher by about ten times and six times, respectively, than the best reported SiGe amplifiers [12], [26] and state-of-the-art amplifiers using other technologies, respectively, such as 50-nm GaAs mHEMT [27], 35-nm InP HEMT [32], and 32-nm SOI CMOS [30]. Furthermore, taking the large-signal, 3-dB BW and the noise performance into consideration, a suitable FoM can be defined as

$$\mathrm{FoM} = \frac{\mathrm{gain}(1) \cdot \mathrm{BW(GHz)} \cdot oP_{1\,\mathrm{dB}}(\mathrm{mW})}{(\mathrm{F}(1) - 1) \cdot P_{\mathrm{dc}}(\mathrm{mW})} \tag{14}$$

where F is the noise factor. Although $oP_{1\,\mathrm{dB}}$ of this amplifier is lower, this amplifier still obtains the highest FoM and outperforms all the SiGe amplifiers listed in the table with an enhancement factor close to two against the amplifier reported in [11].

VI. CONCLUSION

A 173–207-GHz low-power amplifier has been implemented in an experimental 130-nm SiGe BiCMOS technology. Achieving the extremely observed low dc power dissipation has been enabled by a drastic decrease in the supply voltage and collector current, forcing all transistors to operate in saturation. Highly competitive performance in terms of gain, *NF*, and 3-dB BW has been realized simultaneously with the lowest reported dc power consumption and an up to ten times improvement of the gain to dc power ratio. First-pass success, good agreement of simulation with measurement, and the presented detailed circuit analyses have been enabled by accurate modeling and careful circuit optimization.

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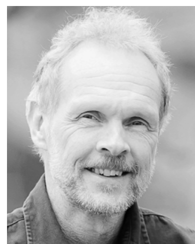

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