Opening of the Backside of ICs for Failure Analysis Using CMP

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Failure analysis methods need access to the backside of the device on chip level, in sub-10 nm technologies often with a back surface on STI level. Global thinning by grinding and polishing can remove the bulk silicon. By using a Si-slurry highly selective to SiO_2, the STI-structured chip backside can be revealed by polishing stop on STI level. In this work, the opening of bare dies and a flip-chip mounted, packaged IC down to STI for failure analysis will be demonstrated for the first time. Constraints of this new development will be identified and means to overcome will be discussed.

Keywords: *failure analysis, chemical-mechanical polishing, high selective slurry, grinding, IC thinning, bare die, flip-chip mounted device*

INTRODUCTION

For integrated circuit (IC) product development and 1st silicon debugging, the chip backside has to be opened for contactless fault isolation techniques (CFI). Near infra-red (NIR) allows the optical inspection of the circuit with a resolution limit of about 180 nm. By using NIR, analysis of 14 nm FinFET technology is possible, as the whole dimension of the FET covers an area of 6-8x of the node (gate dimension) [1]. Resolution has to be increased for actual and future nodes, which can be obtained by using shorter wavelength (e.g., 550 nm) and solid immersion lens. However, the transmission of the thin remaining silicon at the backside of the circuit is reduced drastically for visible light. An ultra-thin silicon back surface, i.e., thinning the back surface down to STI level, would allow access to the active device by various high resolution fault isolation techniques like Laser and E-Beam Inspection, Near-Field Scanning Optical Microscopy (NSOM) and Nano Probing (Fig. 1).

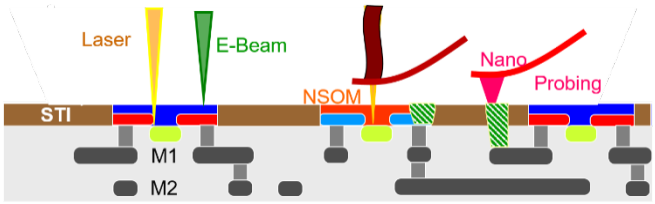


Fig. 1: high resolution fault isolation techniques

Various techniques for preparation of an ultra-thin back surface exist, e.g., by using focused ion beam (FIB) or laser assisted chemical etching (LACE). Beside the fact that these are local thinning techniques, endpoint control of the ablation process is necessary to ensure device functionality. FIB/LACE in combination with local chemical mechanical polishing (CMP) has been proposed to get access to the backside of the device [1], but only on a local scale. For global access of the whole IC we propose and demonstrate for the first time global backside CMP for failure analysis [2], see Fig. 2. Additional challenge is the requirement that the device has to remain faultless and can be contacted electrically after thinning.

Depending on the thickness of the packaged chip, bulk silicon of up to 700 – 800 µm has to be removed. This can be achieved in reasonable time by a combination of grinding and polishing steps whereat the last polishing step must

stop at the STI level. For that we have developed a concept employing an abrasive-free slurry for poly-Si CMP with a very high selectivity to SiO_2 of > 500 : 1 (applied for patent). While standard CMP slurries consist of a mixture of nano-abrasives and chemical additives, abrasive-free slurries have been developed with high Si removal rates. By adding cationic and nonionic polymer additives into basic solutions, predominantly Si is removed, while nearly no attack of SiO_2 can be observed, see, for example [3].

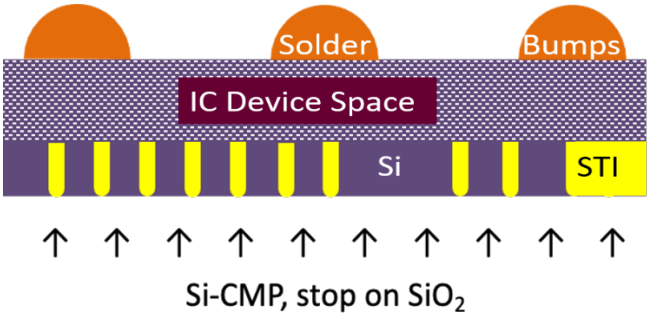


Fig. 2: backside CMP for access to backside of device

EXPERIMENTAL

Generally, the process sequence for opening the backside of ICs consists of the following steps:

- opening of package from backside
- mass removal of bulk silicon by grinding
- chemical-mechanical polishing of Si with slurry highly selective to oxide
- stop when STI oxide is exposed
- contacting circuit for electrical measurements and analysis of device

Grinding and polishing have been executed on a tabletop grinder/polisher MultiPrep™ system 8” together with an AD-5™ Automatic Fluid Dispenser from Allied High Tech, Inc., by using Diamond Lapping Film Disks with 35 µm, 15 µm and 6 µm grain size. After thinning by grinding in a three-step process down to 50 µm Si thickness, the remaining material has been removed by CMP. Using an IC1000™ perforated pad and SS12™ slurry, the Si substrate is polished down to ≈ 20 µm to remove sub-surface damage from grinding. The remaining Si was then removed with an experimental high-selective (HS) Si slurry from Resonac (formerly Showa Denko), whereat SS12 was added at the beginning of the final polishing step to remove native oxide. The whole preparation time summed up to typically 4 h.

Two types of samples have been chosen for prove of concept of failure analysis by inspection of a global ultra-thin back surface, first a bare 300 µm thick 10 x 10 mm test chip with IHP’s 130 nm BiCMOS process and second a commercial sub 50 nm flip-chip mounted processor with 500 µm thickness.

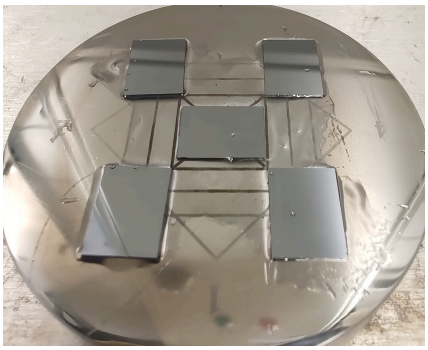


Fig. 3: arrangement of 5 chip stacks to increase stability and uniformity

For the first example, the frontside of the bare chip was wax-mounted against the sample holder so that the backside could be grinded/polished. In order to increase the distance to the sample holder, a second spacer chip had been mounted between test chip and sample holder. Due to the small size of the test chip a total of 5 stacked chips have been arranged on the holder in order to reduce tilting and to increase stability and removal uniformity, see Fig. 3. Nevertheless, a slight tilting remained due to non-uniform wax distribution which we aimed to compensate with an

over polish by the high selective Si slurry. Preliminary tests have confirmed a selectivity between the p-type mono-crystalline Si and TEOS oxide of > 500 : 1.

The second type of samples to which we applied the developed backside thinning method was a commercially available processor flip-chip bonded to a PCB carrier board. First, the capacitors soldered to the board had to be removed. Then, using mounting wax, the PCB was mounted on the parallel polishing fixture, see Fig. 4. Mechanical measurements of the die thickness had revealed that the device is not ideally flat but shows a convex curvature of the chip's backside silicon of 25 µm.

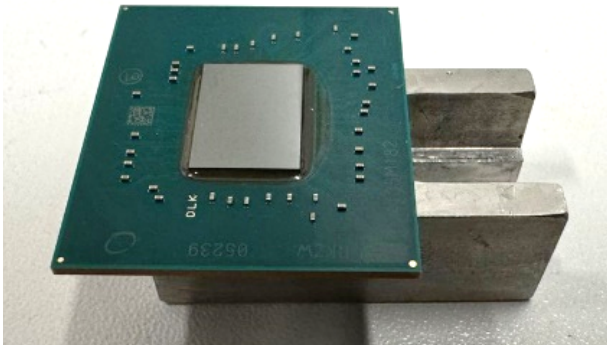


Fig. 4: Flip-Chip mounted sub 50 nm device on customized sample holder

RESULTS

The five stacked chips of Fig. 3 with special attention on the center chip were first grinded in several steps down to about 50 µm and then polished with the more or less unselective, fumed silica based SS12™ slurry down to about 18 µm. Material removal rate achieved with SS12™ was 0.87 µm/min. Subsequently, using the HS poly-Si slurry, the remaining Si was thinned to STI in several steps with a mean removal rate of 0.34 µm/min. The polishing had to be interrupted several times in order to condition the hard-foam IC1000™ polishing pad. The polishing sequence had been stopped when the structured STI level was exposed, see Fig. 5. All five samples have partially revealed their structured STI level. Due to the slightly tilted samples, the edges of the chips were cleared first.

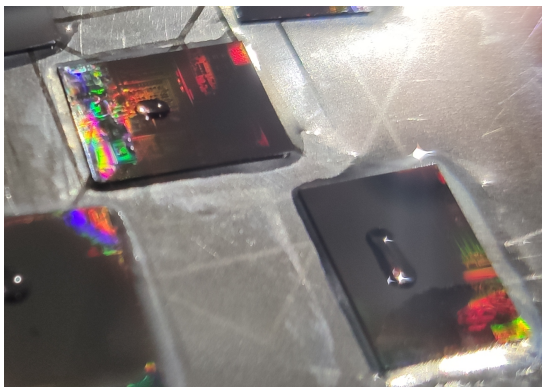
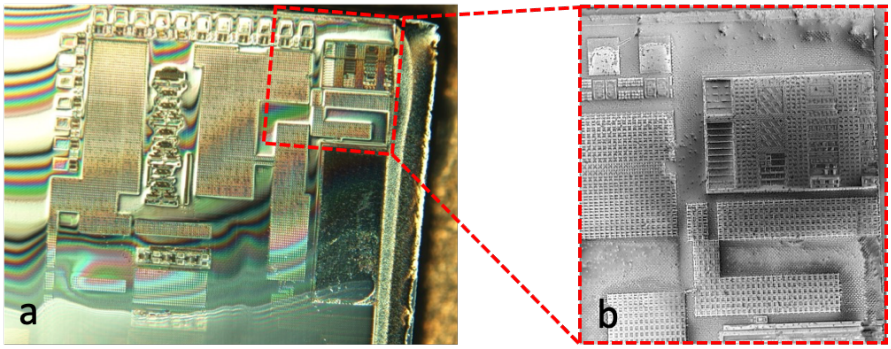


Fig. 5: polished sample stacks with partially removed bulk silicon

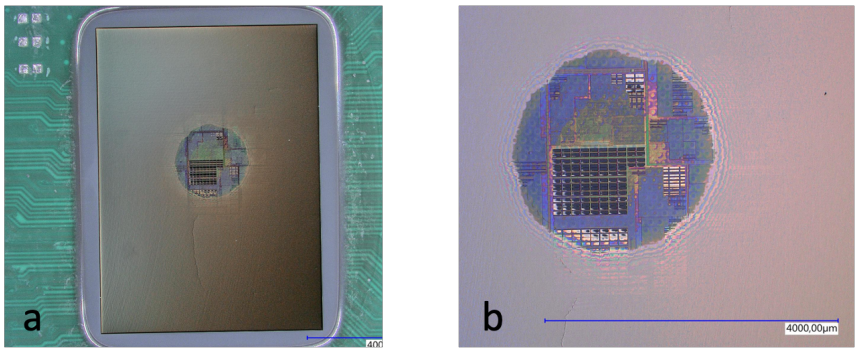
An additional over polish of 10 min removed another ≈ 3.5 µm of Si and it can be seen in Figs. 6 a and b, that the corner of the chip is still maintaining its 400 nm thick STI structures and the 15 µm thick FEOL and BEOL layers. The bulk silicon has been removed and an SEM photograph shows parts of the device from its backside and indicates, that applying electrical contact with nano probes could be possible.

Interestingly, an overhanging part of the polished chip originated due to misalignment of the stack showed elastic behavior and did not break in spite of only ≈ 15 µm thickness. This is an indication that the thinning method developed is gentle to the remaining device and that there is a good chance to successfully perform backside fault isolation techniques at an electrically powered circuit.



Figs. 6 a and b: optical (a) and scanning electron micrograph (b) of the backside of the device

The flip-chip mounted processor IC in sub-50 nm node technology features an initial backside silicon thickness of 500 µm. It was thinned with a similar sequence to the bare chip with the exception of an extended grinding step with 35 µm diamond lapping film disk. Due to the convex surface of the flip-chip, the center of the die was cleared first and revealed a ca. 2.0 mm opening of the STI region, see Figs. 7 a and b. However, an extended polishing with the HS poly-Si slurry did not further increase the STI exposed area. The reason could be the hardness and stiffness of the employed IC1000™ polishing pad, which does not adapt to the slightly curved surface of the flip-chip device.



Figs. 7 a and b: Flip-Chip mounted processor with partially opened backside (a) and detail (b)

CONCLUSIONS

Using high-selective slurry for poly-Si CMP allows the opening of the backside of separated or packaged chips with stopping on STI level. This allows backside contactless fault isolation, i.e., access for optical inspection with shorter wavelengths or even e-beam probing for failure analysis of 1st silicon. In this work we have demonstrated for 2 examples, a bare die and a flip-chip device, the capabilities of this newly developed method. While small deviations like non-parallel polishing or a strained chip backside can be compensated by the extremely high selectivity of the slurry, larger deviations like tilted or bended surfaces need more process development work like, e.g., more flexible sample holders or investigation on the influence of the properties of the polishing pad. Additionally, it must be evaluated how the global extreme thinning of the bulk silicon influences the electrical performance of the device.

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