The Effect of Surface Optimization on Post-grinding Yield of 200 mm Wafer Level Packaging Applications

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***Abstract*—In this paper, a yield increase on post-grinding of 200 mm wafer level packaging applications is presented. 200 mm wafer level plasma enhanced oxide-oxide direct bonding and wafer grinding are used in the packaging of the wafers. Since the surface conditions of the wafers that are used in the packaging is the most critical point of the wafer bonding and grinding processes, it is focussed to optimizing wafer surfaces to increase the yield. After the optimizations on the surface conditions of the BiCMOS wafer used in the packaging, the 200 mm plasma enhanced wafer to wafer direct bonding yield increases from 0% to 99% and at the same time the post-grinding yield of these wafers increases from 0% to over 90%.**

***Index Terms*—Wafer bonding; Microfluidics; Lab-on-Chip (LoC); packaging; grinding; yield**

I. Introduction

Wafer level packaging is a technique that increases throughput and yield on packaging systems and a new generation of packaging systems has been promised by wafer level processing techniques [1]. Additionally many different applications requires wafer level packaging where complex systems are on the wafer like Micro-Electro Mechanical Systems (MEMS) and Lab-on-Chip (LoC) applications [2]–[5].

Finalization of the 200 mm wafer level packaging requires wafer to wafer bonding and wafer grinding/thinning techniques. Even though the there are strict requirements for the 200 mm wafer direct bonding [6], using well defined and reported 200 mm direct wafer bonding and grinding techniques favour to use them to utilize high-throughput in the packaging processes and low cost of the final chips. Therefore, it enables to package all the chips on the 200 mm wafer at once with high throughput.

The wafer level packaging of 200 mm wafers start with bonding of the package wafer on to a functional wafer [7]. The surface of the functional and package wafer need to be processed according to the requirements of the wafer direct bonding. To have high quality and high bonding strength, the surfaces need to be free of roughness and high annealing temperatures on the annealing at the bonding process. It is also possible to get high bonding strength on lower temperatures by plasma activation on the surface [8]. Later, the package wafer needs to be thinned down to required thickness by wafer grinding techniques. In this perspective, having high quality of wafer bonding is the most important determiner for getting high yield on the packaging of the chips.

In this work, the effect of the BiCMOS wafer surface optimization processes on the process yields is shown by non-destructive Scanning Acoustic Microscopy (SAM) and destructive grinding method. These optimization processes are directly affecting the wafer to wafer direct bonding quality which can be seen in the bonding and post-grinding yields. The final yield results of different surface oxide roughness optimization are compared.

II. Microfluidic Packaging

In our Si based microfluidic technology and packaging development, the aim is to integrate microfluidics with in-house BiCMOS technology with CMOS-compatible wafer processing techniques [9]. In this technology development, 200 mm wafer bonding and grinding techniques are used. In Figure 1, the process flow of the technology development can be seen.

On this process flow, firstly the BiCMOS wafer is fabricated and microfluidic inlet and outlet are opened by Localized Backside Etching (LBE) from the backside of the wafer. Secondly, on a bare Si wafer, the microfluidic channel structures are etched. Later, these two wafers are bonded together by plasma activated oxide-oxide fusion bonding from their front sides. The height of the channels are arranged by backside grinding of the microfluidic channel wafer. At last, a glass wafer is bonded on top of the channels in order to encapsulate the channels and package the chips. After this point, the wafer stack is ready for the chip dicing.

The main bottleneck of the method is bonding BiCMOS and microfluidic wafers together [10]. If the bonding strength

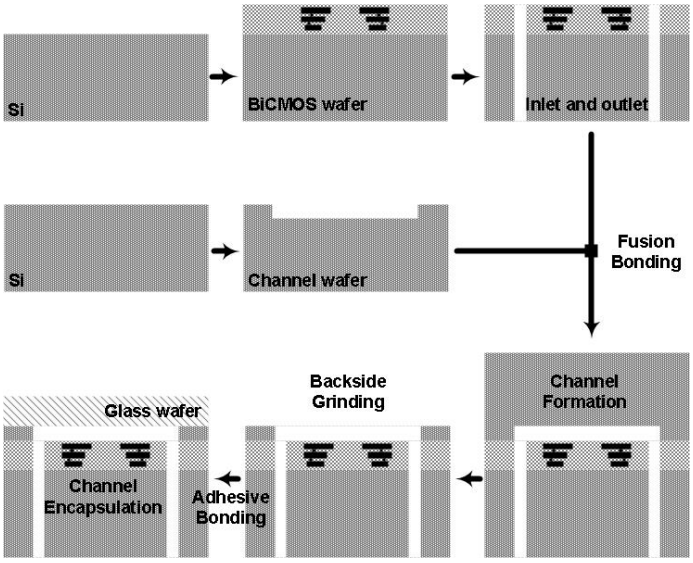

Fig. 1: Packaged microfluidic lab-on chips by three-wafer-stack approach with the optimized wafer surfaces.

is low, then the wafer stack cannot withstand the forces under wafer grinding processes. Therefore, increasing the bonding strength is crucial to increasing the yield in this packaging method. In order to increase the bonding strength, surface roughness optimization applied on the BiCMOS wafer.

In order to understand the effects and the results, some characterization techniques are applied between the steps of the packaging flow. The first characterization step is measuring the micro surface roughness with non-destructive Atomic Force Microscopy (AFM). With this method, it is possible to get high resolution surface topography and the micro roughness over 20 μm x 20 μm area. After the bonding, the wafer stack are investigated under SAM, and the bonding interface is investigated. Finally, the wafer stacks are grinded and destructively tested for the yield.

III. Experimental Results

Before the fusion bonding, the front surface of the BiCMOS wafer which will be on the bonding interface is optimized. This wafer is terminated with a thick oxide layer which is deposited on top of the last metallization layer. Therefore, the effect of the last metallization layer and the thick oxide deposition on the surface roughness tried to be decreased. Firstly, optimum oxide types and the oxide thicknesses are investigated to obtain the best surface roughness conditions. Secondly, the effect of the backside processes on the wafer while the through holes are being opened is decreased by chanhing the order of the process steps. These simple optimizations are already decreased surface micro-roughness (Rq) from 1.79 nm to below 1 nm over 20 μm x 20 μm area [10].

Additionally, before the 200 mm wafer level plasma activated oxide to oxide bonding, a short Chemical Mechanical Polishing (CMP) touch-up step is applied on the front surface to further reduce the surface roughness. A special method of

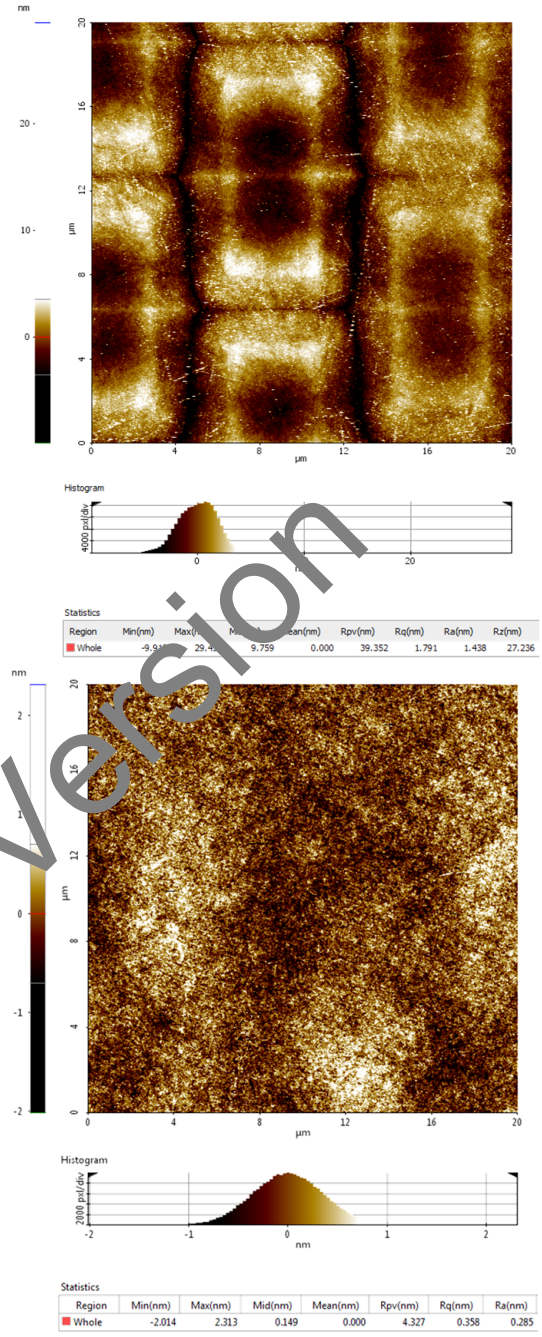

Fig. 2: AFM image of the surface over metal fillers before *(top)* and after *(bottom)* the surface optimization. The surface roughness (Rq) over 20 μm x 20 μm area decreased from 1.79 nm to 0.35 nm.

CMP touch-up is developed for that step due to the open metal structures and through holes on the BiCMOS wafer. The damage done by the CMP on the short touch-up step is reduced while having less rough surface for the fusion bonding. After this step, the oxide micro-roughness is decreased around 0.35 nm over 20 μm x 20 μm area. In Figure 2, AFM image of the surface roughness change can be observed.

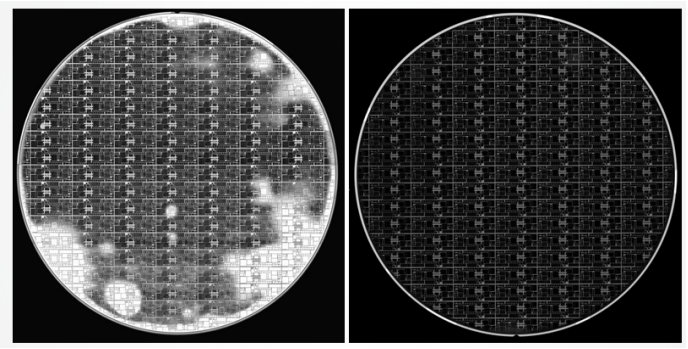

Fig. 3: Post-bonding SAM image of the wafer stack surfaces before *(left)* and after *(right)* the surface optimization. The post-bonding yield increased over 99% after the optimizations.

Fig. 4: Post-grinding photo of the wafer stack surfaces before *(left)* and after *(right)* the surface optimization. The post-grinding yield increased over 90% after the optimizations.

A. Wafer Bonding Yield

The standard flat terminated BiCMOS wafers in IHP technology is yielding 0% wafer bonding results since the micro-roughness is above the requirements of 1 nm over 20 μm x 20 μm area. After the first level of surface roughness optimizations as stated above, the surface micro-roughness is dropped from 1.79 nm to barely below 1 nm with only optimizing the surface oxide type and the deposition processes. Bonding of these wafers are resulted 60% yield of overall 200 mm wafer surface area.

The newly developed short CMP touch-up process decreases the surface micro-roughness around 0.3 nm. This applied last planarization step increases the bonding yield of the wafers up to 99% of the total 200 mm wafer area. The improvement over the 200 mm direct wafer bonding can be seen in the SAM images in Figure 3. The result on the left in the figure shows the bonding yield of the wafer stacks without last CMP touch-up step. In the image, the black areas are where there is successful bonding on the interface since there is no reflected acoustic waves from the interface. The result on the right side on the figure, it can be seen that the bonding yield increases

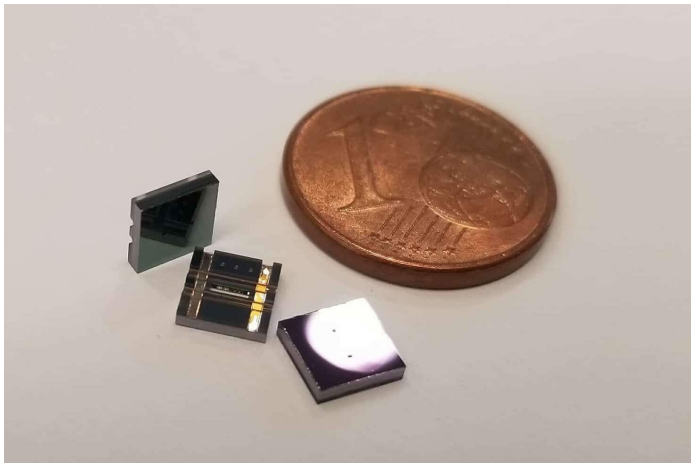

Fig. 5: Packaged microfluidic lab-on chips by three-wafer-stack approach with the optimized wafer surfaces.

up to 99% after applying the last CMP touch-up process step.

B. Grinding Yield

Since there is no bonding successful with the standard flat terminated BiCMOS wafers, there are no results from wafer grinding. The first wafers grinded on this packaging process flow are the wafers with optimized oxide thickness and type wafers which have a bonding yield around 60%. After the grinding of these wafers, the yield drops down to 10%. This drop can be explained by the damage caused by the wafer parts which are not initially bonded on the BiCMOS wafer. Since they are not bonded, they are flying around during the grinding process and hitting back on the surface with high velocity, breaking the neighbouring area. Even though maximum yield can be up to 60% coming from the bonding yield, the yield after grinding drops drastically because of this reason.

On the wafers with final touch-up optimization, it is expected to have more post-grinding yield due to the high bonding yield. As expected, these wafers have over 90% post-grinding yield as expected. Since the bonding yield on these wafers are up to 99%, the flying particle damage effect which can be seen on the wafers with low bonding yield is not seen on these wafers.

In Figure 4, the post-grinding photos of the 200 mm wafers can be seen. On the figures, the front side of the fully processed BiCMOS wafer which is the bonding interface on BiCMOS wafer side is visible in brownish earth colors. The grey parts are the backside of the channel package wafer which consist of only Si. On the left side of the figure, the front side of the BiCMOS is mostly visible due to low post-grinding yield. On these wafers, there si only oxide type and thickness optimizations are done. It is also clear that the post-grinding yield is around 10% which is not enough for further processing. However on the right side of the figure, the high post-grinding yield is seen by grey color covering all over the BiCMOS wafer front surface. The post-grinding yield on these wafers are more than 90%. Therefore, it is

possible to finalize the packaging with these wafers.

After the grinding, a glass wafer is bonded on top to encapsulate the channels and total chip to have the final packaging. Later, the wafer is diced twice: the first to expose the electrical pads from the glass wafer capping; the second to separate the chips from the wafer. In Figure 5 the packaged microfluidic chips and a 1 Euro cent for scaling can be seen.

IV. Conclusion

A well done optimization on the BiCMOS wafer surface and surface termination conditions directly affect the bonding yield and afterwards the post-grinding yield. Even standard flat terminated BiCMOS wafers are not being capable of to be used in packaging applications where wafer to wafer direct bonding is used. A detailed optimization processes need to be applied on the surface in order to get high yield packaging. It is shown that with the detailed optimization processes, first the bonding yield increased from 0% to 99%, and then with the same wafers post-grinding yield increased from 0% to over 90%.

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References

[1] K. Zoschke, M. Wilke, M. Wegner, K. Kaletta, C.-A. Manier, H. Oppermann, M. Wietstruck, B. Tillack, M. Kaynak, and K.-D. Lang, "Capping technologies for wafer level mems packaging based on permanent and temporary wafer bonding," in *Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th*. IEEE, 2014, pp. 1204–1211.

[2] C.-P. Chang, D. J. Nagel, and M. E. Zaghloul, "Go with the (micro) flow," *IEEE Potentials*, vol. 27, no. 6, pp. 17–25, 2008.

[3] S. Babikian, L. Wu, G. Li, and M. Bachman, "Microfluidic thermal component for integrated microfluidic systems," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*. IEEE, 2012, pp. 1582–1587.

[4] E. Ghafar-Zadeh, M. Sawan, and D. Therriault, "A microfluidic packaging technique for lab-on-chip applications," *IEEE Transactions on Advanced Packaging*, vol. 32, no. 2, pp. 410–416, 2009.

[5] M. Kaynak, M. Wietstruck, C. B. Kaynak, S. Marschmeyer, P. Kulse, K. Schulz, H. Silz, A. Kruger, R. Barth, K. Schmalz *et al.*, "Bicmos integrated microfluidic platform for bio-mems applications," in *Microwave Symposium (IMS), 2014 IEEE MTT-S International*. IEEE, 2014, pp. 1–3.

[6] S. H. Christiansen, R. Singh, and U. Gosele, "Wafer direct bonding: From advanced substrate engineering to future applications in micro/nanoelectronics," *Proceedings of the IEEE*, vol. 94, no. 12, pp. 2060–2106, 2006.

[7] S. Skordas, D. Tulipe, K. Winstel, T. Vo, D. Priyadarshini, A. Upham, D. Song, A. Hubbard, R. Johnson, K. Cauffman *et al.*, "Wafer-scale oxide fusion bonding and wafer thinning development for 3d systems integration: Oxide fusion wafer bonding and wafer thinning development for tsv-last integration," in *Low Temperature Bonding for 3D Integration (LTB-3D), 2012 3rd IEEE International Workshop on*. IEEE, 2012, pp. 203–208.

[8] M. Howlader, S. Suehara, H. Takagi, T. Kim, R. Maeda, and T. Suga, "Room-temperature microfluidics packaging using sequential plasma activation process," *IEEE transactions on advanced packaging*, vol. 29, no. 3, pp. 448–456, 2006.

[9] M. Inac, M. Wietstruck, A. Göritz, B. Cetindogan, C. Baristiran-Kaynak, S. Marschmeyer, M. Fraschke, T. Voss, A. Mai, C. Palego *et al.*, "Bicmos integrated microfluidic packaging by wafer bonding for lab-on-chip applications," in *Electronic Components and Technology Conference (ECTC), 2017 IEEE 67th*. IEEE, 2017, pp. 786–791.

[10] M. Inac, M. Wietstruck, A. Göritz, B. Cetindogan, C. Baristiran-Kaynak, M. Lisker, A. Krüger, A. Trusch, U. Saarow, P. Heinrich *et al.*, "Oxide surface roughness optimization of bicmos beol wafers for 200 mm wafer level microfluidic packaging based on fusion bonding," in *Electronics Packaging Technology Conference (EPTC), 2017 IEEE 19th*. IEEE, 2017, pp. 1–4.