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Compact and Transfer Printable 64 Gb/s Differential Transimpedance Amplifier in 130-nm BiCMOS

Mesut Inac[#1], Giannino Dziallas[#], Adel Fatemi[#], Friedel Gerfers[*] and Andrea Malignaggi[#2]
[#]IHP-Leibniz-Institut für innovative Mikroelektronik, Germany
[*]Technische Universität Berlin, Germany
[1]inac@ihp-microelectronics.com, [2]malignaggi@ihp-microelectronics.com

***Abstract*— This paper presents the design and performance comparison a transimpedance amplifier (TIA) first implemented in the standard IHP SG13G2 technology while the second one utilizes a new back-end technology for a transfer printing process. In order to make the TIA design compatible with the transfer printing technology, the topmost metal layer (TM2) is eliminated. As a result, custom inductors are developed using adopting the four lower level metal layers. Small signal measurement of both designs reveal a transimpedance gains above 66 and 68 dBΩ till 40 GHz of signal bandwidth. thus, the use of the transfer printing technology cause only 2 dBΩ loss. The measured S_{11} remains below -10 dB up to 60 and 70 GHz, respectively. The measured eye diagrams at 64 Gbps prove the performance of the transfer printing approach being able to compete with state-of-the-art transimpedance amplifiers' performance.**

***Keywords*— BiCMOS, low noise, receiver, SiGe:C HBT, TIA, transfer print.**

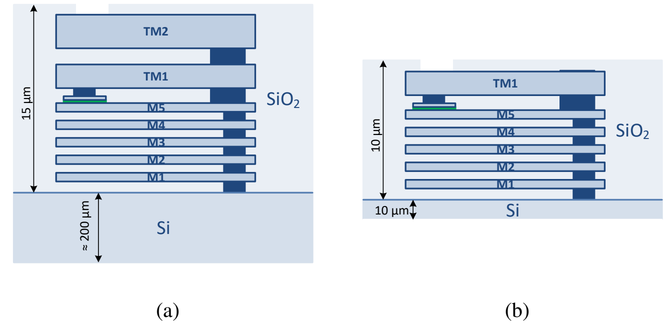
I. Introduction

Data traffic transferred between servers and users has been continuously growing in recent years with the increasing digitalization all over the world. With this increase, the hardware producers are boosting the transceivers' capacity used in communication. In the upcoming years, the employment of transceivers having speeds over 1 Tb/s has been predicted [1].

Co-integration of electro-optical components, integrated into a single substrate, targets high data rate transmission. Due to the complex integration techniques, these systems occupy large areas and their production costs are high. The transfer printing technique is a key solution enabling the integration of high-speed electrical and optical components with reduced cost on a small die [2]. It uses an elastomer stamp to transfer microscale dies from their native substrate onto non-native ones. The electrical and optical dies transferred onto another substrate are connected through a metalization. From a performance perspective, such a process allows to avoid the use of bandwidth limiting mounting techniques like bondwires [3].

Transimpedance Amplifiers (TIAs) are the first electrical block on the receiver side of any opto-electronic communication systems. They are located after photodiodes, where the optical data carried by the photonic components are translated into an electrical signal. High transimpedance gain and low introduced noise are the two main key parameters a TIA designer should take into account [4]. Usually, TIAs are composed of multiple stages. After the transimpedance stage, a variable or fixed gain amplifier is used to amplify the signal and to bring it to the amplitude levels required by the following blocks, i.e. clock and data recovery circuitry or analog to digital converters. A buffer stage usually adapts the impedance at the interface between TIA and such blocks.

In this paper, design and performance comparison between a standard and a transfer printable differential broadband TIAs, both fabricated using the IHP 130 nm SiGe BiCMOS technology, are presented. Designed TIAs have 66 and 68 dBΩ transimpedance gain over 40 GHz of bandwidth.



(a) (b)

Fig. 1. Cross-section representation of the technology (not on scale): (a) standard stack; (b) transfer printable stack with thinned Si substrate and removed uppermost metal layer (TM2).

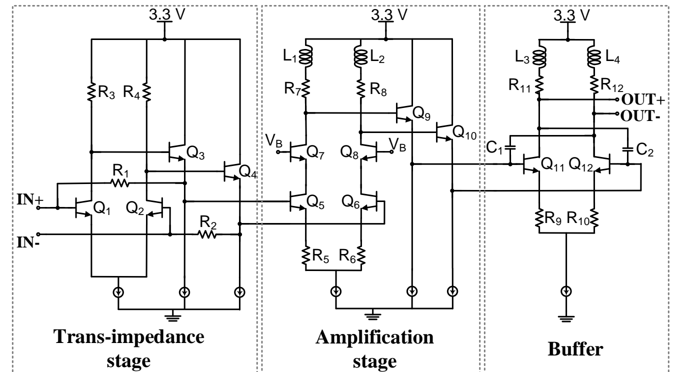


Fig. 2. Circuit schematics. Both TIAs include three stages: a transimpedance stage, a main amplification stage and a 50 Ω buffer stage.

Table 1. The sizes of the components used

Component	Size	Component	Size	Component	Size
Q1-Q2	8x1	Q11-Q12	10x1	R9-R10	8.6 Ω
Q3-Q4	4x1	R1-R2	568 Ω	R11-R12	45 Ω
Q5-Q6	2x1	R3-R4	200 Ω	L1-L2	300 pH
Q7-Q8	2x1	R5-R6	10 Ω	L3-L4	100 pH
Q9-Q10	4x1	R7-R8	120 Ω	C1-C2	19.2 fF

II. Circuit Design

In order to be transfer printed, a chip should satisfy some precise requirements in terms of size [5]. In particular, the process to be used accepts chips having a thickness of 20 μm and a size of 200 μm x 300 μm. In the IHP SG13G2 technology, the standard chip thickness is 200 μm, of which 15 μm belong to the back-end of line (BEOL). To be able to meet the thickness requirements, the substrate of the chips should be thinned and the uppermost metalization (TM2) should be removed. Therefore, the design of the transfer printable TIA has been carried to avoid the usage of TM2. Cross-sections of standard and transfer printable technologies can be seen in Fig. 1.

In order to check the performance difference between transfer printable circuits, two different TIAs have been designed. Both circuits utilize the same topology, the same active devices and the same passive component values, but while one of them is designed using a transfer printable metal stack (TIA1), the other is designed using the standard metal stack (TIA2). The schematics of both circuits are reported in Fig. 2. They consist of three differential stages. The first stage is a transimpedance stage in a resistive shunt feedback configuration, while the second is a fixed gain cascode amplifier followed by an emitter follower. In this stage, two peaking inductors are used on the load of the cascode. The last stage is a 50 Ω buffer, where cross-coupling capacitors are used to extend the bandwidth as well as two peaking inductors. The sizes of the used components can be seen in Table 1.

Both active cores have been kept as compact as possible in order to be suitable for the transfer printing process. Inductors and transmission lines generally occupy large chip areas. In order to reduce their area occupation, input and output transmission lines have been folded, while the peaking inductors have been designed using multiple metal layers for implementing different inductor turns in a stacked fashion. In order to reduce the capacitance between consecutive inductor turns, which has a negative effect on the inductor's self resonance frequency, turns on consecutive metal layers are misaligned and located one line width away from each other. Exploiting this technique, a 300 pH inductor can be fitted onto a silicon area of only 20 μm x 20 μm. On the TIA1, the inductor turns start from top metal 1 (TM1) and end at the third metal layer (M3), while on the TIA2 the inductor turns start from TM2 and end at the fourth metal layer (M4). The 3-D representation and the simulated characteristics of the inductors can be seen in Fig. 3, where can be noticed how the different use of the metal layers does not affect the inductance within the operating frequency band, while it has an impact on the quality factor, which is anyway negligible considering the position of those inductors within the circuits (in series with the load resistors). Input and output lines of the TIA1 are designed on TM1 while on the TIA2, TM2 is utilized. Their widths are designed to provide together with the pad capacitances 50 Ω characteristic line impedance.

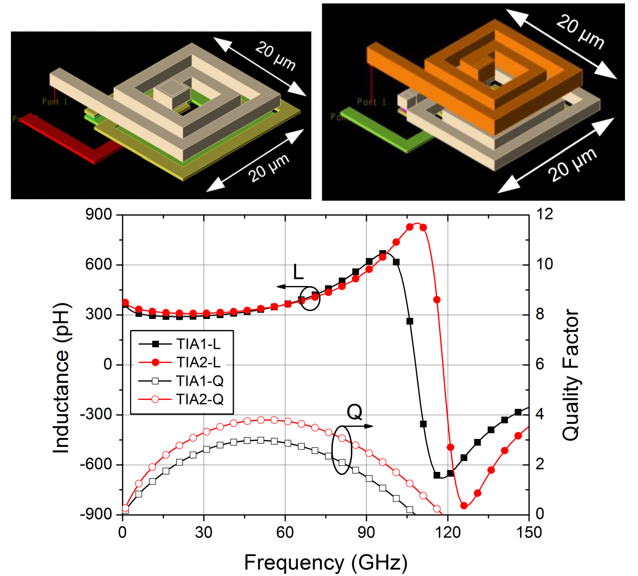


Fig. 3. 3-D representation of the 4-layered compact 300 pH inductor with a size of 20 μm x 20 μm on TIA1 (left) and TIA2 (right). Inductances and quality factors of the designed inductors (bottom).

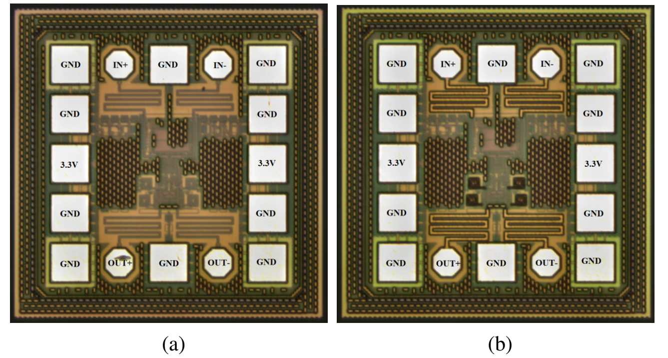


Fig. 4. Micrographs of the fabricated chips: (a) TIA on the modified stack (TIA1); (b) TIA on the standard technology (TIA2).

Moreover, to be able to meet the size requirements for transfer printing, all the blocks in the TIAs are fitted in 125 μm x 200 μm, except pads and the connection lines. Including the connection lines, both circuits occupy 270 μm x 300 μm silicon area.

III. Measurements and Results

Both chips are measured on wafer. The fabricated chips' micrographs can be seen in Fig. 4. The fabricated TIAs are characterized by S-parameters, noise and time domain measurements.

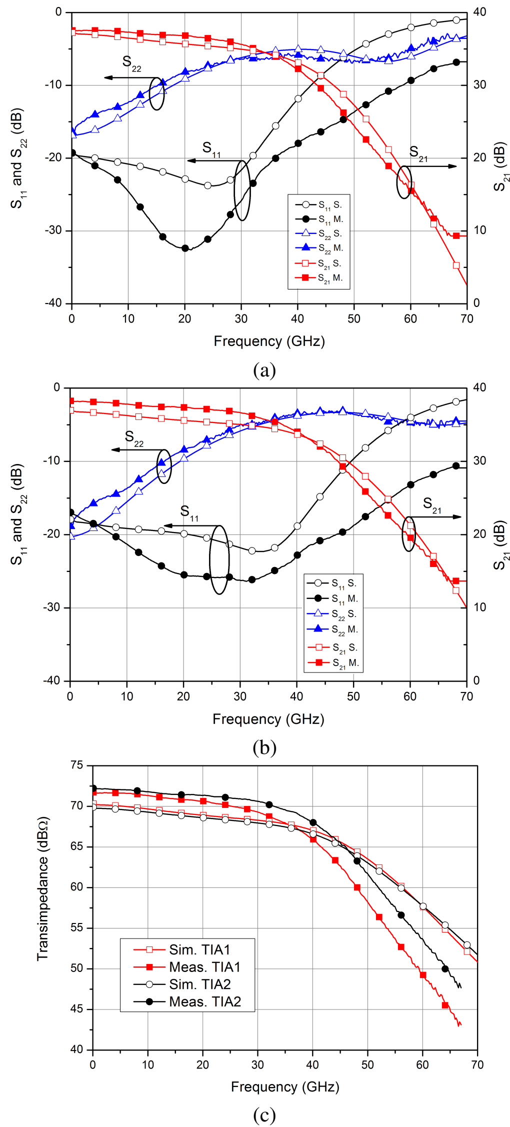


Fig. 5. Simulated and measured S-parameters and transimpedance gain of TIA1 and TIA2: (a) TIA1 S-parameters; (b) TIA2 S-parameters; (c) Extracted transimpedance gain of TIA1 (red) and TIA2 (black).

A. *Small Signal Measurements*

The small signal behavior of both circuits have been measured by a 4-port differential setup using a R&S ZVA67 vector network analyzer, keeping an input power of -38 dBm. The results of S-parameter measurements are shown in Fig. 5a and 5b. The input return loss S_{11} is below -10 dB until 60 GHz and 70 GHz on TIA1 and TIA2 respectively. The output return loss S_{22} is below -10 dB until 20 GHz on both TIA1 and TIA2. The small signal voltage gain S_{21} is around 37 dB for both designs. The transimpedance gains are extracted from S-parameter measurement results and illustrated in Fig. 5c. TIA1 and TIA2 present a gain of above 66 dBΩ and 68 dBΩ over 40 GHz of 3-dB bandwidth. These results prove how the different lines and inductors implementations did not alter significantly neither input and output reflections nor signal gain.

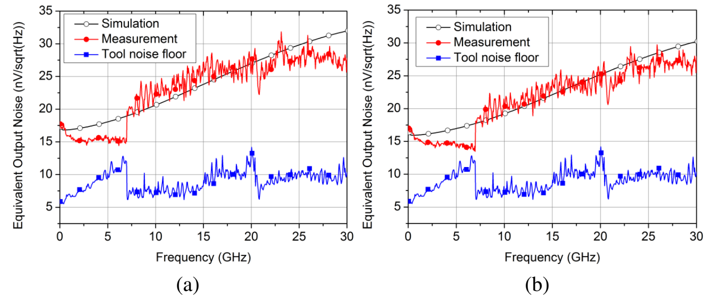


Fig. 6. Simulated and measured output noise density of TIA1 (a) and TIA2 (b). Degraded eye opening at the input due to the measurement setup results degraded output eye diagram.

B. *Noise Measurements*

The noise characterization of both circuits has been conducted using the open input method, monitoring the output noise voltage while leaving the input open. For obtaining a correct measurement, the noise floor of the measurement tool needs to be determined and extracted from the measured output noise. Then, in order to find the output noise density, the result of such subtraction needs to be divided by the measurement resolution bandwidth. The calculated output noise voltage density minimum levels are 15 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and 13 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ on TIA1 and TIA2 respectively. These values are obtained from a R&S FSV30 signal and spectrum analyzer. The noise measurement results can be seen in Fig. 6.

C. *Time Domain Measurements*

The eye diagrams of the circuits are plotted using a Keysight DCA-X 86100D wideband oscilloscope with 100 GHz measurement heads. An on-off keying (OOK) signal is applied through a SHF 603A multiplexer preceded by a SHF 12105A bit pattern generator. Two attenuators with total attenuation of 30 dB are employed together with a DC blocking capacitor at the input in order not to saturate the TIAs. At the output, a DC blocking capacitor and a 6 dB attenuator are used to avoid oscilloscope saturation. All attenuators have 60 GHz bandwidth while the DC block capacitors have 110 GHz bandwidth.

The resulting eye diagrams and the input eye after the multiplexer at 64 Gb/s can be seen in Fig. 7. Due to oscilloscope minimum voltage level limitations, the input eye diagram measured after 30 dB attenuators seems to be closed. Additionally, because of the bandwidth limited attenuators, the input eye brings a lot of noise. Therefore, it is expected and observed to see a noisy and not fully opened eye also on the TIAs outputs. In spite of all, an eye opening at 64 Gb/s can be clearly noticed with this measurement setup.

The performance of the presented TIAs is compared with the state-of-the-art on Table 2. The Figure-of-Merit (FOM) is calculated according to FOM calculations in [12] as $\mathrm{FOM}=(\sqrt{\mathrm{BW}}[\mathrm{GHz}]*\mathrm{TI}[\Omega]*C_D[\mathrm{pF}])/(I_{in}[\mathrm{pA}/\sqrt{\mathrm{Hz}}]*P_{DC}[\mathrm{mW}])$. Both TIAs' performances are in line with the published works.

Table 2. Comparison between the presented TIAs and the state of the art TIAs.

Ref.	Year	Technology	Topology*	TI (dBΩ)	BW (GHz)	$I_{n,in,avg}$ (pA/$\sqrt{Hz}$)	P_{DC} (mW)	Area(μm x μm)**	FOM
[6]	2010	250 nm BiCMOS	S2D	75.5	37.6	20	150	300 x 700	6.08
[7]	2012	250 nm BiCMOS	S2D	70.8	20.5	18	57	400 x 700	7.64
[8]	2013	InP	Diff.	55	107	44***	360	220 x 80	0.18
[9]	2017	130 nm BiCMOS	Diff.	62.5	60	5.5	85	550 x 550	11.03
[10]	2018	130 nm BiCMOS	Diff.	65	66	7.6	150	300 x 500	6.33
TIA1	2019	130 nm BiCMOS	Diff.	66	40	9.4*** (6.1****)	142	270 x 300	4.88
TIA2	2019	130 nm BiCMOS	Diff.	68	40	9.1***(6.5****)	142	270 x 300	6.14

*S2D = single-ended to differential, SE = single-ended; **excluding pads; ***simulated; ****extracted from measured up to 30 GHz as in [11], simulated noise is in the brackets. C_D is taken 0.5 pF when there is no diode [12].

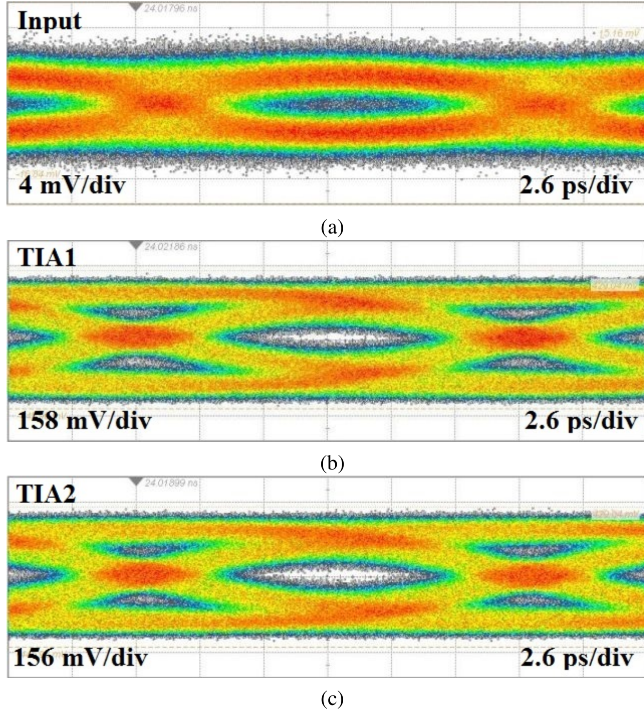


Fig. 7. Eye diagrams at 64 Gb/s (a) Input; (b) TIA1; (c) TIA2.

IV. Conclusion

This paper presented the design and performance comparison a transimpedance amplifier (TIA) first implemented in the standard IHP SG13G2 technology while the second one utilized a new backend technology with a transfer printing process. In order to make the TIA design compatible with the transfer printing technology, the topmost metal layer (TM2) has been eliminated. Compact inductor design enabled the reduction of the total chip size. Both TIAs achieved similar electrical performance occupying only a silicon area of 270 μm x 300 μm while providing 66 and 68 dBΩ transimpedance gain up to 40 GHz of bandwidth. The equivalent output noise is minimum 15 and 13 nV/$\sqrt{Hz}$ with a FOM of 4.88 and 6.14 respectively. In summary, the adopted transfer printing integration technologies enables TIA performing without any performance degradation than state-of-the-art TIAs.

Acknowledgment

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References

[1] (2018) 2018 Ethernet Roadmap. [Online]. Available: https://ethernetalliance.org/the-2018-ethernet-roadmap/

[2] G. Muliuk *et al.*, "4 × 25 Gbps polarization diversity silicon photonics receiver with transfer printed III-V photodiodes," *IEEE Photonics Technology Letters*, vol. 31, no. 4, pp. 287–290, Feb 2019.

[3] A. D. Carter *et al.*, "Si/InP heterogeneous integration techniques from the wafer-scale (hybrid wafer bonding) to the discrete transistor (micro-transfer printing)," in *2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Oct 2018, pp. 1–4.

[4] B. Razavi, *Design of integrated circuits for optical communications*. John Wiley & Sons, 2012.

[5] D. Gomez *et al.*, "Manufacturing capability of micro-transfer printing," in *Smart Systems Integration; 13th International Conference and Exhibition on Integration Issues of Miniaturized Systems*, April 2019, pp. 1–4.

[6] C. Knochenhauer, S. Hauptmann, J. C. Scheytt, and F. Ellinger, "A jitter-optimized differential 40-Gbit/s transimpedance amplifier in SiGe BiCMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 10, pp. 2538–2548, Oct 2010.

[7] B. Sedighi and J. C. Scheytt, "Low-power SiGe BiCMOS transimpedance amplifier for 25-GBaud optical links," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 8, pp. 461–465, Aug 2012.

[8] E. Bloch *et al.*, "A 107 GHz 55 dB-Ohm InP broadband transimpedance amplifier IC for high-speed optical communication links," in *2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Oct 2013, pp. 1–4.

[9] I. G. López *et al.*, "A 60 GHz bandwidth differential linear TIA in 130-nm SiGe:C BiCMOS with $<$ 5.5 pA/ $\sqrt{Hz}$," in *2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2017, pp. 114–117.

[10] I. García López *et al.*, "100 Gb/s differential linear TIAs with less than 10 pA/ $\sqrt{Hz}$ in 130-nm SiGe:C BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp. 458–469, Feb 2018.

[11] E. Säckinger, *Broadband circuits for optical fiber communication*. John Wiley & Sons, 2005.

[12] A. Romanova and V. Barzdenas, "A review of modern cmos transimpedance amplifiers for otdr applications," *Electronics*, vol. 8, no. 10, p. 1073, 2019.