Transfer Printable 64 Gbps Lumped Driver for Optical Communication

Mesut Inac, IHP – Leibniz-Institut für innovative Mikroelectronik, Frankfurt (Oder), Germany, and Technische Universität Berlin, Berlin, Germany, inac@ihp-microelectronics.com
Dr. Adel Fatemi, IHP – Leibniz-Institut für innovative Mikroelectronik, Frankfurt (Oder), Germany
Prof. Friedel Gerfers, Technische Universität Berlin, Berlin, Germany
Dr. Andrea Malignaggi, IHP – Leibniz-Institut für innovative Mikroelectronik, Frankfurt (Oder), Germany, malignaggi@ihp-microelectronics.com

Abstract

This paper presents design and performance comparison of two drivers implemented one in the standard IHP SG13G2 technology and the other in the transfer printable technology based on IHP SG13G2, but lacking of the topmost metal layer and with thinner substrate. For a fair comparison, both drivers utilize the same topology. The design of compact inductors enables with 20 µm x 20 µm size to have a core area lower than 200 µm x 300 µm. Small signal measurements of the drivers resulted in very similar performance, revealing 17 dB DC gain on both chips with only 10 GHz bandwidth degradation in transfer printable design. The extracted group delay variation of the designs are low as 2.5 ps and 3.7 ps. The measured eye diagrams at 64 Gb/s prove the performance of the drivers. Both drivers present outstanding performance in terms of gain, bandwidth and power consumption, resulting in a GBP/P_{DC} which is almost two times larger than the one presented by other designs, occupying a very limited silicon area, strongly supporting the use of transfer printing for packaging high performance lumped drivers for optical communication systems.

1 Introduction

The number of devices connected to internet is raising every day. Communication in between devices and servers creates large data traffic [1], requiring efficient and compact hardware products. The transfer printing technique is one of the enabling technologies for having efficient and compact packaging of devices. In this technique, it is possible to package electrical and optical chips onto a same substrate with minimum interconnect lengths and thus increase the package density and efficiency [2].
Optical modulator drivers are required to be broadband and linear in order to transfer the data from the transmitter back-end to the modulator [3]. Interconnects between drivers and modulators as bondwires are the main factors limiting the system performance, as bandwidth and amplitude of the transmitted signal. The minimized interconnect length proper of the transfer printing (TP) represents a promising solution to this problem [2]. TP offers to place the chips side by side and connect them by a metallization instead of bondwires. By this method, interconnect losses are minimized which is a huge problem in integrated systems. In this paper, a performance comparison between two driver amplifiers, one in a standard technology (ST) and one in a transfer printing technology (TPT) is presented. Both designed drivers have more than 17 dB small signal gain over more than 60 GHz bandwidth.

2 Circuit Design

A die to be used in TP needs to have a thickness around 20 µm, instead of a standard thickness of 200 µm in IHP SG13G2 (G2) technology, and an overall size not larger than 200 µm x 300 µm [4]. The used TPT is based on G2 technology, where the Si substrate is thinned down to 10 µm and the topmost metal layer (TM2) removed. On **Figure 1**, the schematic cross section of both ST and TPT can be seen.

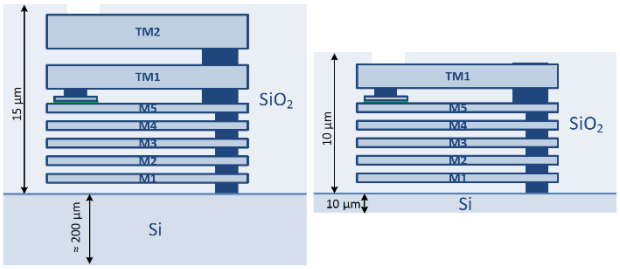

Figure 1 Cross-section representation of the used technology stacks (not on scale); (a) standard technology stack, (b) transfer printable technology stack.

The two presented circuits are designed in ST (DRI1) and TPT (DRI2). For a fair comparison, both circuits have the same topology, here reported on **Figure 2**. The fully differential circuits have two amplification stages: a differential pair stage as pre-amplifier and a differential cascode as main amplifier. The supply of the first stage and the bias of the second stage are controlled by a self-adjusting LDO. In order to extend the bandwidth, peaking inductors are utilized on both designs, together with a varactor on the first stage, which enables fine peaking control.
Due to the size requirement of the TP process, the active core of the circuit has been optimized to be compact. The output peaking inductors L3 and L4 on DRI1 are removed

on DRI2. Additionally, a special stacked inductor occupying 20 µm x 20 µm has been employed on DRI2. Transmission lines connecting the active cores and the chip pads are folded on DRI2, whereas such connection is straight on DRI1.

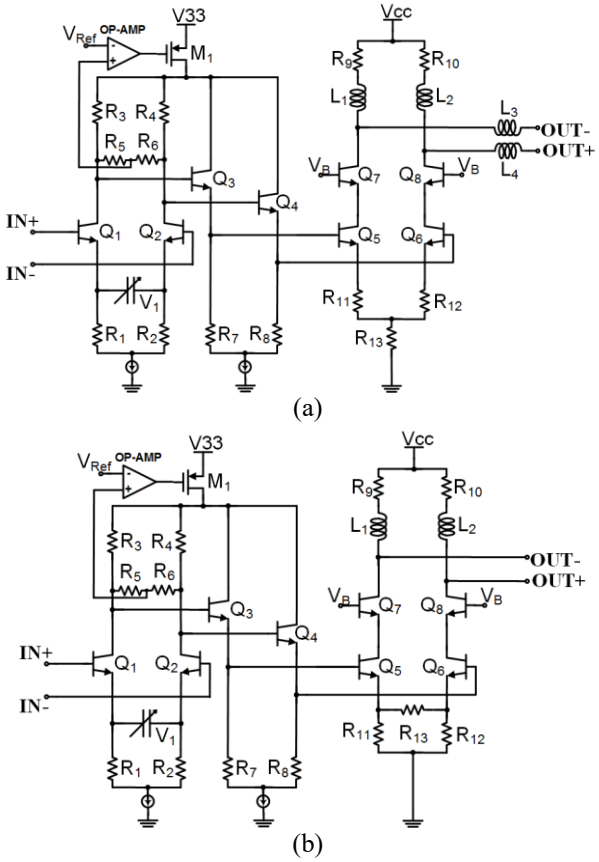

Figure 2 Driver circuit schematics; (a) DRI1 on standard technology stack, and (b) DRI2 on transfer printable technology stack.

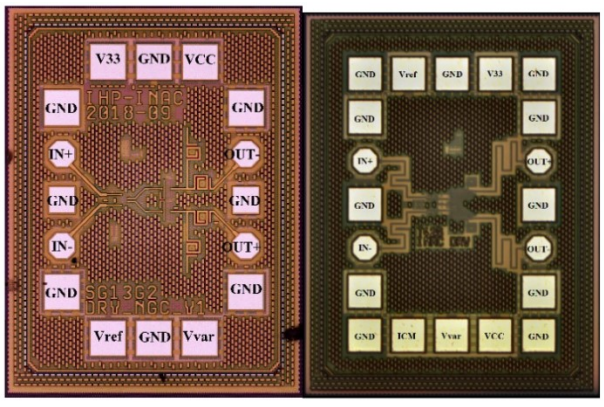

Figure 3 Micrographs of the fabricated chips; (a) DRI1 on standard technology stack, and (b) DRI2 on transfer printable technology stack.

3 Measurement Results

Micrographs of the fabricated dies can be seen on **Figure 3**. Both chips have been measured on-wafer. Small signal measurements were performed using a 4-port differential R&S ZWA67 VNA.

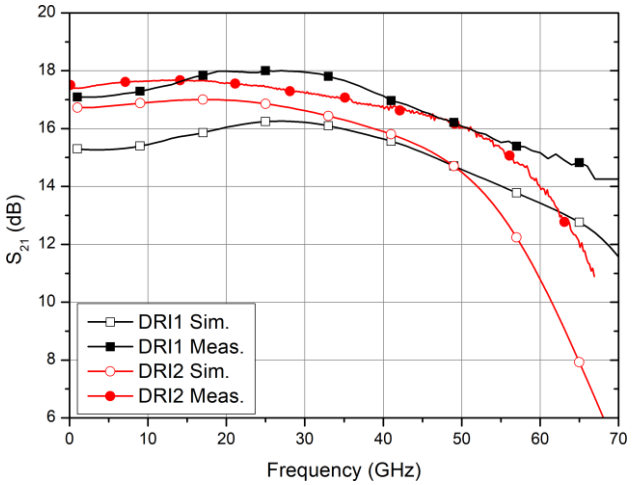

Figure 4 Small signal gain of fabricated DRI1 and DRI2 chips.

The small signal gain S21 of both circuits is shown on **Figure 4**. Both drivers present a low frequency gain around 17 dB, while DRI2 shows 10 GHz less bandwidth than DRI1. Resistive mismatches during the fabrication lead a positive shift on the gain, which is more visible on DRI1 measurements. Measured input and output return losses are shown on **Figure 5**. The output return loss of the DRI1 is higher than 10 dB until 35 GHz, while in DRI2 it is better than 10 dB only until 22 GHz. Clearly, the absence of the output inductor on DRI2 degrades its output return loss. The group delay of the circuits is extracted from the S-parameter measurements and reported on **Figure 6**, where a group delay variation of ±2.5 ps and ±3.7 ps for DRI1 and DRI2 can be seen, respectively.

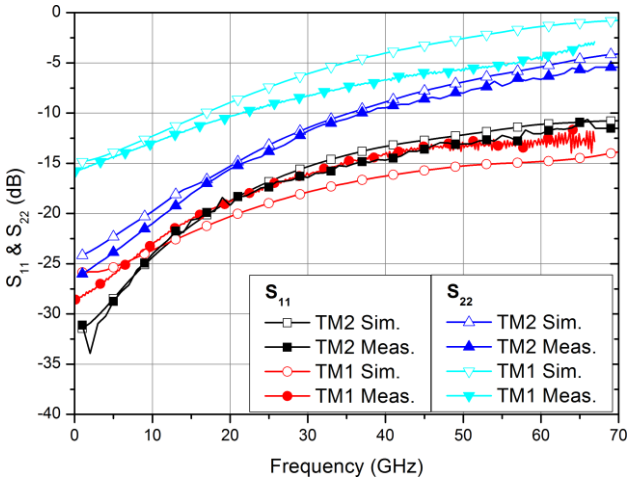

Figure 5 Input (S_{11}) and output (S_{22}) return losses of fabricated DRI1 and DRI2 chips.

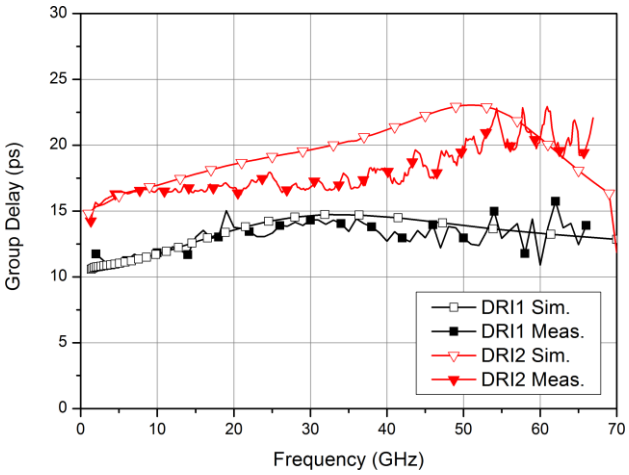

Figure 6 Extracted group delays of fabricated DRI1 and DRI2 chips.

A SHF 12105A bit pattern generator and a Keysight DCA-X 86100D wideband oscilloscope were used for performing time domain measurements. The measured eye diagrams at 64 Gb/s for both DRI1 and DRI2 can be seen on **Figure 7**. Even if the use of attenuators at the output of the devices in order to protect the oscilloscope from the high gain output deteriorates the eye diagrams, a clear eye opening is still visible, and validating the performance of both designed drivers. The overall performance of DRI1 and DRI2 are comparable at 64 Gb/s data rate, even though DRI2 has only 10 GHz of bandwidth degradation.

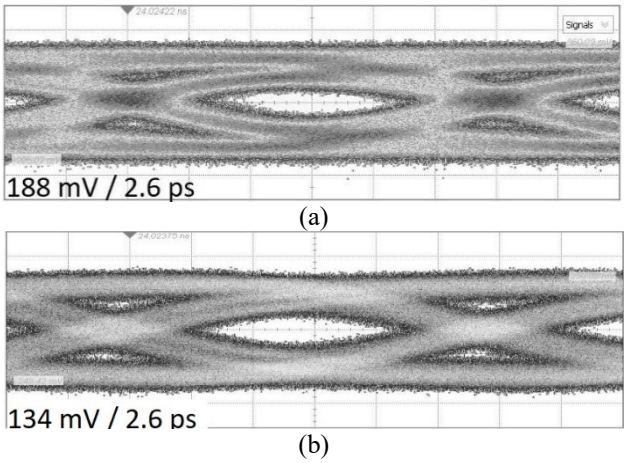

Figure 7 Driver circuit schematics; (a) DRI1 on standard technology stack, and (b) DRI2 on transfer printable technology stack.

A performance comparison of state-of-the-art lumped drivers is provided in **Table I**. Both proposed drivers present outstanding performance in terms of gain, bandwidth and power consumption, resulting in a GBP/P_{DC} of 1340 and 1130 GHz/W, which is almost two times larger than presented by other designs. These designs are occupying a very limited silicon area, and strongly supporting the use of TPT for packaging high performance lumped drivers for optical communication systems.

Table I Performance comparison between State-of-the-art lumped drivers.

Ref.	Gain (dB)	BW (GHz)	P_{DC} (mW)	Area mm^2	GBP/P_{DC} (GHz/W)
[3]	18.8	57.5	820	0.6	609
[5]	7	25	120	-	466
[6]	16.2	37.8	730	0.7	334
DRI1	17	70	370	0.12	1340
DRI2	17	60	376	0.12	1130

4 Conclusion

This paper presented the design and performance comparison of two drivers, one fabricated using standard IHP SG13G2 technology while the second one utilized a new backend technology for a transfer printing process. Compact designs enable the drivers to be easily used in any transfer printing processes. Both designs provide around 17 dB small signal gain over 60 GHz of bandwidth. Around ±3 ps group delay variation is achieved together with the highest GBP/P_{DC} FOM of 1340 and 1130 GHz/W from these chips. The performance of the chips shows the adopted transfer printing integration technologies enables driver performing without any performance degradation than state-of-the-art drivers.

5 Acknowledgements

This work is partially supported by the project “Micro assembled Terabit/s capable of optical transceivers for Datacom applications” (CALADAN). CALADAN is an initiative of the Photonics Public Private Partnership, under the grant agreement H202-ICT-2018 No. 825453.

6 Literature

[1] C. V. N. Index, “Forecast and trends, 2017–2022 white paper,” Cisco Systems Inc.: San Jose, CA, USA, 2019.

[2] A. D. Carter et al., “Si/InP Heterogeneous Integration Techniques from the Wafer-Scale (Hybrid Wafer Bonding) to the Discrete Transistor (Micro-Transfer Printing),” 2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2018, pp. 1-4.

[3] A. Zandieh, P. Schvan and S. P. Voinigescu, “57.5GHz bandwidth 4.8Vpp swing linear modulator driver for 64GBaud m-PAM systems,” 2017 IEEE MTT-S International Microwave Symposium (IMS), 2017, pp. 130-133.

[4] D. Gomez et al., “Manufacturing Capability of Micro-Transfer Printing,” Smart Systems Integration; 13th International Conference and Exhibition on Integration Issues of Miniaturized Systems, 2019, pp. 1-4.

[5] P. Rito, I. G. Lopez, A. Awny, M. Ko, A. C. Ulusoy, and D. Kissinger, “A DC-90-GHz 4-V_{pp} modulator driver in a 0.13-µm SiGe: C BiCMOS process,” IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 12, pp. 5192–5202, 2017.

[6] M. Nagatani, Y. Bouvier, H. Nosaka and K. Murata, “A 3-Vppd 730-mW Linear Driver IC Using InP HBTs for Advanced Optical Modulations,” 2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), 2013, pp. 1-4.