BiCMOS eingebettete Mikrofluidiktechnologie basierend auf Wafer-Bonding-Techniken für Biosensor-Anwendungen
BiCMOS Embedded Microfluidic Technology Based on Wafer Bonding Techniques for Biosensor Applications

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Kurzfassung

In dieser Arbeit wird Mikrofluidik auf 200 mm Waferebene zusammen mit einer Hochleistungs-SiGe-BiCMOS-Technologie integriert. Durch Kombination von Si Mikrofluidik und BiCMOS Elektronik können Lab on Chip Systeme (LoC) mit hohem Durchsatz auf 200 mm Wafern hergestellt werden. Ein Niedrigtemperatur-Fusion-Bonding bei 300 °C und ein Adhesive-Bonding werden angewendet, um diese Technologien zusammen zu integrieren. Durch das entwickelte Integrationsverfahren können die elektrischen und mikrofluidischen Interfaces zum Chip voreinander getrennt werden und ermöglichen damit hochintegrierte LoC Systeme. Diese entwickelte Technologie hilft, sowohl die Kosten zu senken als auch die Empfindlichkeit zu erhöhen, welche die Bedürfnisse von LoC-Systemen erfüllen.

Abstract

In this paper, a 200 mm wafer level integration of microfluidics together with a high performance SiGe BiCMOS process is presented. Using high throughput 200 mm wafer level semiconductor processing steps and wafer bonding techniques, Lab-on-Chip (LoC) systems with combination of Si microfluidics and BiCMOS electronics are realized. A low temperature fusion bonding at 300 °C and an adhesive bonding are applied to integrate these technologies together. Based on the BiCMOS microfluidic integration technique, the electrical and microfluidic interfaces are separated from each other enabling highly miniaturized LoC systems. This developed technology helps to reduce the costs and increase the sensitivity which satisfy the needs of LoC systems.

1 Introduction

Increasing interest on analysing small amounts of chemical and biological samples in a fast and reliable way leads scientists to research on electronics and microfluidic systems [1]. Lab-on-Chip (LoC) concepts are being used [2] in order to satisfy the requirements on the area of chemical and biological sample analysis. Smaller distances between sample and sensing units are increasing the sensitivity on small amounts of samples [3]. Demonstrated LoC systems are already in relatively large size [4] due to the polymeric channel structures and the limited alignment accuracy of the channels. In order to miniaturize the LoC which consist of microfluidic and sensing interfaces, better integration solutions are required.

Integrated microfluidics and electronics on LoC systems is a solution for the miniaturization of these systems [5]. Using standardised BiCMOS fabrication and 200 mm wafer bonding techniques, it is possible to have sensors close to the fluidic interface while having smaller size of channels. In this work, the integration of microfluidics into IHP BiCMOS technology by 200 mm wafer bonding techniques for biosensor applications is presented. Using high throughput 200 mm semiconductor processing steps and wafer bonding techniques, LoC systems with combination of Si microfluidics and BiCMOS electronics can be realized. The combination of these two technologies helps to reduce the costs as well as increasing the sensitivity by decreasing the distances between sensors and biological samples which will satisfy the needs of future LoC systems.

2 Process Flow

In order to integrate microfluidics and BiCMOS technologies on 200 mm semiconductor processing platform, a 3-wafer stack LoC system is proposed. This 3-wafer stack consists of one BiCMOS wafer which includes sensors and the active circuitry, one Si microfluidic channel wafer to

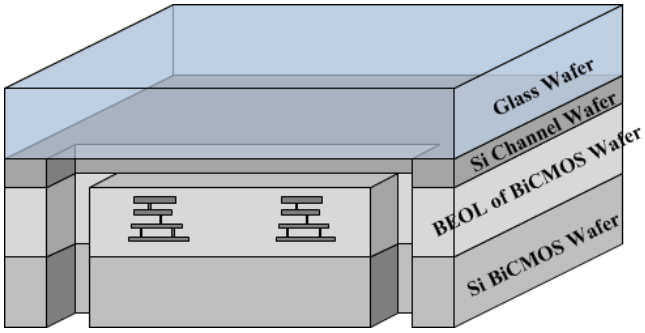

Figure 1 3D representation of the microfluidic channel packaging.

provide channel structures and one glass wafer to enclose the channels with transparent material (Figure 1). This 3-wafer-stack is integrated with 200 mm wafer bonding techniques. The first bonding occurs between the BiCMOS wafer and the Si microfluidic channel wafer and the second bonding occurs between the backside of microfluidic channel wafer and a glass wafer.

The general process flow can be seen in Figure 2. The process starts with 2 bare Si wafers. On the first wafer (Figure 2(a)), sensors and circuits for LoC system are fabricated using standard IHP 200 mm BiCMOS processes (Figure 2(b)). Additionally, the inlet and outlet are opened from backside of the wafers with through-Si etching (Figure 2(c)). On the second wafer (Figure 2(d)), channel structures are etched into a bare Si wafer using standard BiCMOS process steps (Figure 2(e)). In this case, the depth of the channel plays an important role for defining the channel height. Later, these two wafer are bonded together (Figure 2(f)). In order to achieve high quality bonding, both of the wafers have to have microroughness values less than 0.5 nm. Optimized oxide deposition and planarization [6] techniques are applied to have smooth surfaces on BiCMOS fabrication line.

After BiCMOS and Si microfluidic channel wafers are fabricated on BiCMOS line, the wafers are bonded together from their front sides by low-temperature oxide-oxide fusion bonding. The Si microfluidic channel wafer's surface is activated by low power N_2 plasma in order to decrease the annealing temperature for high bonding quality. The bonding is performed at room temperature under 5 kN applied force. After the bonding, the wafers are annealed at 300 °C for 1 hour. These wafers are aligned using the alignment tool $EVG-SmartViewNT2^{®}$ providing a less than 1 μm alignment accuracy.

Then the bonded stack is grinded from the backside of the Si microfluidic channel wafer using both #4800 and poly-grinding meshes. (Figure 2(g)). There are two main reasons of wafer grinding. The first reason is to expose the channels. Exposing channels gives opportunity to encapsulate the channels with a transparent wafer. The second reason is to adjust the channel heights. The Si microfluidic channel wafer grinding can be stopped at a defined level to provide the required channel heights.

When the channels are adjusted and exposed, a transparent glass wafer is bonded with an adhesive on top of the

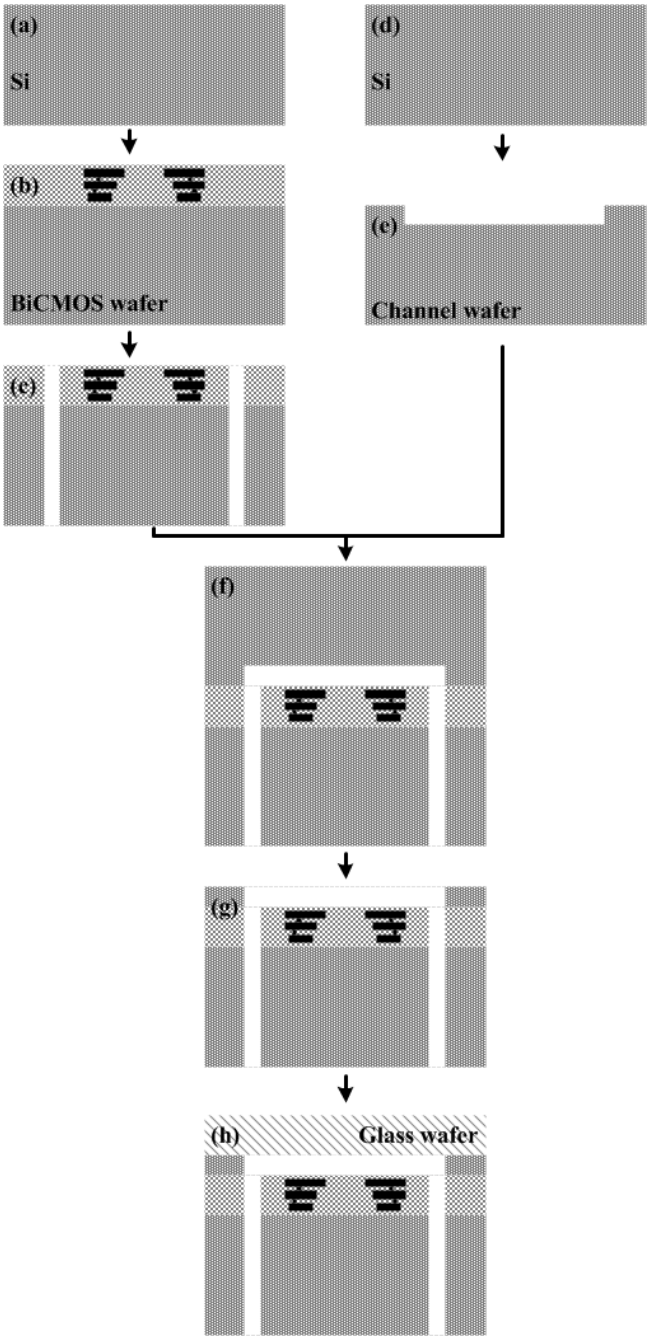

Figure 2 Schematic representation of the microfluidic packaging processes steps. On a Si wafer (a), active circuitry (b) and microfluidic inlets (c) are opened and this wafer bonded (f) together with a channel wafer (e) built on a bare Si wafer (d). After the grinding (g) and adhesive bonding steps (h), transparent microfluidic channels are encapsulated.

microfluidic channels. Due to high roughness values after grinding which does not allow for second fusion bonding, a chemical and bio-compatible adhesive is used to bond the glass wafer on top. This transparent wafer enables optical observations simultaneously with electrical measurements on the sensors. Since the glass bonding is applied on full 200 mm wafer, not only the channels are encapsulated, but also electrical pads are covered with glass wafer. In order

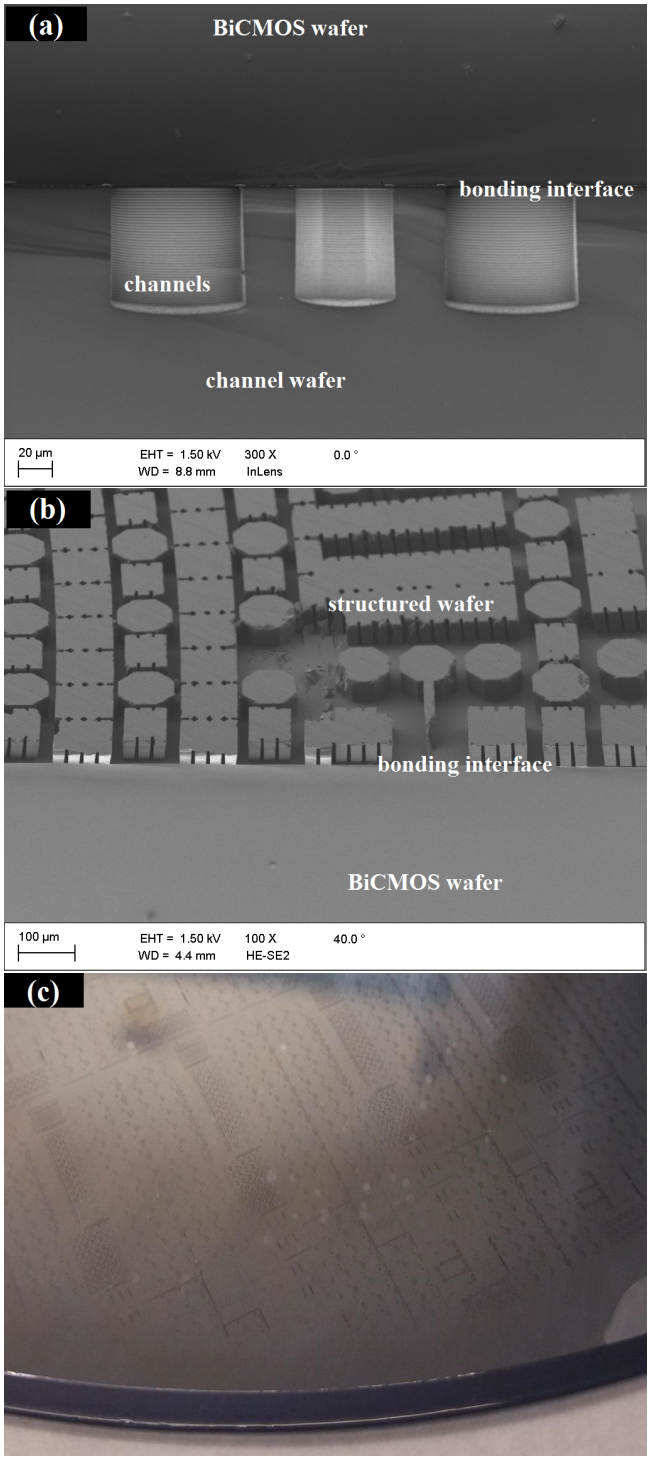

Figure 3 Demonstrated process flow steps (a) Channels after fusion bonding (b) Bonded wafer after backside grinding for exposing the channels (c) 3-wafer stack after glass bonding.

to open the electrical pads and separate the microfluidic LoCs, a two level dicing is applied.

3 Microfluidic LoC Results

Firstly, the process flow on dummy wafers is demonstrated. In Figure 3(a), it can be seen that a Si channel wafer is

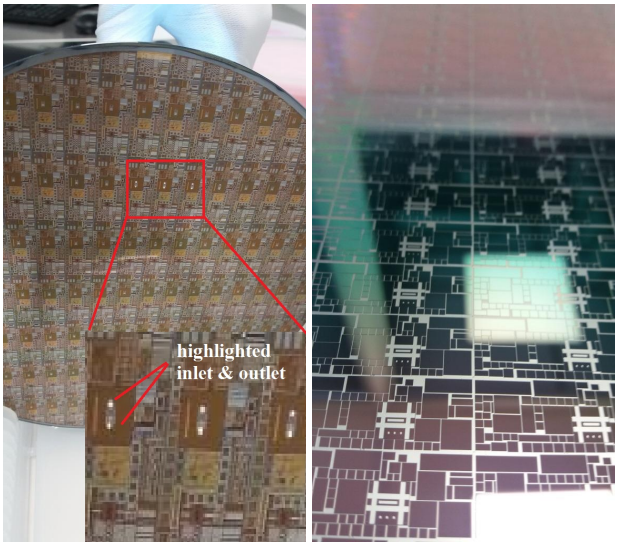

Figure 4 Microfluidic packaging for LoC applications (the BiCMOS wafer including highlighted inlets and outlets (*left*) and the channel wafer (*right*) before integration)

bonded to a wafer with 100 nm oxide on top in order to demonstrate the fusion bonding with Si microfluidic channel wafer. The formation of the channels on the interface can be seen in this figure. Later the Si microfluidic channel wafer is grinded from backside and the channel structures are exposed (Figure 3(b)). In this step, the height of the channels are determined by the grinding. After the grinding, a glass wafer is bonded to the stack to encapsulate the channels and make inside of the channel visible. This 3-wafer stack after the glass bonding step can be seen in Figure 3(c).

After the successful demonstrations of each step of the 3-wafer stack microfluidic LoC system flow as in Figure 3, the integration of these 3-wafer stack is finalized. This time, instead of dummy wafer, fully processed BiCMOS wafer is used in the flow.

The inlet and the outlet on the BiCMOS wafer is highlighted in the Figure 4 left. This wafer is bonded together with the Si microfluidic channel wafer (in Figure 4 right) on the front sides. Due to high accuracy of wafer alignments, and the smaller feature sizes, the total area of the LoC system decreases. Then a grinding follows the bonding of the BiCMOS and Si microfluidic channel wafers.

After the backside grinding of the microfluidic channel wafer, the channel is exposed. The sensors and microfluidic inlet on BiCMOS wafer and the microfluidic channel can be seen in Figure 5(a). Later, the stack consist of BiCMOS wafer and a Si microfluidic channel wafer is bonded with a transparent glass wafer, and the wafer level integration of microfluidics and electronics is completed.

In order to separate the dies of Si microfluidic LoC, a 2-level dicing is applied on the wafer. First, the glass wafer is diced to remove the part on the electrical pads, then the chips are separated by dicing. A cross-section image of the final microfluidic LoC can be seen in Figure 5(b). The microfluidic samples are flowing from inlet to outlet through

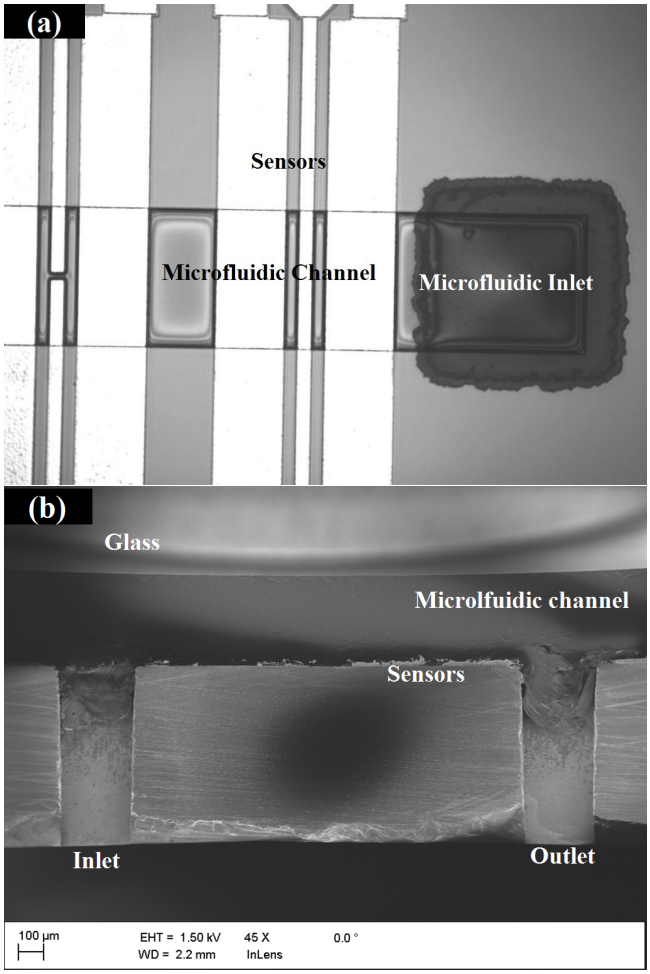

Figure 5 Demonstrated LoC systems (a) top view of microfluidic chip including microfluidic inlet and sensors (b) cross-section image of microfluidic LoC system.

electrical sensors. Since the sensors are directly located inside the microfluidic channels, the sensitivity of the sensors are increased.

4 Conclusion

A BiCMOS compatible 200 mm wafer level integration of microfluidic technology is demonstrated. A low temperature fusion bonding and an adhesive bonding are applied to combine a BiCMOS wafer, a Si microfluidic channel wafer and a glass wafer. Encapsulation by a glass wafer enables to have simultaneous optical and electrical measurements which is highly desired by the bio-medical community. The presented 200 mm wafer level integration approach of electronics and microfluidics increases the throughput and decreases the costs of the LoC systems for bio-medical applications.

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