DOI: 10.23919/EuMIC61603.2024.10732403

A Signal Source in J-Band with 237-287 GHz Tuning Range in a 130-nm SiGe BiCMOS Process

Farabi Ibne Jamal[#1], T. Mausolf[#], M. Yazici[#], F. Vater[#], C. Carta[#$], R. Scholz[#]
[#]IHP, Germany
[$]Technische Universität Berlin, Germany
{[1]jamal}@ihp-microelectronics.com

***Abstract* — This article presents a J-band signal source fabricated in a 130 nm SiGe BiCMOS process which consists of a K-band voltage controlled oscillator (VCO), a D-band frequency quadrupler (X4) and an amplifier (AMP) and a J-band frequency doubler (X2). It has a tuning range of 19.1 % (237-287 GHz) centered at 262 GHz with an average output power of −3.1 dBm. Average measured phase noise is −78.4 dBc/Hz at 1 MHz offset. The chip has an area of 1.6 mm^2 and it consumes a maximum power of 622 mW. Thus it results in 0.15 % DC-to-RF efficiency. It stands out as a fully integrated state-of-the-art silicon-based signal source at J-band frequencies, with a wide tuning range and practical output power.**

***Keywords* — BiCMOS, SiGe, J-band, signal source, wideband, VCO, frequency multiplier, quadrupler, doubler.**

I. Introduction

The advancements in sub-THz technologies have significantly favored diversified applications such as high-speed short-range wireless communication [1], high-resolution imaging, sub-THz spectroscopy [2], and radar systems [3] etc. Efficient wideband signal sources play a crucial role in providing the necessary bandwidth. Thus, the systems can meet the demands of the above mentioned applications and offer compact, modular and scalable solutions with high-end performances. However, as the current technology stands, limited breakdown voltage of active devices and low quality factor of passive components are blocking factors for low-noise, high-power signal sources. A stable and low-noise low-frequency source (e.g. a K-band VCO) in conjunction with a frequency multiplier is a strategical approach to overcome the limitations in generating sub-THz signals. Distributing the low-frequency signal is also convenient when constructing a multi-module system even for multi-band operations [4], [5]. It offers low-cost, low-loss and low-complexity without compromising the performances, leading to a reliable and robust multi-module system.

This paper describes the design, implementation and characterization of a fully integrated J-band signal source in a 130 nm SiGe BiCMOS process. It features a frequency multiplier chain followed by K-band VCO for generating a single-ended J-band output signal. With output frequencies ranging from 237 GHz to 287 GHz and an average output power of −2.6 dBm, this work showcases the potential of such integrated circuits for high-frequency applications.

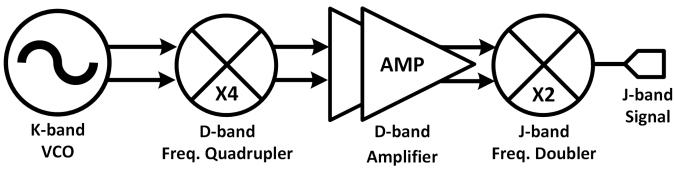

Fig. 1. Block diagram of the J-band signal source.

II. System Architecture and Circuit Design

Fig. 1 shows the architecture of the proposed J-band signal source. In the first stage, an wideband VCO generates a differential K-band signal, which is transformed into a differential quadrature signal by using a polyphase filter (PPF). The quadrature K-band signal from the PPF is quadrupled into a differential D-band signal in two subsequent steps. A two-stage amplifier amplifies the D-band signal to provide sufficient input power for the next stage. A common emitter push-push frequency doubler and a common-base amplifier provide the singled-ended J-band output signal at the end.

The signal source is fabricated in 130 nm IHP SG13G2 SiGe BiCMOS process. The MPW services offer npn HBTs (f_T / f_{max} = 350/ 450 GHz), 3.3 V I/O and 1.2 V CMOS logic nodes, MIM capacitors, MOS varactors and poly-silicon resistors. Backend of Line (BEOL) process offers seven metal stacks with two thick and five thin Aluminum layers. The design aspects of the building blocks are described below.

A. K-band VCO

In order to generate periodic signals in the K-band, a VCO is implemented based on differential common-emitter Colpitts topology [6]. The schematic is shown in Fig. 2. A common-base buffer amplifier is cascoded in the following stage. Non-uniform tapered microstrip lines have been used to improve the tuning range [7]. It is supplied with a 4 V source and consumes 61 mW to 165 mW power. For tuning the frequencies, there are two possibilities: the control voltage of the varactor (V_T) to vary the capacitances and the control voltage to tune the core current (V_{CM}, i.e. g_m) in the VCO. The VCO oscillates from 29 GHz to 41 GHz for a tuning voltage (V_T) of −1 V to 4 V in simulation and provides ca. 5- 8 dBm output power.

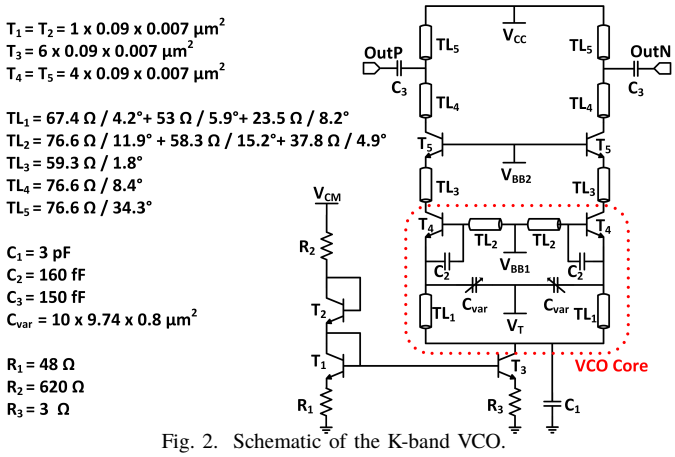

Fig. 2. Schematic of the K-band VCO.

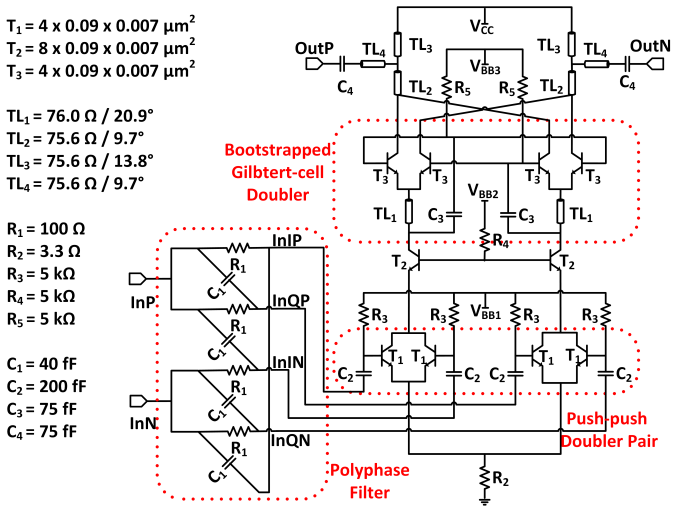

Fig. 3. Schematic of the D-band frequency quadrupler.

B. D-band Frequency Quadrupler

Frequency multiplication in the D-band is performed in two stages. In the first stage, the differential K-band signal is converted into differential quadrature signal by using a polyphase filter. The in-phase and quadrature differential output are fed to two push-push doublers. It results in a balanced differential signal at the second harmonic in the V-band. In the second stage, the signal is fed into a differential common-base buffer followed by a boot-strapped Gilbert-cell doubler [8]. It delivers a quadrupled differential signal at the output in the D-band. Figure 3 depicts the schematic of the frequency quadrupler. It needs a 4 V voltage source and 112 mW power. An input power of 6 dBm yields a peak output power of 1 dBm at 142 GHz. The 3-dB bandwidth is 124 GHz to 162 GHz (27.1 %) with an average conversion loss of 6.2 dB in simulation. There is at least a 20 dB harmonic suppression seen for the strongest harmonic signal at the 8th harmonic.

C. D-band Amplifier

The output power of the D-band quadrupler is not sufficient to drive the J-band frequency doubler. Therefore, a two-stage differential D-band amplifier is included to after the quadrupler. It adopts a stacked configuration to achieve high output power [9]. Schematic diagram of the amplifier is depicted in Fig. 4. It is supplied with a 4 V power source and uses 244 mW of power. In small-signal simulation, the results indicate a maximum gain of 12 dB at 145 GHz and the 3-dB bandwidth is 31.5 GHz (126 - 157.5 GHz). In large-signal simulation, for an input power of −1 dBm, 9 dBm peak output power is observed at 143 GHz and the 3-dB bandwidth is distributed from 115 GHz to 160 GHz.

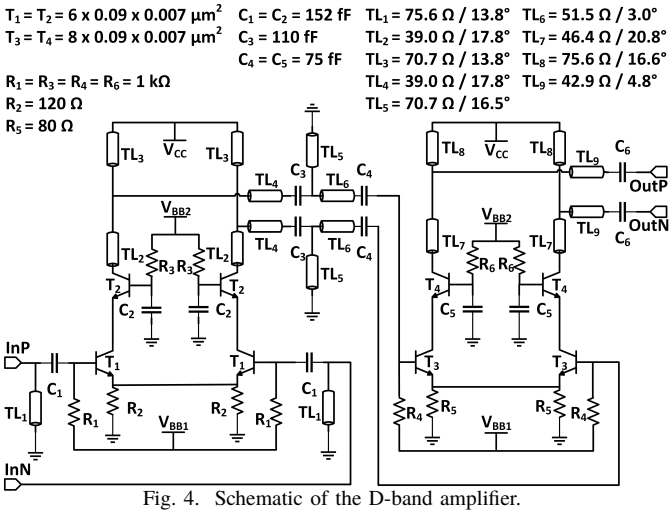

Fig. 4. Schematic of the D-band amplifier.

D. J-band Frequency Doubler

A common-emitter push-push topology is adopted to implement the frequency doubler in J-band. Second harmonic current has maximum amplitude and third harmonic current is approximately half of the second harmonic in class C operation. In a differential input, even harmonics are combined in phase and odd harmonics, including the fundamental signal cancel out each other in the push-push topology at the common node output [9]. A common-base amplifier is added to improve the output power. Fig. 5 illustrates the schematic of the frequency doubler. A 4 V power supply is needed, with a power consumption of 101 mW. When an input power of 9 dBm is applied at 143 GHz in HB-simulation, the peak output power is 1.5 dBm at 286 GHz. An input power of 6 dBm at 115 GHz and at 160 GHz yield output power of 2.5 dBm and −31.3 dBm at 230 GHz and 320 GHz respectively. The 3-dB bandwidth ranges from 211 GHz to 278 GHz, with a peak output power of 3 dBm at 237 GHz when the input power is 6 dBm.

III. Measurement Setup and Results

Chip photograph is shown in Fig. 6. The DC pads have a dimension of 80×80 µm and a pitch of 100 µm. The single-ended RF pad has a dimension of 20×60 µm.

A. Measurement Setup

On-wafer measurements were performed to characterize the signal source. It was supplied with multiple DC sources using ZPROBE DC probes from CascadeMicrotech®. The RF

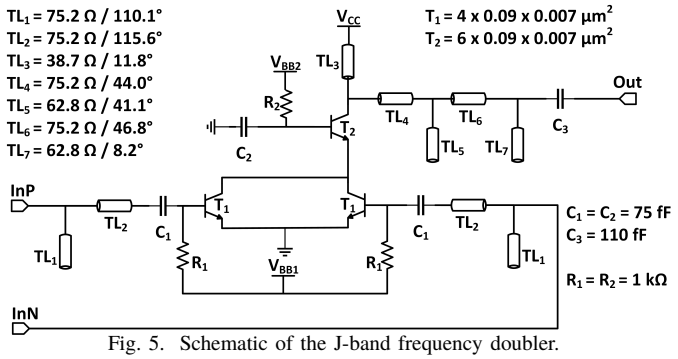

Fig. 5. Schematic of the J-band frequency doubler.

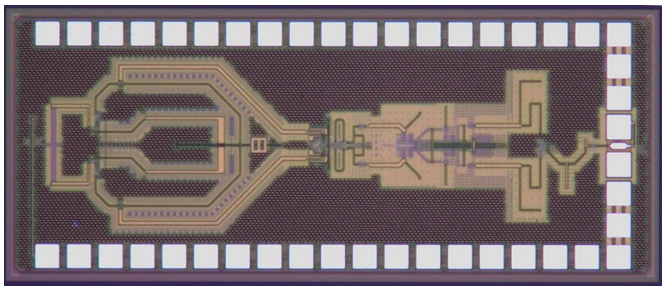

Fig. 6. Chip photograph (2 mm×0.8 mm).

output was probed by WR-3 (220-325 GHz) Infinity Waveguide Probe (I325-T-GSG-50-BT) from FormFactor™. It includes a tranmission loss of 6.5 dB in J-band frequencies. In order to characterize the output frequencies and power simultaneously, a directional coupler (WSC 220-325, from RPG-Radiometer Physics GmbH) is added after the probe. The coupler has a coupling factor of 10 dB and a transmission loss of 2 dB. The thru output of the coupler is delivered to VDI Erickson PM5 power meter system for RF power measurement. It is then tapered into a WR-10 from WR-3 system and then fed to the WR-10 power sensor. This tapering incurs 0.6 dB loss. Thus, the power measurement path experiences 9.1 dB loss. The coupled output of the coupler is provided to the combination of harmonic mixer (FS-Z 325, from RPG-Radiometer Physics GmbH) and spectrum analyzer (R&S® FSW67, from Rohde & Schwarz) for the frequency detection. The harmonic mixer uses a local oscillator input of 10-14.77 GHz and a frequency multiplier with a multiplication factor of 22. Typically it has 38 dB conversion loss. Excluding the cable and harmonic conversion loss, spectrum analyzer sees a transmission loss of 16.5 dB. The output power recorded in both power meter and spectrum analyzer have been averaged to ensure a distributed and accurate measurement. The setup is shown in Fig. 7. In order to measure the harmonic contents in lower bands (i.e. D-band: 110-170 GHz), a similar setup was implemented with relevant probe, coupler, transition and harmonic mixer.

B. *Results and Discussion*

Measured output signals are shown in Fig. 8. It shows a minimum and maximum output frequencies of 237.5 GHz and 287.6 GHz respectively while the tuning voltage (V_T) was

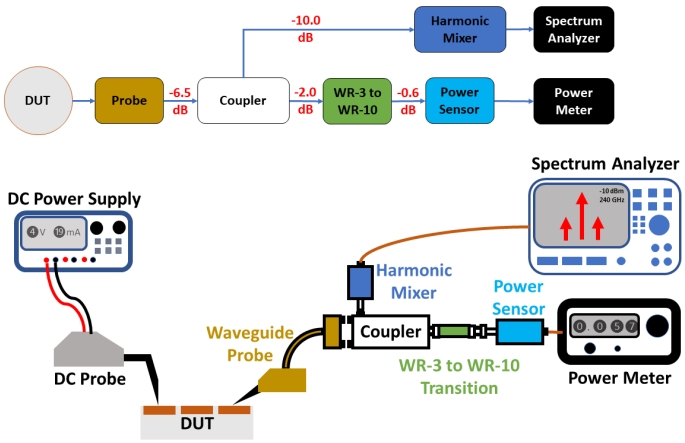

Fig. 7. Measurement setup for spectrum and output power.

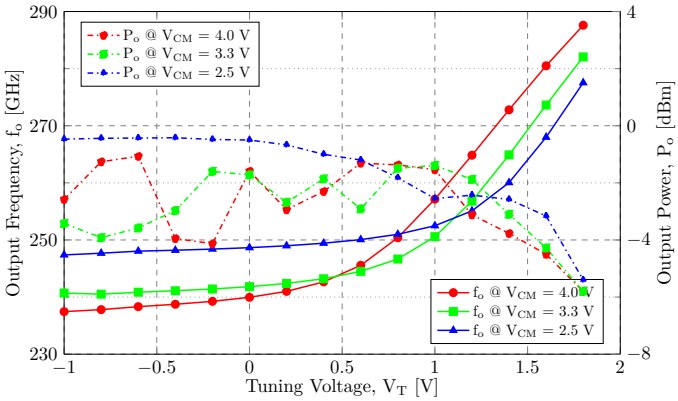

Fig. 8. Measured output frequencies and power.

−1 V to 1.8 V for three cases of V_{CM}. A maximum power of −0.4 dBm was observed at 248.2 GHz while minimum power was −5.8 dBm at 287.6 GHz. Phase noise were measured in real-time at output frequencies in the spectrum analyzer without cross-correlation method. Thus, the phase noises of the local oscillator and its harmonics in the spectrum analyzer affected the phase noise of the signal source. For simplification, the attenuation caused by the probe and coupler have been deducted to get an approximation of the phase noise. Average measured phase noise is −78.4 dBc/Hz at 1 MHz offset frequency. Figure 9 demonstrates the comparison of output power between simulations and measurements. As it is seen, measured power is ca. 4 dB less than simulation. RF pad encounter ca. 0.2 dB loss in these frequencies. 4th harmonic signals were seen in the D-band measurement setup and the results are shown in Fig. 10. In this measurement, when V_T was tuned from −1 V to 4 V, D-band signals were observed from ca. 118 GHz to 160 GHz within 3-dB bandwidth.

Table 1 summarizes the performances of relevant publications in J-band frequencies. This work compares reasonably well against the state-of-the-art with wide tuning range and practical output power. However, the noise characteristics and DC-to-RF efficiency are the points which need improvement.

Table 1. Summary and comparison of J-band signal sources from literature.

Reference	Technology	f_T / f_{max} [GHz]	Output frequency [GHz]	Tuning range [%]	Peak RF power [dBm]	DC power [mW]	Phase noise at 1 MHz offset [dBc/Hz]	DC-to-RF efficiency [%]	Chip area [mm^2]
[10]	55 nm BiCMOS	330 / 350	234-261	10.9	7.2	566	-82	1.3	0.83
[11]	65 nm CMOS	160 / 200	283-296	4.5	-1.2	325	-78	0.23	0.36
[12]	130 nm BiCMOS	250 / 300	292-318	8.5	0.6	142	-82.7	0.80	0.30
[13]	120 nm BiCMOS	300 / 400	288-311	7.7	-1.7	167	-101.6	0.40	-
[14]	130 nm BiCMOS	300 / 450	273.5-312	13.2	2.3	435	-88.5	0.40	1.25
[5]	130 nm BiCMOS	300 / 500	223-276	21.2	3.1	890	-85.4	0.23	2.27
This work	130 nm BiCMOS	350 / 450	237.5-287.6	19.1	-0.4	622	-78.4	0.15	1.60

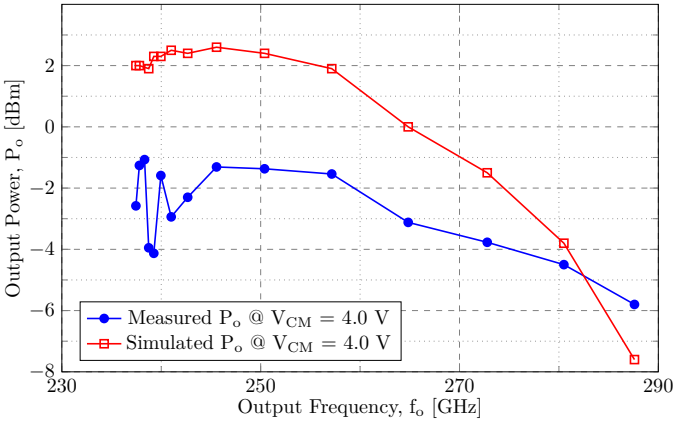

Fig. 9. Measured and simulated output power at V_{CM} = 4.0 V.

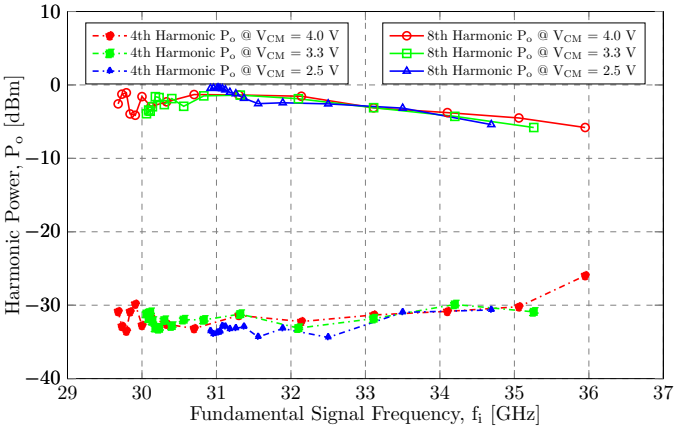

Fig. 10. Measured output power at 4th and 8th harmonic frequencies.

IV. Conclusion

This work demonstrates a J-band signal source consisting of a K-band VCO and a multiplier (X8) chain implemented in a 130 nm SiGe BiCMOS process. The tuning range is 19.1 % (237-287 GHz) centered at 262 GHz with a maximum output power of -0.4 dBm. This silicon-based signal source offers high-performance solution in J-band spectrum. Thus, it is ideal for a wide range of applications in radar, communications, imaging and instrumentation.

Acknowledgment

This work has been supported by European Commission as part of the project SMARTWAY.

References

[1] M. H. Eissa, A. Malignaggi, R. Wang, *et al.*, "Wideband 240-GHz Transmitter and Receiver in BiCMOS Technology With 25-Gbit/s Data Rate," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2532–2542, 2018.

[2] K. Schmalz, N. Rothbart, A. Glück, *et al.*, "Dual-Band Transmitter and Receiver With Bowtie-Antenna in 0.13 µm SiGe BiCMOS for Gas Spectroscopy at 222 - 270 GHz," *IEEE Access*, vol. 9, pp. 124 805–124 816, 2021.

[3] R. Hasan, M. H. Eissa, W. A. Ahmad, H. J. Ng, and D. Kissinger, "Wideband and Efficient 256-GHz Subharmonic- Based FMCW Radar Transceiver in 130-nm SiGe BiCMOS Technology," *IEEE Trans. Microw. Theory Tech.*, vol. 71, no. 1, pp. 59–70, 2023.

[4] H. J. Ng, M. Kucharski, W. Ahmad, and D. Kissinger, "Multi-Purpose Fully Differential 61- and 122-GHz Radar Transceivers for Scalable MIMO Sensor Platforms," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2242–2255, 2017.

[5] E. Turkmen, I. K. Aksoyak, P. Djondovic, *et al.*, "A 223–276-GHz Cascadable FMCW Transceiver in 130-nm SiGe BiCMOS for Scalable MIMO Radar Arrays," *IEEE Trans. Microw. Theory Tech.*, vol. 71, no. 12, pp. 5393–5412, 2023.

[6] H. Li and H.-M. Rein, "Millimeter-Wave VCOs With Wide Tuning Range and Low Phase Noise, Fully Integrated in a SiGe Production Technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 184–191, 2003.

[7] F. I. Jamal, J. Wessel, and D. Kissinger, "A Low-Power K-Band Colpitts VCO with 30% Tuning Range in a 130 nm SiGe BiCMOS Technology," in *2018 IEEE 18th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2018, pp. 37–40.

[8] F. I. Jamal, M. H. Eissa, J. Borngräber, H. J. Ng, D. Kissinger, and J. Wessel, "A Low-Power 190-255 GHz Frequency Quadrupler in SiGe BiCMOS Technology for On-chip Spectroscopic Applications," in *2017 IEEE Radio and Wireless Symposium (RWS)*, 2017, pp. 94–97.

[9] A. Ali, J. Yun, M. Kucharski, H. J. Ng, D. Kissinger, and P. Colantonio, "220–360-GHz Broadband Frequency Multiplier Chains (x8) in 130-nm BiCMOS Technology," *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 7, pp. 2701–2715, 2020.

[10] S. Shopov, A. Balteanu, J. Hasch, P. Chevalier, A. Cathelin, and S. P. Voinigescu, "A 234–261-GHz 55-nm SiGe BiCMOS Signal Source with 5.4–7.2 dBm Output Power, 1.3% DC-to-RF Efficiency, and 1-GHz Divided-Down Output," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2054–2065, 2016.

[11] Y. M. Tousi, O. Momeni, and E. Afshari, "A 283-to-296GHz VCO with 0.76mW peak output power in 65nm CMOS," in *2012 IEEE International Solid-State Circuits Conference*, 2012, pp. 258–260.

[12] F. Ahmed, M. Furqan, B. Heinemann, and A. Stelzer, "0.3-THz SiGe-Based High-Efficiency Push–Push VCOs With > 1-mW Peak Output Power Employing Common-Mode Impedance Enhancement," *IEEE Trans. Microw. Theory Tech.*, vol. 66, no. 3, pp. 1384–1398, 2018.

[13] S. P. Voinigescu, A. Tomkins, E. Dacquay, *et al.*, "A Study of SiGe HBT Signal Sources in the 220–330-GHz Range," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2011–2021, 2013.

[14] P. Zhou, J. Chen, P. Yan, Z. Chen, D. Hou, and W. Hong, "A 273.5–312-GHz Signal Source With 2.3 dBm Peak Output Power in a 130-nm SiGe BiCMOS Process," *IEEE Trans. Microw. Theory Tech.*, vol. 10, no. 3, pp. 260–270, 2020.