Low Insertion Loss D-band SPDT Switches Using Reverse and Forward Saturated SiGe HBTs

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***Abstract*— This paper presents two D-band SPDTs utilizing forward and reverse saturated SiGe HBTs. The SPDT switch designs are based on quarter-wave double shunt topology and state-of-the-art performance are achieved at D-band frequencies from 110 to 170 GHz. Measurement results of the reverse saturated SPDT switches show minimum insertion loss of 2 dB (including pads losses) at 140 GHz and insertion loss better than 2.3 dB from 120 GHz to 170 GHz. The power consumption of both SPDTs is 3.04 mW at 0.9 V supply.**

***Index Terms*— D-band, Single Pole Double Throw (SPDT), forward and reverse saturated, SiGe BiCMOS**

I. INTRODUCTION

The frequency band from 110 to 170 GHz (D-band) has a low atmospheric attenuation which makes it suitable for medium distance backhaul high data rate wireless communication. Due to the extremely high operating frequency, the design of integrated D-band transceivers [1] has to be supported by a high performance integrated technology, such as the new generation IHP 0.13 μm SiGe BiCMOS Heterojunction Bipolar Transistors (HBT) technology. In modern high frequency communication systems, phased arrays play a dominant role.

The single pole double-throw (SPDT) switch is one of the critical block of these systems, which is used for toggling between transmit and receive modes. The overall performance of the system is highly affected by insertion loss, isolation and linearity of the switch. That is why, in order to increase system performance, D-band mm-wave SPDT switches are designed in different technologies as CMOS [2], III-V [3] and SiGe BiCMOS [4]–[5].

In this paper, both forward and reverse saturated SPDTs covering the entire D-band are realized. Quarter-wave double-shunt SPDTs are designed in a 0.13 μm SiGe HBT technology. The measurement of reverse saturated SPDT switch demonstrate state of art performance at D-band compared to any other switch realized in different technologies.

Section II describes the design of the fabricated SPDTs in details. Section III compares both simulated and measured results of the forward and reverse saturated SPDTs.

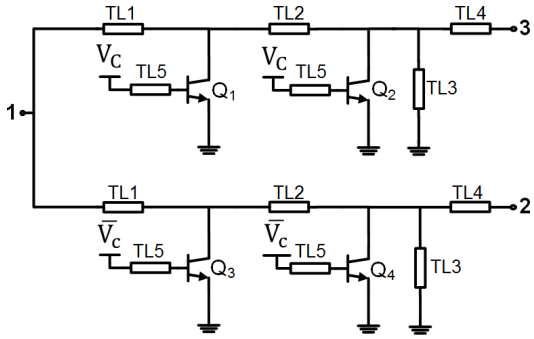
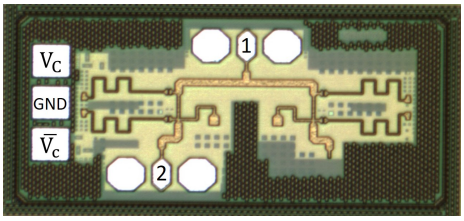


Fig. 1: Schematic of the forward saturated SPDT

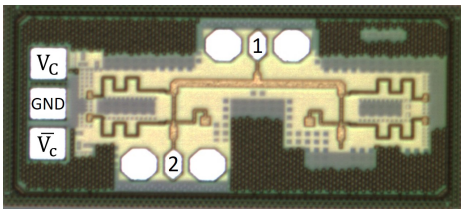
II. CIRCUIT DESIGN

The schematic of a forward saturated SPDT is shown in Fig. 1. Both presented designs are based on a quarter-wave double shunt switch topology. In this topology, if V_C is at a high voltage Q_1 and Q_2 are turned on, being $\overline{V_C}$ at low voltage Q_3 and Q_4 are turned off. Being TL1 a quarter wave transmission line, when Q_1 and Q_2 are in on state the input of TL1 (port 1) will present high impedance and the upper branch will be isolated. The lower the impedance offered by Q_1 and Q_2, the higher the isolation. At the same time, Q_3 and Q_4 are turned off and they present a high-impedance to the signal path of the lower branch which allows RF power traveling from port 1 towards the output port 2. The higher the impedance offered by Q_3 and Q_4, the lower the insertion loss.

The reverse saturated topology is obtained by flipping collector and emitter of all the HBTs [6]. Doing so, the impedance offered by Q_3 and Q_4 will increase and the insertion loss will decrease. This is the reason why the reverse saturated configuration has better insertion loss than the forward saturated one. TL3 is included to resonate out devices parasitic capacitances. Besides that, it reduces to zero the collector-emitter DC voltage of the transistors, making them operate in deep saturation region. The characteristic impedance of each transmission line is optimized for both matching and insertion loss. Only the quarter wave transmission line TL1 has 50 Ω



(a)



(b)

Fig. 2: Chip photo of the (a) forward saturated and (b) the reverse saturated SPDTs

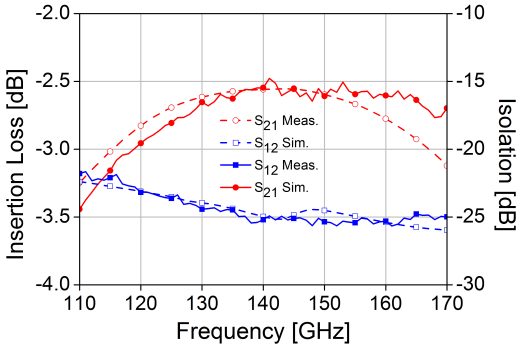
characteristic impedance. These differences can be seen in Fig. 2, which shows the chip photo of the forward and reverse saturated SPDT. Another quarter wave transmission line, called TL5, is used as a RF-choke on the HBT's bases, improving linearity and switching time of the SPDT [4]. Both switches are designed using 7 fingers HBTs. The microstrip transmission lines are realized on the topmost (thickest) metal layer and are modeled by means of electromagnetic simulation.

III. MEASUREMENT AND DISCUSSION

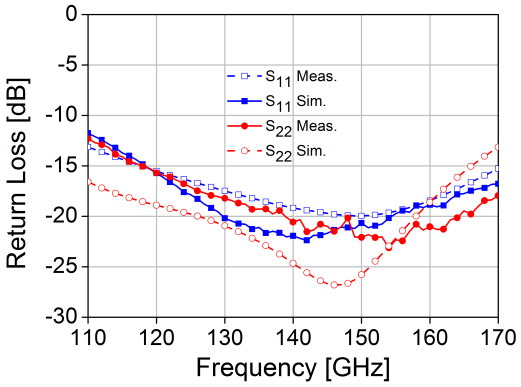
Two variants of D-band SPDT switches are fabricated in IHP SG13SG2 SiGe BiCMOS technology, featuring f_t/f_{max} of 300 GHz / 500 GHz. The control voltages V_C and $\overline{V_C}$ applied to the base terminals of the HBT devices are equal to 0.9 V and 0 V, respectively. Each SPDT dissipates a current of 3.4 mA for a total power consumption of 3.06 mW. The overall size of the forward saturated SPDT is 0.72 x 0.22 mm^2, while the reverse saturated one occupies an area of 0.78 x 0.22 mm^2 pads excluded. Two port s-parameter measurements of the both SPDTs are performed on-wafer while port 3 is terminated with an on-chip 50 Ω resistance.

A. Forward Saturated SPDT

The simulated and measured insertion loss and isolation of the fabricated forward saturated SPDT are shown in Fig. 3(a). The measurement shows a minimum insertion loss of 2.5 dB and insertion loss better than 2.7 dB from 120 GHz to 170 GHz. The measured isolation is greater than 22 dB across the band, with a maximum of 26 dB at 150 GHz. The input and output return losses, presented in Fig. 3(b), are better than 10 dB between 110-170 GHz.



(a)



(b)

Fig. 3: Measured and simulated (a) insertion loss, isolation and (b) return loss of the forward saturated SPDT switch

B. Reverse Saturated SPDT

Fig. 4(a) presents the simulated and measured insertion loss and isolation of the fabricated reverse saturated SPDT. It achieves state of art performance with an insertion loss of 2 dB (including pads losses) at 140 GHz and insertion loss better than 2.3 dB from 120 GHz to 170 GHz. The measured isolation is greater than 21 dB across the band, with a maximum isolation of 26 dB at 147 GHz. The input and output return losses, shown in Fig. 4(b), are better than 10 dB across the whole D-band.

C. Output Ports Isolation

Fig. 5 shows the chip photo of the re-configured forward saturated SPDT which is designed to be able to measure the isolation between output ports, being port 1 connected to an on-chip 50 Ω. Measured and simulated isolation between the output ports are shown in Fig. 6. More than 26 dB isolation across the D-band, with a maximum of 29 dB at 143 GHz, has been measured.

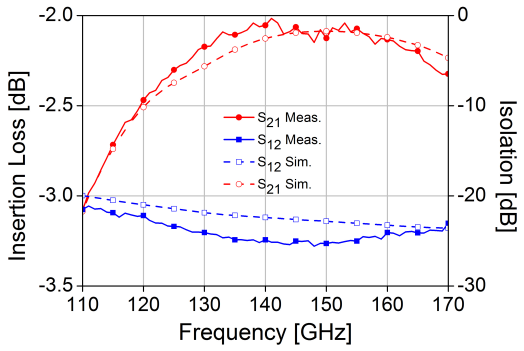
IV. CONCLUSION

Table I shows the performance comparison of the designed forward and reverse saturated SPDT switches with other state-of-the-art D-band switches. The designed double shunt reverse saturated SPDT shows a record minimum

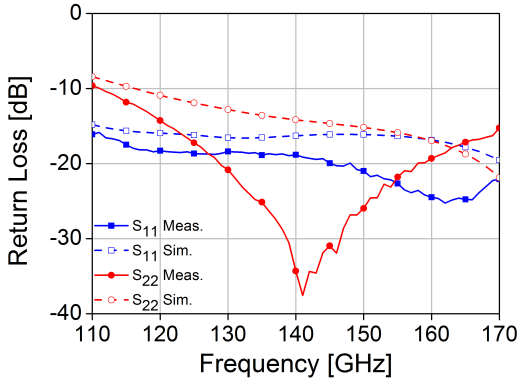
TABLE I: Comparison Table of the D-band SPDTs

Reference	Topology	Technology	Frequency (GHz)	Insertion Loss (dB)	Isolation (dB)	Output Isolation (dB)	Pdc (mW)	P1dB (dBm)	Area (mm^2)
[4]	Double Shunt Forward Saturated	0.13-μm SiGe BiCMOS	110-170	2.6-3.4	23-28	-	6	19*	0.36
[2]	Double Shunt Forward Saturated	32-nm CMOS SOI	110-170	2.6-4	19-21	-	-	-	0.21
[5]	Single Shunt Reverse Saturated	0.13-μm SiGe BiCMOS	110-170	2.6-4.6	26-30	-	5.3	-	0.16**
This Work	Double Shunt Forward Saturated	0.13-μm SiGe BiCMOS	110-170	2.5-3.4	22-26	26-29	3.06	18.6*	0.32
This Work	Double Shunt Reverse Saturated	0.13-μm SiGe BiCMOS	110-170	2.0-3.0	21-26	-	3.06	22*	0.34

*Simulation, ** Excluding the pads



(a)



(b)

Fig. 4: Measured and simulated (a) insertion loss, isolation and (b) return loss of the reverse saturated SPDT switch

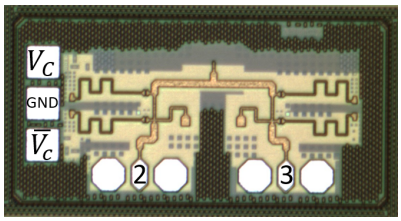


Fig. 5: Chip photo of the forward saturated SPDT used to measure the output ports isolation

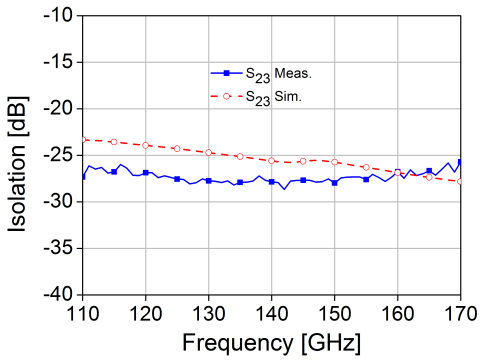


Fig. 6: Measured and simulated output ports isolation

loss of 2 dB, including pads losses, at 140 GHz, along with return losses and isolation in line with the state-of-the-art. Such high performance makes the presented circuit suitable for being used in bidirectional D-band transceivers.

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