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Broadband 110 - 170 GHz True Time Delay Circuit in a 130-nm SiGe BiCMOS Technology

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***Abstract* — This paper presents a fully integrated D-band true time delay (TTD) circuit designed in 0.13 μm silicon-germanium (SiGe) BiCMOS technology. It provides a relative time delay of 0.446 ps to 6.64 ps from 110 to 170 GHz with the resolution of 0.446 ps equivalent to the accuracy of a 4-bit phase shifter. The presented true time delay IC occupies 2.2 mm x 0.53 mm and draws a current of 6.92 mA from 3.3 V. To our knowledge, it is the first true time delay circuit above 100 GHz in silicon technology with a record 3-dB bandwidth of 60 GHz.**

***Keywords* — true time delay, TTD, D-Band, phased array, SiGe BiCMOS, broadband**

I. Introduction

Broad-bandwidth millimeter-wave phased arrays are considered a key solution to perform beam forming and steering for high data rate wireless communication systems. Due to the large bandwidth availability, the D-Band (110 to 170 GHz) is considered as a potential candidate for high capacity back-haul links for 5G and beyond [1][2]. Up to now, there are very few phase shifters reported in D-Band [3] - [6]. They achieved 3-dB bandwidth of 16 GHz [3], 14 GHz [4], 12 GHz [6], and 6 GHz [5], respectively. However, phase shifters traditionally used to steer the beam in phased array systems suffer from beam squinting [7]. This phenomenon, caused by time delay variations within the signal bandwidth, reduces the array resolution since different signal frequencies generate different beam patterns [7][8]. True time delay circuits can be used instead of narrow-band phase shifters thanks to its linear phase shift or, in other words, constant time delay across the signal frequency to avoid such a problem.

In this paper, a true time delay circuit covering the entire D-band is realized in 0.13 μm silicon-germanium (SiGe) BiCMOS technology. The maximum relative delay is 6.64 ps and the resolution 0.446 ps, which is equivalent to 22.5 °. According to the authors' knowledge, this is the first true time delay circuit above 100 GHz in silicon technology with record 3-dB bandwidth from 110 to 170 GHz. Section II describes the design of the TTD in details. Section III compares both simulated and measured results of the TTD performance.

II. Circuit Design

The true time delay IC was designed and fabricated in IHP SG13G2 SiGe BiCMOS technology, featuring f_t/f_{max} of 300 GHz / 500 GHz. The process offers seven metal layers with two top thick metals. Top thick metal layers TM1 and TM2 are used to implement transmission lines with M3 as ground shield. As shown in Fig. 1, a true time delay based phased array generates aligned beam patterns even at different signal frequencies. The true time delay circuit consists of 4 cascaded delay elements as shown in Fig. 2. Each delay element has 2 single pole double throw (SPDT) switches, a reference path and a delay path. Both reference and delay paths of each state are realized using microstrip lines. The difference of delays between two paths sets the relative time delay of each stage. The time delay resolution is set to be 0.446 ps, which is 1/16 period at 140 GHz. The order of the stages is chosen according to better isolation, input and output matching response. By combining the relative delays of each stage, total relative delay from 0 to 15-time resolution can be obtained which covers a phase shift range of 360 degree at 140 GHz. The reverse saturated SPDT switch presented in [9] has been modified and used for each stage of the TTD. Instead of the quarter wave transmission line used as a RF-choke on the HBT's bases in [9], a 3 kΩ resistor has been here introduced, which can provide sufficient RF isolation in a much smaller area. This reverse-saturated SPDT switch shows a record minimum insertion loss of 2 dB at 140 GHz and insertion loss better than 2.3 dB from 120 GHz to 170 GHz.

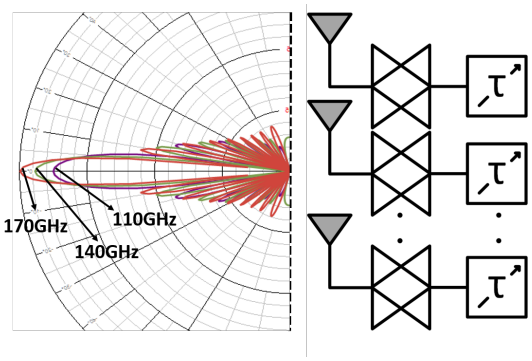

Fig. 1. Beams generated at different signal frequencies by a true time delay based phased array

To provide an impedance of 50 Ω to the TTD ports, SPDT switches' input and output ports are matched to 50 Ω. The reference path of each stage is implemented using a microstrip line with a width of 15 μm in order to realize a characteristic

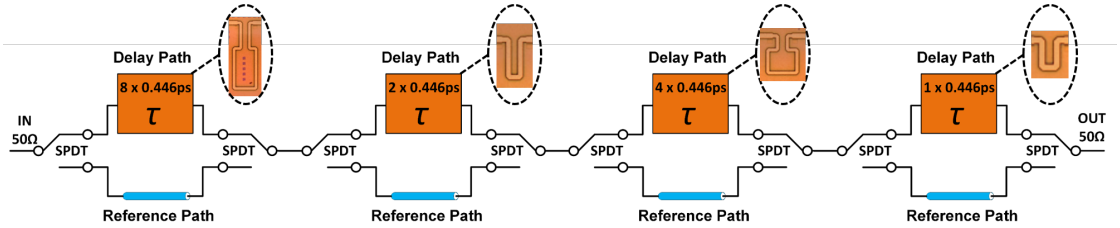

Fig. 2. Architecture of the true time delay circuit

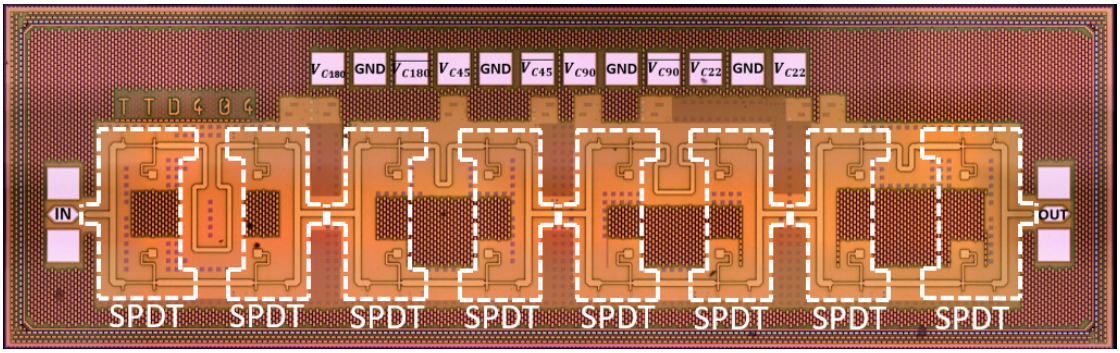

Fig. 3. Chip photo of the fabricated true time delay circuit

impedance of 50 Ω. Delay paths' microstrips are implemented with a characteristic impedance that is slightly higher than 50 Ω in order to minimize the time delay variation across the frequency band by improving the isolation between stages and make shorter transmission lines. The microstrip transmission lines are realized on the top most (thickest) metal layer and are modeled by means of electromagnetic simulation.

III. Measurement and Discussion

The chip photograph of the fabricated TTD is shown in Fig. 3. The IC occupies 2.2 mm x 0.53 mm excluding pads and consumes 6.92 mA. The control voltages V_C and $\overline{V_C}$ applied to the terminals of the HBT devices of the SPDT switches are equal to 0.9 V and 0 V, so that the total power consumption is 6.22 mW. Two port s-parameters measurement is performed on-wafer using D-band extension modules. The simulated and measured insertion losses of the fabricated TTD are shown in Fig. 4.

The measurement shows an average insertion loss of 21.5 dB along the 16 states with record 3-dB bandwidth of 60 GHz. 8-SPDT switches have totally 16 dB insertion loss and 5.5 dB insertion loss is due to delay paths' microstrip lines. The input and output return losses along all states presented in Fig. 5 and Fig. 6 are both better than 10 dB between 110-170 GHz. Fig. 7 presents the simulated and measured phase shift for all states. The measured and simulated relative time delay from 110 GHz to 170 GHz can be seen in Fig. 8. The minimum time delay was designed to be 0.446 ps but measured as 0.519 ps, resulting in a deviation of 12.8 % at 140 GHz. Both root mean square (RMS) values of amplitude and time delay variation for all states are given in Fig. 9. The time delay deviates in

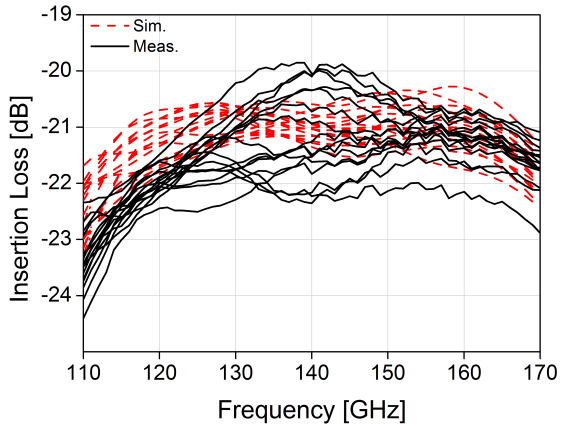

Fig. 4. Measured and simulated insertion loss at the different TTD states

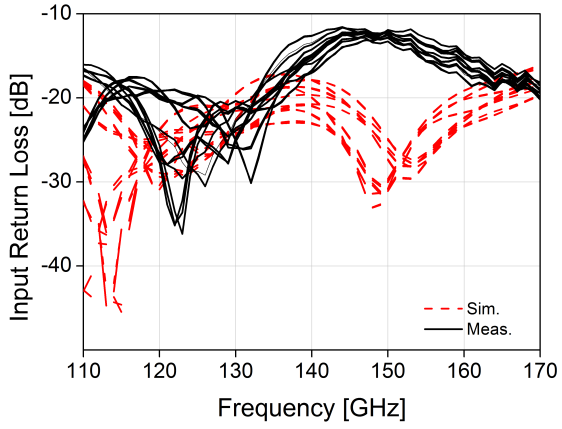

Fig. 5. Measured and simulated input return loss at the different TTD states

Table 1. Performance comparison of published mm-wave integrated true time delay circuits

Reference	Frequency (GHz)	3-dB BW (GHz)	Technology	Maximum Delay (ps)	Resolution (ps)	Gain Variation (dB)	Delay Variation	P_{DC} (mW)	Area (mm^2)
This Work	110-170	60	0.13-μm SiGe	6.64	0.44	1.4	15 %*	6.22	1.16
[10]	31-41	10	0.13-μm SiGe	54	18	N.A	N.A	104	1.44
[11]	15-40	25	0.13-μm CMOS	42	3	2	20 %*	24.6	0.99
[12]	10-50	20	0.25-μm SiGe	32.8	Cont.	1.3	N.A	-	0.22

*Average delay variation across frequency in percentage of resolution

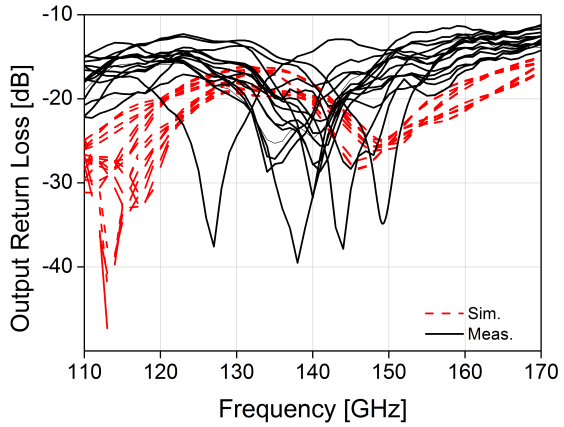

Fig. 6. Measured and simulated output return loss at the different TTD states

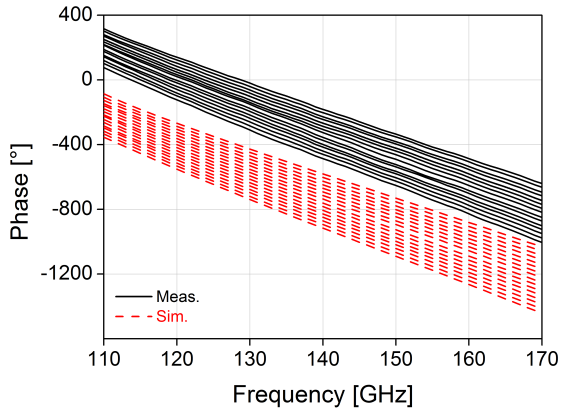

Fig. 7. Simulated and measured phase response of the TTD

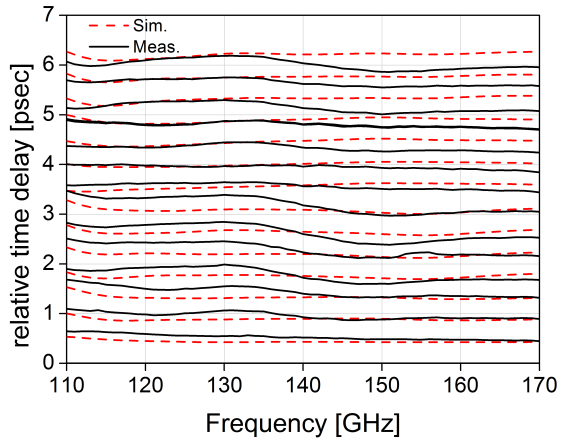

Fig. 8. Simulated and measured relative time delay of the TTD

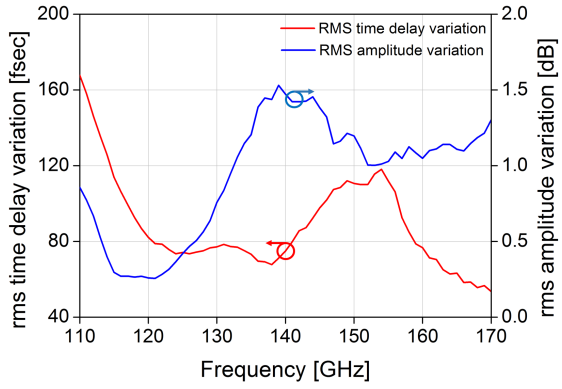

Fig. 9. RMS value of amplitude and time delay variations of the TTD

average 15 % from the ideal resolution value. At the worst case at 110 GHz it deviates 39 % in terms of resolution.

IV. Conclusion

Table I shows the performance comparison of the fabricated TTD with other mm-wave integrated true time delay circuits. The designed TTD covers the entire D-Band and has a record relative bandwidth of 42 %. To our knowledge, this is the first true time delay circuit above 100 GHz in silicon technology. Such high performance makes the presented circuit suitable for being used in D-band phased array systems.

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