Rad-hard Microcontroller with Open Access ISA for Space Applications

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The application field of small satellites develops rapidly over the last years. It is expected that the number of satellites until 2029 will exceed 57000. This opens new perspectives and application possibilities, including replacement of old satellites and more complex processing needs for tasks such as satellite constellation and swarm formation.

For various applications within the satellites the microcontrollers are needed. This includes control domain, with propulsion systems, various robotics applications, motor & mechanisms, DC/DC conversion, or thermal regulation. Another application domain is represented also by scientific instrumentation for control of various sensing devices. Microcontrollers market is already having a number of very good and mature solutions, including products from Cobham Geisler, Atmel, and several US suppliers (Vorago, Texas Instruments).

One trend in general hardware development is the open hardware approach which rapidly started to develop in the last years. One of the major concepts is the use of open access instruction set architectures (ISA), where the main example is the rapid growth of RISC-V approaches. This trend requires also changes in the space domain.

This development is part of the EU project MORAL, targeting development of microcontroller IC with a 130nm standard CMOS technology, and corresponding development software. MORAL approach exactly addresses this need with the target to develop a completely European, ITAR-free µcontroller for space applications. MORAL approach is based on the novel PEAKTOP architecture (incl. novel open access ISA), and includes formally-verified C-compiler, RTOS and toolchain, and corresponding demonstrator board.

The microcontroller contains, in addition to the regular execution pipeline, also floating-point unit, memory protection unit, as well as DSP support. The integrated SRAM, based on rad-hard ELT transistors and extended with ECC for SEU correction, should support initially 256 KB, with the perspective of further memory space increase. The microcontroller includes a number of interfaces relevant for space applications, including CAN, UART, SPI, SpaceWire, I2C, MIL-STD-1553 etc. It is important to emphasize also the integration of rad-hard A/D and D/A converters with 12-bit

resolution. The former is a SAR-based ADC, while the latter is a resistor-string DAC. The schematic of MORAL design is provided in the attached figure.

The key aspect of MORAL development is the radiation hardening methodology which is consequently implemented at different abstraction layers. Concerning the analog IPs, the hardening has been achieved acting on architecture, circuit and layout sides. For the DAC, the choice of a topology based on poly-resistors (insensitive to radiation) is coupled with proper MOS sizing. Extended use of ELT shapes and guard-rings are common to both. For the ADC, MIM capacitances (insensitive to radiation) and over-design have been adopted. Moreover, digital control section serving analog functions is implemented with proven rad-hard digital library.

At the level of complex digital sequential cells, the TMR (triple modular redundancy) methodology has been applied for filtering SEUs while timing filters address SETs. SETs in control logic are addressed by specific combinational cells, pre-tested for SET sensitivity. SET mitigation is achieved either at circuit level (reducing the number of p-channel and n-channel transistors not directly connected to power supply and ground) and layout level (making leverage on enhanced guard rings also used for SEL mitigation). Extensive use of ELT geometry guarantees TID resiliency well over 100 Krad (Si) making the final SoC suitable for the major part of LEO and GEO missions. At system level, the error accumulation is addressed by use of error correcting codes and scrubbing in memory.

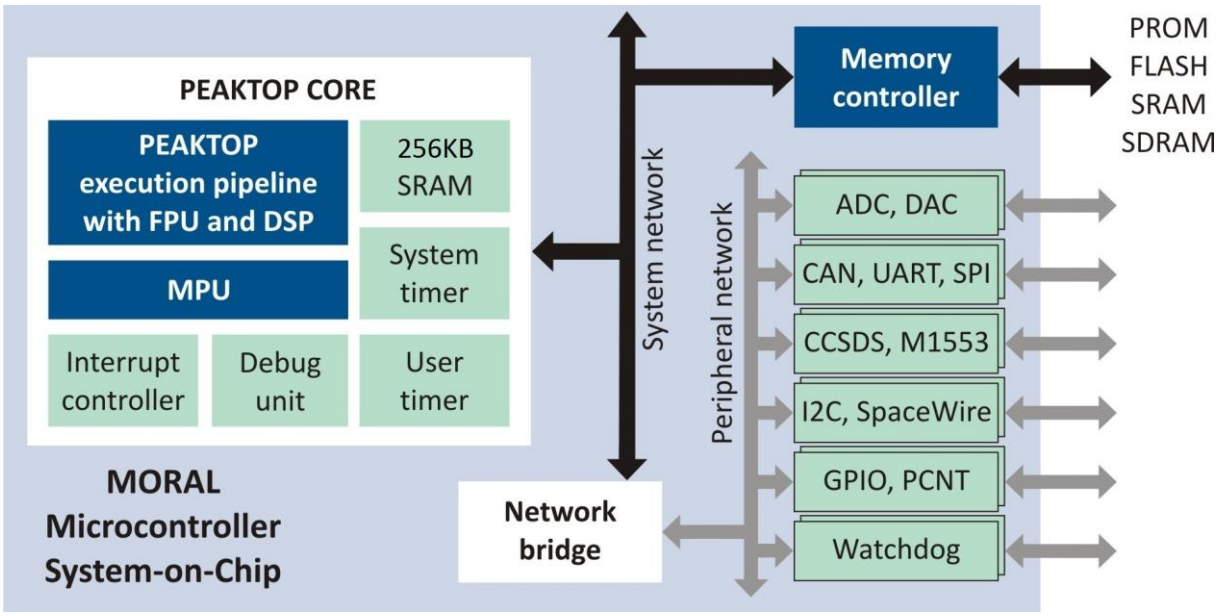
The project started in 2020, and until now significant developments have been performed. The complete RTL processor core has been developed and verified in extensive simulations. The complete RTL platform is also mapped to an FPGA, which is used for co-verification. As for the analog IPs, the DAC have been successfully characterized in lab operation environment. The final integration and back-end design is ongoing. The target process is SG13RH technology from IHP, that is currently under ESA evaluation. The technology has been commercially qualified and used in many products, and radiation hardness features have been verified within successfully finished DLR project. Based on such background we are aiming for 100 Krad (Si) TID hardness, as well as to be SEL-free up to at least 60 MeV·cm2/mg (Si) and with SEU sensitivity > 30 MeV·cm2/mg (Si).

At the software side, CompCert, a formally verified C compiler, was successfully ported to the PEAKTOP architecture. Through its formal verification, CompCert is free of miscompilation and allows the use of code optimizations, even for safety- and mission-critical applications. This ensures the effective use of limited hardware resources. Furthermore, formal verification of software is a major advantage over typical proven-in-use arguments, which are not applicable if the target audience is not a mass-market.

Serving as an operating system, a new separation kernel has been developed to run on the PEAKTOP CPU. The challenging frame conditions, and strong security and safety standards, are combined with an extremely small footprint, to match the embedded memory limitations.

After successful production the produced IC will be functionally verified, but also initial reliability tests will be performed. In parallel we are working on the demonstration board which will include also application demonstration.

PEAKTOP microcontroller platform introduces novel ISA concept and aims to result in competitive mixed-signal solution for space applications. The advanced development stage of digital & analog IPs, as well as system software, provide us with great confidence for successful exploitation of final project results.


PEAKTOP CORE
PEAKTOP execution pipeline with FPU and DSP
256KB SRAM
MPU
System timer
Interrupt controller
Debug unit
User timer
MORAL Microcontroller System-on-Chip
System network
Memory controller
PROM
FLASH
SRAM
SDRAM
Peripheral network
ADC, DAC
CAN, UART, SPI
CCSDS, M1553
I2C, SpaceWire
GPIO, PCNT
Watchdog
Network bridge