

# Wafer edge planarization after wafer bonding

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## INTRODUCTION

In order to reduce the chipping at the wafer edge of the bonded and thinned (by grinding) wafer due to following process steps involved in the fabrication, the wafer is trimmed at its edge. The resulting step at the wafer edge of the bonded wafers was to be planarized for the subsequent standard preparation.

## BACKGROUND

This work shows how the step height at the wafer edge can be planarized. A 200 nm silicon nitride was deposited as a polishing stop layer. Silicon dioxide with a thickness of 4500 nm was deposited before the planarization which serves as a filling layer for the wafer edge. It was then polished with a silica slurry with a polishing pressure of 0 psi at the edge zone of the polishing head. The other polishing pressure zones were set at about 5 psi. The final polish, with a stop on the SiN layer, was carried out with a highly selective ceria slurry (CeO<sub>2</sub>-slurry) with the same polishing pressure distribution.

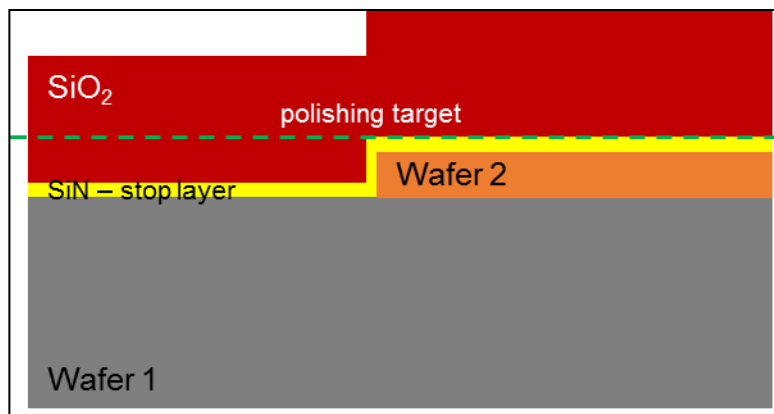


Fig. 1 Schematic of the edge of the bonded wafers

## EXPERIMENTAL

A Mirra Mesa with contour heads from AMAT was used as the polishing tool. The contour head has 5 independent polishing zones to can control the wafer homogeneity (Fig. 2). To planarize the wafer edge a special polishing recipe without pressure in zone 1 was created. This recipe was used to planarize the overfilled structures in the wafer layout and the wafer edge at the same time.

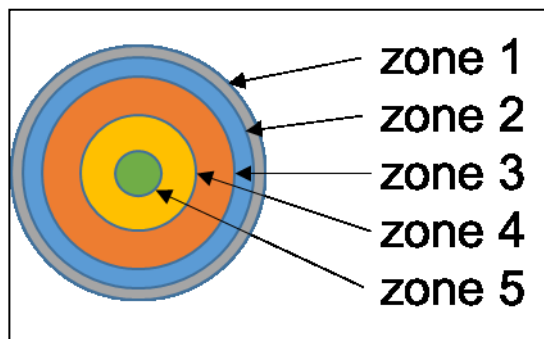


Fig. 2 Schematic of the pressure zones on the contour head

An HRP-250 from Tencor was used to measure the profile. The slurries, SS12 from Cabot and the CES-333F-2.5 from AGC were used.

Before the wafers were bonded (oxide to oxide and face to face), the edge of the top wafer was trimmed (10 mm) and a new bevel was polished at the same time. This prevents the wafer edges from breaking out after grinding/thinning [1]. After bonding the wafers, the bulk silicon is grinded down to approx. 20  $\mu\text{m}$ . After that, the remaining silicon of the bonded wafer was removed up to the buried oxide layer (BOX) of the silicon-on-insulator (SOI) -substrate by reactive ion etching (RIE). Another RIE process removes the 2  $\mu\text{m}$  of BOX. Thereafter the step height at the wafer edge of the bonded wafers is 3  $\mu\text{m}$ . A PE nitride layer of 200 nm is deposited subsequently and the layer is structured by using photolithography and RIE steps. Further, the SiN is used as a hardmask to pattern the Si-layer of the bonded wafer. The remaining step at the wafer edge of the device to the carrier wafer has to be planarized for further standard processing. For this purpose, the remaining SiN hard mask (approximately 180 nm) is utilized as a polishing stop layer. Before planarization, a 4500 nm of PE-TEOS layer was deposited on the SiN. This serves to fill the edge of the wafer. In the first polishing method, the oxide is polished to a residual thickness of approx. 500 nm over SiN with SS12 slurry. Here, the polishing is carried out without pressure on the edge of the wafer. Then the wafers were polished with CeO<sub>2</sub> slurry down to SiN. The oxide removal with the CeO<sub>2</sub> slurry is highly selective to SiN and the polishing is stopped on the SiN-layer. The first polishing method takes too long to polish the oxide layers to 500 nm target thickness. Further, after polishing SiO<sub>2</sub> until the stop layer, the SiN was slightly polished with SS12. Finally, the highly selective CeO<sub>2</sub>-slurry is used for polishing SiN. The results show that the step height is good but the SiN-wafer range was very high (wafer #1). The second method with less polishing time and stop on SiO<sub>2</sub> at 500 nm over SiN & the final polishing with the CeO<sub>2</sub>-slurry up to SiN show good step height with a better SiN wafer range (wafer #2).

## DISCUSSION

The step height at the wafer edge could be reduced from 3  $\mu\text{m}$  (Fig. 3 (a)) to approx. 0.1  $\mu\text{m}$  (Fig. 3 (b)).

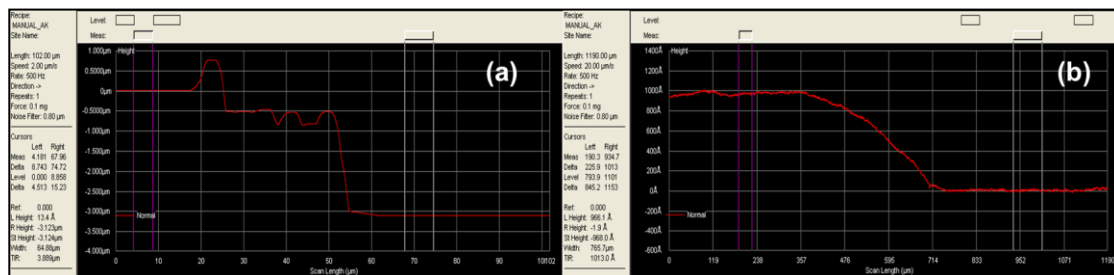


Fig. 3 Step height at wafer edge (a) before & (b) after cmp

A two-step polishing process was used. Before starting the 1<sup>st</sup> polishing the oxide thickness of wafer #2 was 4474 nm and the wafer range was 134 nm. The wafer was polished for 485 s with a special polishing recipe consisting of 0 psi zone 1 pressure on the contour head. The oxide thickness reduced to 546 nm and the wafer range was 270 nm. After the 2<sup>nd</sup> polishing with the ceria slurry for 120 s, the oxide thickness was 0 nm and the SiN thickness was 185 nm. The wafer range was 3 nm. The oxide thickness of wafer #1 before starting the 1<sup>st</sup> polishing was 4515 nm and the wafer range was 151 nm. After the 1<sup>st</sup> polishing with 589 s polishing time the oxide thickness was 3.5 nm and the wafer range was 30 nm. The SiN value after the 1<sup>st</sup> step of oxide polishing was 116 nm and the wafer range was 164 nm. This shows that the 1<sup>st</sup> polishing time was too high. Polishing only with SS12 slurry up to the SiN layer produce large wafer range for the following processes. To get information about the ability of the ceria slurry we tried the 2<sup>nd</sup> polishing step with CES333 on these over polished wafer. But the range in the SiN layer was not improved.

The loss of the SiN stop layer (wafer #2) was only a few nanometers. The wafer range of this SiN layer was 3 nm. A microscope picture of the whole wafer shows the excellent uniformity of the

SiN layer (Fig. 4 (b)). The picture of the overpolished wafer shows the inhomogeneity of the SiN layer because of long polishing time in the 1<sup>st</sup> polishing step (Fig. 4 (a)).

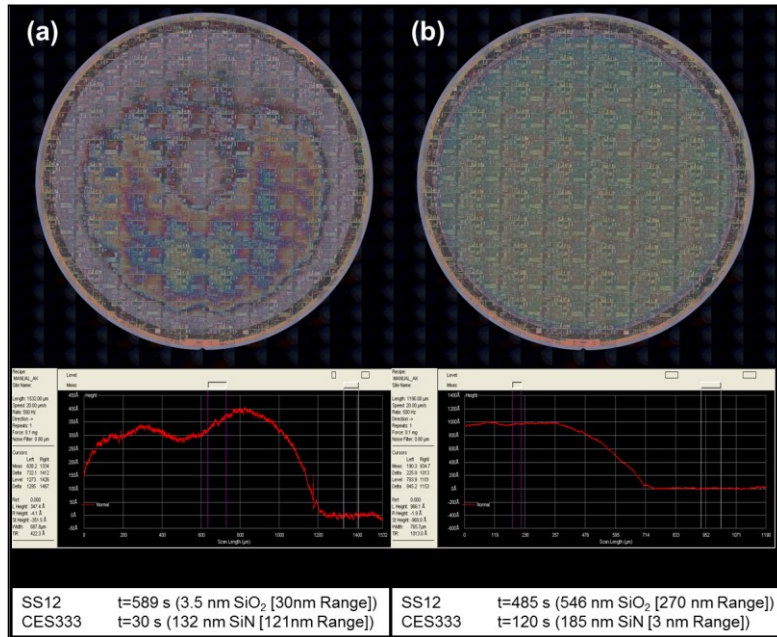


Fig. 4 Images from wafers and step height after 2<sup>nd</sup> CMP step (a) wafer #1 overpolished in 1<sup>st</sup> polishing step & (b) wafer #2 with reduced polishing time in 1<sup>st</sup> polishing step

## CONCLUSIONS

It has been shown that the step height at the wafer edge could be reduced. At the same time, the wafer range of the SiN stop layer can remain small if a highly selective slurry such as the CES333F from AGC is used. It is important not to polish too close to the SiN layer during the first polish with the SS12 slurry, which is less selective to SiN. Otherwise, due to an uneven SiO<sub>2</sub> removal, the SiN is already partially reached and removed, while other areas of the wafer surface still have some thickness of the SiO<sub>2</sub> layer left on SiN. This creates a high wafer range. However, the step height at the wafer edge of the bonded wafer could be reduced to less than 100 nm in both variants. In order to achieve a further reduction in the step height, a longer polishing time would have to be chosen, which, however, requires a thicker deposition of the oxide.

[1] Matthias Wietstruck et al 2017 ECS Trans. 80 135

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