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Flip-Flop SEUs Mitigation Through Partial Hardening of Internal Latch and Adjustment of Clock Duty Cycle

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***Abstract*— A radiation-hardness-by-design (RHBD) method for flip-flop single-event upsets (SEUs) mitigation is studied in this paper. This method applies a certain radiation hardened structure, e.g., the dual-interlocked storage cell (DICE), to implement one stage latch of a flip-flop while the SEUs protection for the other stage is realized by adjusting the clock duty cycle to shorten its hold state duration. Since the radiation hardening technique is used for only one stage latch, the overall area and power costs can be lowered. This technique is compatible with the automatic digital design flow and was implemented for an asynchronous first-in-first-out (FIFO) circuit as a case study in this paper.**

Keywords—flip-flop; partial hardening; soft-error

I. INTRODUCTION

Single-event upsets (SEUs) in flip-flops play a critical role in determining the overall soft-error rate (SER) of microelectronic circuits [1]. To mitigate the flip-flop SEUs, many radiation-hardness-by-design (RHBD) methods, either at the system-level (e.g., triple modular redundancy or TMR [2]) or at the circuit-level (such as the dual-interlocked storage cell or DICE [3]), have been developed. In design practices, a chosen RHBD technique would normally be applied for both the master and slave latches of flip-flops [4]. The rationale behind is that, the master and slave latches will stay in the hold state and be sensitive to SEUs in turn, therefore enabling SEUs hardening for both of them can promise the radiation resistance for the whole flip-flop. However, this design style can introduce obvious area and power penalties which may limit the applications of certain hardening methods.

In this paper, we propose an RHBD approach to address the flip-flop SEU issue through applying a certain hardening technique for only the master or slave latch while the other radiation-soft latch's SEUs sensitivity is lowered by shortening its hold state duration through adjusting the clock duty cycle. With the proposed methodology, the overall area and power costs can be lowered, because the redundancy based hardening technique is applied for only one stage latch. The rest of this paper is organized as follows. Section II provides a review of the SEU hardening methods. Section III details the principle of the proposed method. Section IV provides the design cost comparison among the proposed and other hardening solutions. Section V gives a case study of the implementation of this method by taking a first-in-first-out (FIFO) module as the example circuit. Design constraints posed by this method are discussed in Section VI. This paper is concluded in Section VII.

II. PREVIOUS WORK

The mitigation of SEUs can be realized at different levels. The selection of a hardening method reflects at what abstract level a designer is considering a single-event.

At the physical level, the fundamental processes of the generation and diffusion of single-event charge are considered. To minimize those effects, designers may choose to use guard drains (reverse-biased junctions placed in the substrates and wells) to help absorb the charge [5] and guard rings (substrate and well contacts) to stabilize the substrate/well potential to suppress the bipolar amplifying [6]. As technology scales, charge sharing effect induced multi-node upsets become critical [7]. Although charge sharing is considered as a threat because it can make many traditional SEUs hardening methods ineffective, recent researches revealed that, by properly arranging the placements of devices and enhancing their charge sharing, the overall single-event effects on circuits can be minimized [8]. This concept has been developed into a technique called LEAP (Layout design through Error-Aware transistor Positioning), and the very good hardening performance of this technique has been proven experimentally [8], [9].

At the circuit level, designers may simply the consideration for a single-event and only model it as a voltage pulse resulting from a current injection. Special circuit topologies can be employed to prevent the propagation of a single-event voltage pulse occurred at any internal node. A classic example of this category of methods is DICE [3]. Normally, designers would prefer structures with infinite critical charge amount for each node. If this infinite critical charge requirement can be met, a structure is considered as single-node upsets immune, and the way of modeling a single-event current is actually not very important in the fault injection simulations to validate such a structure. However, this is not always the case. Recently,

another circuit named Quatro was proposed [10], and it showed better hardening performance than DICE in 40 nm [11], [12]. Interestingly, Quatro is not fully immune to single-node upsets [10]. Therefore, more accurate single-event current modeling is needed to measure its nodal critical charge, which is important for understanding its radiation hardening ability. As mentioned above, charge sharing is also important for nanoscale circuits. Multi-node upset tolerant circuit structures can also be options, but they would need more transistors to implement, which could be undesirable.

At the system level, SEUs can only be seen as bit flips. At this level, the main metric of a method's hardening ability may be how many bit flips it can correct. This is frequently considered when one needs to choose a proper error correction code (ECC) for a memory array. For logic circuits, some special schemes have been developed for some specific architectures, for example, a rollback recovery structure [13] and an improved one-hot coding method [14] have been proposed for the SEUs hardening of finite state machines. For the broader range of digital circuits, TMR can be a universal solution to address the soft errors issues.

It should be noted that different categories of hardening methods would have different benefits and drawbacks. The physical level methods can address the radiation effects at the very source. Because they require little resource redundancies, the performance, area, and power costs induced by them can be less. This is preferable when design costs are of critical concern in some projects. Circuit level hardening methods would need more complicated structures implemented with more transistors to enable radiation hardening for single sequential cells. Obviously they can induce area and power penalties, and sometimes performance can also be lowered compared to unhardened designs. Another part of costs of these methods is introduced by their validations. The concepts of hardening at the physical and circuit levels have to be experimentally verified before integrating them into any real designs. On the other hand, the verifications of system level hardening methods might be more straightforward, since they could have clearer principles. Another benefit of system level methods is that their implementation can be compatible with the automatic digital design flow, which enables high design efficiency [15]. However, the system level hardening would require higher costs for implementation (e.g., 3× areas of TMRs), and this might make them less attractive in some cases.

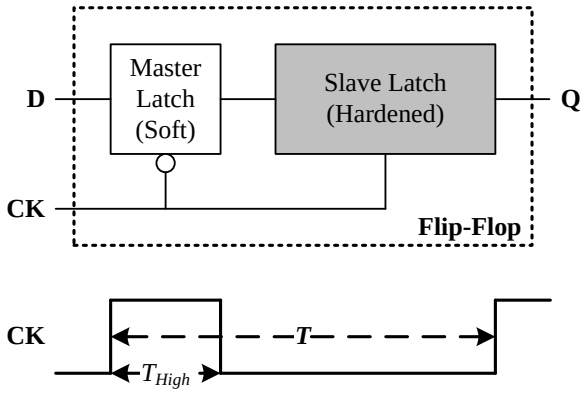

Fig. 1. Conceptual diagram of the proposed scheme.

One reason of the high costs of digital circuits' system level hardening methods is that they are usually based on relatively big granularities – flip-flops. This granularity limits the space for further optimizations. In this paper, we study a new hardening method that works on the reorganizations of latches rather than flip-flops. Because the granularity is shrunk, more optimizations can be enabled, and the high design efficiency can still be kept.

III. Proposed Scheme

The proposed hardening scheme is based on a basic concept that a latch is only SEUs sensitive in the hold state. For a transparent latch, the radiation charge deposition can only induce single-event transients (SETs) at certain nodes but will not lead to bit flips. These SETs would not be issues unless the circuit is operated with a high frequency [16], [17]. However, for hold state latches, their internal feedbacks can easily turn any short SETs into SEUs, and the resulting SER is virtually independent from the clock frequency [16], [17].

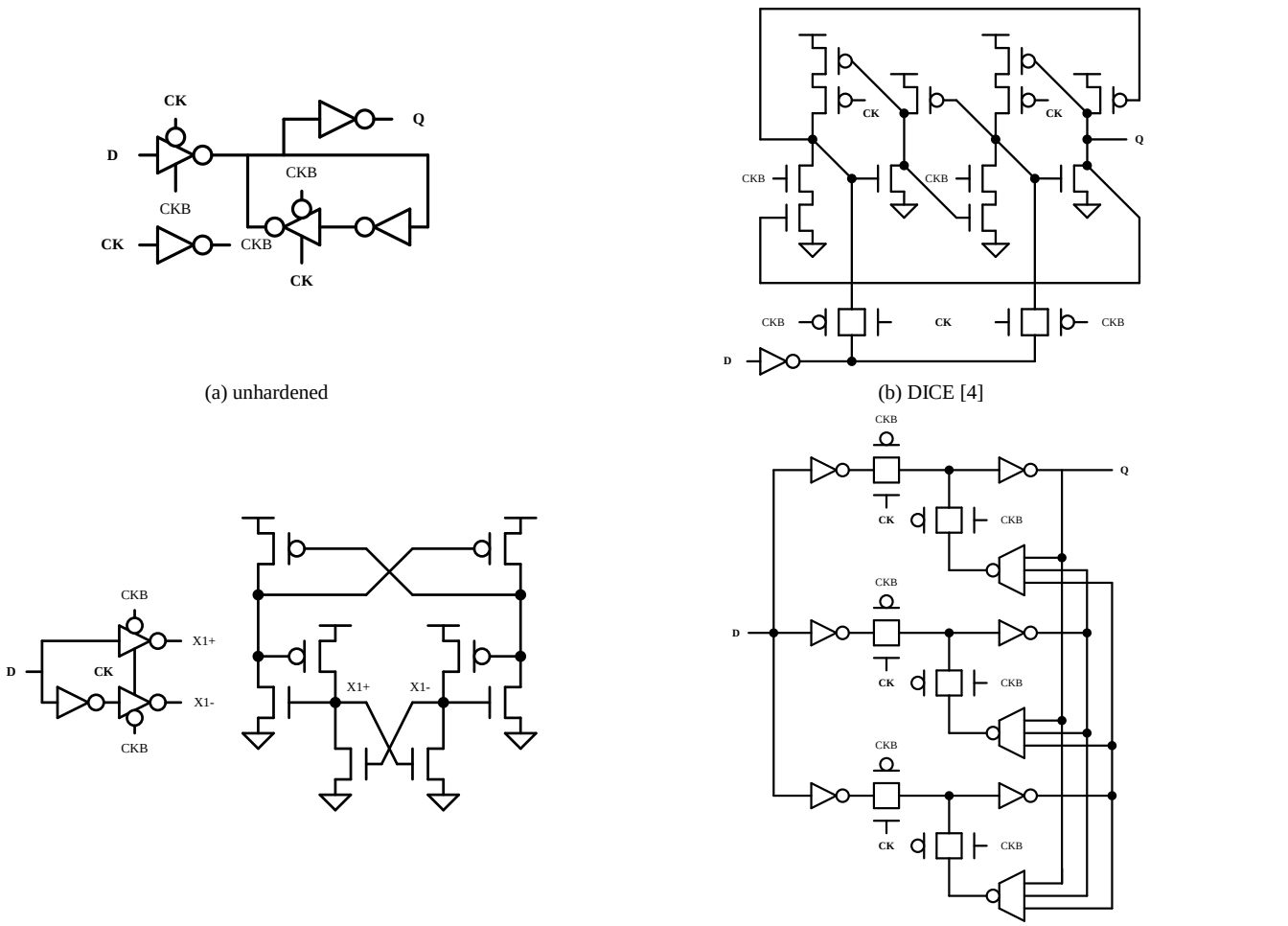

Fig. 2. (a) Unhardened, (b) DICE, (c) Quatro, and (d) TMR latches.

The above analysis indicates that one can improve a flip-flop's SEUs resistance through: 1) applying a certain RHBD structure, e.g., DICE [3], Quatro [10], or TMR [2], for a single stage latch inside the flip-flop while the protection performance of this part would not vary with different frequencies, and 2) adjusting the clock duty cycle to shorten the hold state duration of the other unhardened latch. As shown in Fig. 1, we assume that the slave latch of a flip-flop is hardened by employing a certain hardening structure and the master latch is left radiation soft. The clock period is T and the high duration (the master latch is in the hold state) of the clock waveform is T_{High}. For a specified radiation environment, if the hardened and soft latch structures have the SERs (cross sections, Failure-in-Times, etc.) of SER_{Hard} and SER_{Soft}, respectively, then the overall SER of the flip-flop, SER_{FF}, can be calculated according to (1).

$$SER_{FF} = \frac{T_{High}}{T} \times SER_{Soft} + \frac{T - T_{High}}{T} \times SER_{\text{Hard}} \quad (1)$$

In (1), due to the first term, the SER_{FF} cannot be as low as SER_{Hard}. However, by properly adjusting the duty cycle, we can still achieve an acceptable SER_{FF}, for example, only 10% higher than SER_{Hard}. To illustrate this, some previously reported SER results of various RHBD structures are applied to calculate the required duty cycles to obtain the $SER_{FF} = 1.1\times SER_{Hard}$. The calculation results are summarized in Table I. As listed in this table, for hardened structures that can provide significant SER reduction compared to the unhardened designs (e.g., cases 1 and 5), very small duty cycles would be required to meet the $SER_{FF} = 1.1\times SER_{Hard}$ requirement. This is because the hold state duration of the unhardened latches needs to be shortened significantly to elevate their equivalent hardening performance to the similar levels of the hardened ones. In these cases, applying the duty cycles presented in Table I may be not very necessary. Actually, for cases 1 and 5, around 9.8% and 9.1% duty cycles can lower the SER_{FF} to 10% of SER_{Soft}, respectively, which represent one order of magnitude SER reduction.

TABLE I
DUTY CYCLE CALCULATION RESULTS FOR RHBD DESIGNS

Case	Ref.	radiation type	SER_{Soft}	RHBD structure	SER_{Hard}	Duty cycle
1	[8]	Proton	1	DICE	1.94×10^{-3}	2×10^{-2}%
2	[18]	Neutron	1	RST*	0.33	5%
3	[11]	Neutron	1	DICE	0.68	21%
4	[11]	Neutron	1	Quatro	0.3	4%
5	[11]	Alpha	1	Quatro	0.01	0.1%

*RST = Robust Schmitt Trigger

IV. Design Costs Estimation

We select three well-known RHBD latch structures, DICE [4], Quatro [12], and TMR [4], and compare the design costs among flip-flops using them for full and partial hardening. The schematics of these latches, as well as the unhardened one, are illustrated in Fig. 2. As shown in Fig. 2 (a), the inverter used to generate the CKB (inverted CK) signal is included in the unhardened latch while absent in other hardened structures. We assume that the unhardened latch in Fig. 2 (a) would be used as the master latch and this clock inverter is shared between the master and slave latches. The total transistor count and clocked transistor count of different designs are summarized in Table II.

TABLE II
Design Costs Estimation

Design type	Total transistor #	Clocked transistor #
Unhardened flip-flop	26	10
DICE flip-flop	38	18
Quatro flip-flop	36	10
TMR flip-flop	122	26
Unhardened (master) + DICE (slave)	32	14
Unhardened (master) + Quatro (slave)	32	10
Unhardened (master) + TMR (slave)	74	18

As listed in Table II, once the proposed scheme is applied, for each RHBD solution, the required total transistor amount can be reduced, which can lead to smaller areas and lower power consumption. For flip-flops, another important performance metric is the number of clocked transistors, since these transistors will switch all the time regardless of the input data pattern and act as major sources of power. With the proposed scheme, since RHBD structures are only used for single stage latches, the numbers of clocked transistors can also be reduced. One exception is the Unhardened (master) + Quatro (slave) case. This design style uses 10 clock transistors as its Quatro flip-flop counterpart. This is because the slave Quatro cell, as shown in Fig. 2 (c), also has 4 clock transistors, which is the same as the unhardened one in Fig. 2 (a).

V. Implementation

The implementation of the proposed method can be realized in two ways:

1) Flip-flops with one stage latch hardened and another soft can be designed through the custom-design process. One can choose any hardening structure, e.g., DICE [3] and Quatro [7], to form the hardened stage. To enable high design efficiency, these flip-flops need to be later integrated into a standard cell library through timing characterization and physical design information extraction.

2) One can also implement the proposed scheme by utilizing proper latches only. In this way, the implementation flow will switch from flip-flop based to latch based. Unhardened and hardened latches can be used to construct flip-flops if the hardened ones are available in the standard cell library. If only regular latches are available, the hardening of one stage latches in the flip-flops can be realized by choosing a system level SEUs mitigation method like TMR. The implementation process can be compatible with the automatic digital design flow.

The benefit of the first option is that designers can have full control over the design process. Thus, flip-flop performance can be optimized by careful designing. However, radiation tests on the custom-designed cell would be required before it can be applied in any projects, especially those targeting extreme radiation environments. This may induce additional costs and increase the time to application. The second option can be more straightforward without any extra custom-design work.

In this paper, we illustrate the second implementation solution above. The example circuit chosen is an asynchronous FIFO module derived from [19]. The functional diagram of this FIFO is given in Fig. 3. The depth and width of this FIFO were configured to be 300 and 8. Within this FIFO, the write/read pointer generators, synchronizers, and memory array contain sequential elements.

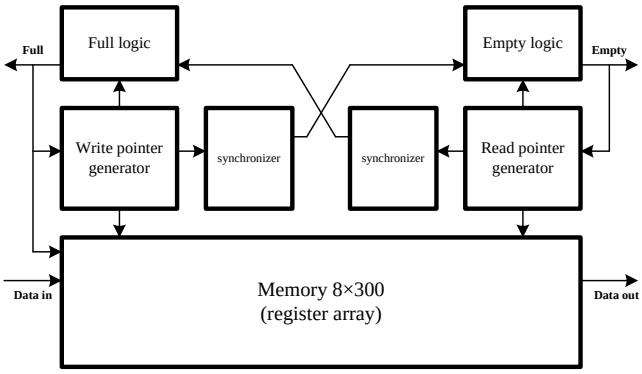

Fig.3. An asynchronous FIFO (derived from [19]).

A radiation hardened standard cell library was used to implement this FIFO circuit. This library includes regular and radiation hardened flip-flops and latches. This FIFO was implemented by using 1) regular flip-flops, 2) hardened flip-flops, and 3) the proposed scheme (soft master latch and hardened slave latch) in different synthesis runs. The synthesis area results are shown in Table III. The total gate areas of clocked transistors are also given in this table. Compared to the hardened flip-flop based solution, the proposed scheme reached 5.9 % reduction for area and 18.9 % reduction for the total gate area of clocked transistors. The latter one can lead to the decrease of clock switching related power consumption. The physical implementation of the FIFO module hardened through the proposed scheme is shown in Fig. 4.

TABLE III
DESIGN COST COMPARISON

	Unhardened FFs	Hardened FFs	Proposed
Area	1	2.32	2.18
Gate area of clocked transistors	1	4.74	3.84

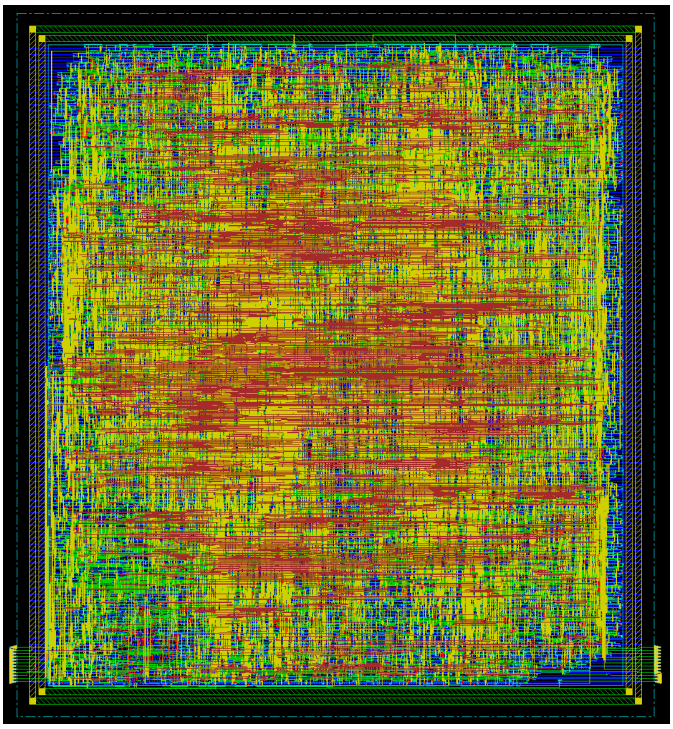

Fig. 4. Physical implementation of the proposed scheme applied on an FIFO.

VI. DESIGN CONSIDERATIONS

One design constraint posed by the proposed method may be the delays of clock inverters and buffers. With a smaller duty cycle, designers need to ensure that the relatively short clock pulses can still propagate through the clock tree without attenuation. To achieve this, static timing analysis (STA) should be performed to measure the delay of each single clock inverter/buffer, and the minimum clock pulse width should be at least 2.5 times of the maximum cell delay [20]. This issue should be less critical when the target frequency is relatively low. For the FIFO design in Fig. 4, the highest target frequencies for the write and read clocks are both 66.7 MHz (period $\leq$ 15 ns). The STA results showed that the maximum insertion delays (the sum of delays of all inverters/buffers of a clock propagation path) for both the write and read clocks were shorter than 1.5 ns. Therefore, 10% duty cycles can be safely applied for these two clocks, which will result in one order of magnitude sequential SER reduction if the hardened latches can be virtually immune to SEUs in certain radiation environments.

It should also be noted that the proposed method is only for SEUs mitigation and may still be sensitive to input SETs arisen in combinational logics. To further enable SETs protection, certain temporal hardening techniques, e.g., the pulse filtering circuits based on TMR [21] and guard-gate [22], can be employed.

VII. CONCLUSIONS

In this paper, we have proposed an RHBD method to mitigate the SEUs in flip-flops. This method realizes the hardening by applying a certain hardened structure for only one stage latch inside a flip-flop and adjusting the clock duty cycle to shorten the SEU sensitive duration of the other stage. Design costs estimation shows that this method can reduce the required transistor number to implement a flip-flop and also the number of clock transistors. This property can reduce the area and power (both data activity and clock switching related) costs. The applicability of this method is evaluated on an example FIFO circuit based on a radiation hardened standard cell library.

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