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1. Extended Data

Figure # 	Figure title One sentence only	Filename This should be the name the file is saved as when it is uploaded to our system. Please include the file extension. i.e.: *Smith_ED_Fig1.jpg*	Figure Legend If you are citing a reference for the first time in these legends, please include all new references in the main text Methods References section, and carry on the numbering from the main References section of the paper. If your paper does not have a Methods section, include all new references at the end of the main Reference list.
Extended Data Fig. 1	Simplified interface between electronic output stage and plasmonic Mach-Zehnder modulator (MZM).	Koch_ED_Fig1_TML.tif	Typically, both output stage and modulator are terminated by 50 Ω. In our case, the plasmonic MZM can be modelled as electrically lumped, which allows for single-end termination. Hence, the driving voltage is doubled without increase in energy consumption. Additionally, such an approach allows tuning of the output impedance to specific needs.
Extended Data Fig. 2	Active area and power consumption per circuit part.	Koch_ED_Fig2_PowerArea.tif	The operation-critical functions (2:1 SEL and clock distribution) are separated from the optional parts for advanced functionalities and for measurement purposes.
Extended Data Fig. 3	Temperature map of monolithic transmitter.	Koch_ED_Fig3_Temperature.tif	Thermal simulations of the electronic circuit revealed the temperatures listed in the table inset, which have been compared to measurements with on-chip temperature diodes. Ideal and reduced thermal conduction to the substrate match well with measurements on a raw electronic chip and a post-processed transmitter chip, respectively.
Extended Data Fig. 4	Temperature stability of the nonlinear organic	Koch_ED_Fig4_OEO.tif	Stable operation until about 140°C was measured with a drastic degradation when reaching the glass temperature of

	electro-optic material.		150°C. The small dip at 120°C is due to thermally induced setup fluctuations. The trend line (dashed) serves to guide the eye.
Extended Data Fig. 5	Data modulation experiment for externally driven monolithic plasmonic modulator.	Koch_ED_Fig5_DataExternalDrive.tif	An amplified external source applies the electrical signal to the modulator. 100 GBd NRZ-OOK has been modulated and transmitted to the receiver for direct detection. The insets show the received optical eye after equalization.

6 # A monolithic bipolar CMOS electronic–
7 # plasmonic high-speed transmitter

8

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24

25 ## *ABSTRACT*

26 In order to address the challenge of increasing data rates, next generation optical communication networks will

27 require the co-integration of electronics and photonics. Heterogeneous integration of these technologies has

shown promise, but will eventually become bandwidth limited. Faster monolithic approaches will, therefore, be needed, but monolithic approaches using complementary metal–oxide–semiconductor (CMOS) electronics and silicon photonics are typically limited by their underlying electronic or photonic technologies. Here, we report a monolithically integrated electro-optical transmitter that can achieve symbol rates beyond 100 GBd. Our approach combines advanced bipolar CMOS with silicon plasmonics, and addresses key challenges in monolithic integration through the co-design of the electronic and plasmonic layers, including thermal design, packaging, and a nonlinear organic electro-optic material. To illustrate the potential of our technology, we develop two modulator concepts — an ultra-compact plasmonic modulator and a silicon-plasmonic modulator with photonic routing — both directly processed onto the bipolar CMOS electronics.

Future communications systems will require the co-integration of electronic and photonic systems. A key example is optical transmitters: electro-optical devices that convert electrical information to the optical domain for signal transmission. Such devices should currently offer dozens of Gb/s of data speed on a compact footprint, while being cost- and energy-efficient[1]. However, data centres and computing infrastructures will shortly require Tb/s data

51 rates in a single optical link[2,3]. This calls for parallelization and high line data rates, and to achieve such data rates,
52 the co-integration of high-speed electronics and high-bandwidth photonics is needed.

53 Integration of electronics and photonics is typically achieved heterogeneously using two separate chips.
54 Transmitters using vertical-cavity surface-emitting lasers[4] have demonstrated energy-efficient data links at up to
55 56 GBd[5-7]. However, such directly modulated sources are bandwidth limited and higher symbol rates are hard to
56 achieve[1]. Externally modulated sources and external modulators offer a photonic high-speed alternative, and
57 photonic solutions based on lithium niobate[8,9], indium phosphide[10-18], silicon[19-25] and plasmonics[26-29] have emerged
58 for intensity modulation and direct detection (IM/DD) systems. So far, heterogeneous transmitters in bondwire
59 assembly[14,17,25,29] have shown the highest symbol rates, achieving 222 GBd with plasmonics[29], 192 GBd with indium
60 phosphide photonics[17], and 56 GBd with silicon photonics[25]. However, parasitics at the mismatched bondwire
61 interface eventually constitute a bottleneck to the speed. Alternatively, three-dimensional bonding or flip-chip
62 assemblies can reduce the interface parasitics[30], with 100 GBd operation being demonstrated using indium
63 phosphide photonics[14]. But heterogeneous integration remains a costly and non-ideal approach since two separate
64 high-performance chips are interfacing at the most critical position of highest data bandwidth.

65 Monolithic integration could overcome this bottleneck and reach higher symbol rates using ultra-short
66 direct connections known as on-chip vias. This use of a common substrate could offer a more compact footprint,
67 simplified testing and lower costs. However, most electronic and photonic technologies rely on two incompatible
68 material platforms, and thus new approaches are required. The silicon CMOS technology could provide a cost- and
69 energy-efficient solution for both electronics and photonics[31-34]. A full photonic library on a zero-change CMOS
70 platform with a 10 GBd data link has, in particular, been demonstrated[33], and has shown modulation at 40 GBd[34].
71 However, standard CMOS technology is bandwidth limited and cannot achieve the symbol rates of high-speed
72 heterogeneous demonstrations. Alternative monolithic solutions relying on indium phosphide or bipolar CMOS
73 (BiCMOS) technologies are therefore of interest. BiCMOS could be of particular value because it offers high-speed
74 electronics and is CMOS-compatible. In addition, plasmonics is, in principle, an ideal counterpart as a photonic
75 technology[35], offering bandwidths in excess of 500 GHz[36] and compatibility with a variety of substrate materials[37].

76 In this Article, we report a monolithically integrated BiCMOS electronic–plasmonic transmitter[38] that can
77 achieve symbol rates beyond 100 GBd. The transmitter is comprised of high-speed BiCMOS electronic layers and a
78 plasmonic layer on a single chip. The electronic layers offer a BiCMOS circuit that has been designed in line with
79 data-centre standards and performs a 4:1 power multiplexing to deliver on-off keying (OOK) signals to the
80 plasmonic layer above. The plasmonic layer consists of compact and high-bandwidth plasmonic Mach-Zehnder
81 modulators (MZM). The electronic and plasmonic layers are interconnected by vias. The chips have been designed
82 to operate at elevated temperatures and are tested in uncooled data modulation experiments. Operation at 120
83 GBd is demonstrated using a silicon-plasmonic MZM, and an ultra-compact modulator is created that shows
84 operation at 100 GBd on a footprint of 29 × 6 μm^2. Neither the BiCMOS electronics nor the plasmonic technologies
85 operate at their fundamental speed limit, suggesting that our approach could provide a route to 200 GBd and
86 beyond.

87 Concept

88 Our monolithically integrated high-speed transmitter is conceptually depicted in Fig. 1. The transmitter
89 consists of BiCMOS electronic layers (blue) and a plasmonic top layer (red), which are implemented on a common
90 substrate and connected through electrical wires (vias). The zoom-in to the plasmonic modulator shows the direct
91 high-speed connection of electronics with plasmonics.

92 In the electronic layer stack (blue), electrical signals are generated to drive the plasmonic modulators. A
93 multiplexer (MUX), designed in agreement to data centre standards, achieves highest data rates by performing a
94 4:1 multiplexing. The MUX input data is either externally supplied or generated on-chip. At the MUX output, a
95 power multiplexing stage replaces the standard output driver amplifier to achieve highest signal quality in an
96 energy-efficient implementation[39]. The SiGe BiCMOS platform hereby not only offers highest speeds and
97 CMOS-compatibility but also enables monolithic integration with photonic components based on the silicon
98 technology.

99 The plasmonic layer (red) comprises silicon photonics and gold plasmonics in a top layer: photonics for
100 passive and plasmonics for active components. In this layer, plasmonic Mach-Zehnder modulators (MZMs) convert

101 the electrical signals into the optical domain through light intensity modulation for reception with direct detection.
102 Plasmonic modulators, despite having increased insertion loss, are an ideal solution as they offer ultra-compact
103 footprint[40], independence of photonic substrates[37], high electro-optical bandwidth[36], energy-efficient modulation[41]
104 and operation at CMOS-compatible voltages[42]. The transmitter comprises two types of plasmonic MZMs on a single
105 substrate. A silicon-plasmonic MZM using photonic waveguides[43] was implemented together with an alternative
106 ultra-compact plasmonic MZM, where direct fiber-to-modulator coupling has been integrated into the device (see
107 zoom-in of Fig. 1). Both modulator types have been simultaneously driven, which is possible due to the compact
108 size and small capacity of plasmonic modulators.

109 The electronic layers and the plasmonic layer are connected by on-chip vias. Vias at the final power
110 multiplexer (PMUX) stage bring the electrical output signal directly to the plasmonic modulators. The proximity of
111 the PMUX outputs to the plasmonic modulators enables best signal quality at highest speed. Additional vias for
112 high-speed electrical interfaces are connecting the bondpads in the top layer with the electronic circuit beneath.
113 They give access to data input and clock in- and output. Note that the compactness of the plasmonic modulators
114 allows describing them as electrically lumped elements. This renders their electrical impedance a design parameter
115 and allows trading in driving voltage and energy consumption (see Methods).

116 Power dissipation in the high-speed electronics can lead to excess heating with temperatures hot spots
117 above 150°C. Hence, thermal co-design of electronics, plasmonics and packaging was crucial to successfully
118 demonstrating a monolithic transmitter (see Methods). Moreover, plasmonic switching in the modulators takes
119 advantage of a nonlinear electro-optic effect in an organic material[44]. Here, a nonlinear organic electro-optic (OEO)
120 material, 2:1 HLD1:HLD2 (ref. [45]), has been used in the device, which enables operation at elevated temperatures.
121 This organic material system mixes the anthracene-containing chromophore HLD1 and the acrylate-containing
122 chromophore HLD2, and allows for crosslinking without additional agents. Its thermal stabilization offers reliable
123 operation at temperatures beyond 120°C. With this configuration, we demonstrate 120 GBd data modulation with a
124 monolithically integrated transmitter.

125 ## Electronics

126 The electronics of the monolithically integrated chip needs to meet multiple demands. First, the data input
127 interface needs to be compatible with standard data centre sources. Second, a sufficiently high voltage swing with
128 smallest possible power consumption must be generated to drive the MZM at symbol rates of at least 100 GBd.
129 Third, a semiconductor technology well-suited for a photonic monolithic integration is required.

130 The electronic circuit that forms the MUX to drive the plasmonic modulator is shown with its corresponding
131 building blocks in Fig. 2a. The design considerations are presented in the following with the focus on the
132 monolithical integration together with an on-chip MZM. Details concerning the circuit development and
133 performance can be found in Refs.[46,47] for a previous version. The present implementation is detailed in Ref.[48]. A
134 4:1 MUX topology allows for conversion of data-centre-compatible 4 × 25 Gb/s non-return-to-zero (NRZ)
135 on-off-keying (OOK) input signals to a 100 Gb/s NRZ-OOK output signal at the MZM. Integrated delay locked loops
136 (DLL) align the input data to the MUX clock, see inset of Fig. 2a, and thereby automatically compensate for a timing
137 skew between the data inputs[49]. Regarding the use of the circuit in an integrated transmitter, a trade-off between
138 performance and power consumption has to be chosen. The presented design is optimized to reach highest
139 performance and to provide a large flexibility in order to enable the characterization of the transmitter under
140 various conditions (see Methods). Thanks to a wideband circuit design, the chip can be operated at flexible data
141 rates. For this, only the input clock frequency has to be adjusted correspondingly.

142 To drive the MZM, a power multiplexer (PMUX) concept is chosen such that no additional driver amplifier is
143 required. Instead, the final 2:1 selector (SEL) stage of the MUX directly drives the MZM. This offers several
144 advantages[39,47]. For the present application, the good signal quality at high data rates and the low power
145 consumption should especially be highlighted. The final 2:1 SEL has a power consumption of 0.9 W when operating
146 with a nominal differential voltage swing of 2 V_{pp} (1 V_{pp} single-ended) at highest data rates. The PMUX concept can
147 readily be extended to implement a PAM-4 transmitter by parallel connection of a second output stage with halved
148 output swing and reduced power consumption. For the present design, this option is not implemented, however, it

149 offers the potential to reach even higher data rates and higher energy efficiency. Design considerations concerning
150 the adaption of the output interface to the MZM are presented in the Methods.

151 For the implementation, the BiCMOS semiconductor technology SG13G2 from IHP (adaptions in Methods)
152 with a high transit frequency f_T = 300 GHz of the bipolar transistors has been chosen. Compared to compound
153 technologies (e.g. InP), which offer higher transit frequencies (e.g. f_T = 400 GHz enabling the fastest MUX known so
154 far with 222 Gb/s[29]), a BiCMOS technology brings the advantages of being cost-efficient and enabling a dense
155 co-integration of high-speed bipolar electronics with standard CMOS signal processing. Moreover, there are
156 developments of faster BiCMOS technologies that allow for an increase in the data rate of the presented circuit.

157 To assess the performance of the electronics (and of the MZM) without the need for an external data
158 source, an on-chip pseudo-random bit sequence (PRBS) generator has been integrated and connected to the data
159 inputs. On-chip measurements with a wafer probe at a chip variant with an electrical output interface demonstrate
160 the performance of the electronics. The presented circuit delivers a flat operation for clock frequencies up to
161 90 GHz (limited by measurement equipment), which was tested by applying a 1-0-1-0 sequence[48]. Data modulation
162 experiments show a clear open eye diagram for a data rate of 100 Gb/s, see Fig. 2b. Due to the external 50 Ω load
163 of the measurement equipment, the voltage swing of 1.2 V_{pp} is only half of the voltage swing at an integrated
164 high-ohmic MZM. A comparison between an on-chip measurement and when interfaced by bondwires at a data
165 rate of 120 Gb/s shows, how bondwires reduce the eye opening by almost 20 % and hereby degrade the signal
166 quality, see Fig. 2c. This demonstrates the advantage of monolithic integration, where no bondwires are needed.

167 Plasmonics

168 The plasmonic MZMs are the principal optical components in the demonstration for a monolithic integrated
169 transmitter. Three plasmonic modulator concepts were pursued in this work and integrated in the plasmonic layer:
170 two silicon-plasmonic MZM concepts, one driven with the internal MUX and one externally driven as a reference,
171 and a new ultra-compact MZM concept. All three concepts are based on the 500 GHz plasmonic modulator
172 technology[36] and have a built-in asymmetry in order to tune the operation point in the optical domain without the

173 need of an electrical bias. Fig. 3 introduces the new concept, depicts the co-integrated modulators and
174 demonstrates the capabilities of monolithic integrated MZMs.

175 The first modulator concept is based on silicon photonic waveguides and splitters and relies on previous
176 demonstrations from our group[27,43]. Standard single mode fibres connect to this device via grating couplers. Silicon
177 photonic multimode interference coupler split and combine the optical carrier. A photonic delay line in one arm of
178 the Mach-Zehnder interferometer allows choosing the MZM operation point by tuning the optical wavelength. The
179 actual modulation is performed in two plasmonic phase modulators[50] that operate in push-pull mode. The
180 co-integrated silicon-plasmonic MZM offers an extinction ratio of 35 dB with a total insertion loss of 25 dB. Fig. 3b
181 depicts a scanning electron microscope (SEM) image of the two modulator arms of the actual monolithic MZM.

182 The second concept is the ultra-compact plasmonic MZM with a footprint of only $29 \times 6\ \mu m^2$, which is
183 optically connected through a 24 µm pitched optical fiber array (OFA), see Fig. 3a. The direct fiber-to-slot coupling
184 scheme shown in the inset efficiently converts an optical fiber mode directly into a plasmonic slot mode, omitting
185 losses in intermediate photonic components[40]. Metallic y-splitters split and combine the optical carrier. Asymmetric
186 arm lengths cause a phase difference between the two MZM arms and fix the operation point. Two plasmonic
187 phase modulators constitute the MZM, which is driven in push-pull mode. Fig. 3c shows an SEM image of the
188 ultra-compact modulator co-integrated with electronics, which offers an extinction ratio above 10 dB and insertion
189 losses of 27 dB.

190 As a reference, an externally driven monolithic MZM was processed on the same chip to evaluate the
191 performance of integrated plasmonic devices on BiCMOS chips – but without interface to the electronics. Hereby,
192 the plasmonic modulator with insertion losses of 25 dB and an extinction ratio of 30 dB has been operated under
193 ideal conditions at room temperature. An amplified electrical data signal (V_p = 2.71 V, V_{rms} = 1.55 V) has been
194 applied to the modulator via an RF probe, which results in a higher voltage swing than for integrated solutions and
195 does not need a bandwidth-limiting bondwire interface. 100 GBd data modulation was demonstrated with a bit
196 error ratio (BER) $< 10^{-5}$ for two-level modulation (NRZ-OOK) (setup and measurement in Methods). Fig. 3d depicts

197 the corresponding eye diagrams. The received signal quality of 16 dB signal-to-noise ratio (SNR) indicates an
198 enormous potential for symbol rates beyond 200 GBd[51].

199 Monolithic integration

200 The monolithic integration of electronics and plasmonics was confronted with a set of challenges from
201 platform compatibility over module assembly to high processing demands. While the electronic chips were
202 produced in a SiGe BiCMOS foundry, the plasmonic top layer and the bondpads were post-processed directly onto
203 the electronic chip in the in-house facilities. In a final step, chip assembly and wirebonding to a dedicated printed
204 circuit board (PCB) as well as packaging and connectorisation were performed. The final monolithic test module is
205 depicted in Fig. 4, where the subfigures show zoom-ins at different scales – centimetre to micrometre scale – on
206 which the monolithic integration was optimized. Fig. 4a shows the complete test module with DC and RF
207 connectors and a PCB bringing the differential input data, clock and DC supply to the transmitter chip. Fig. 4b shows
208 the bondwire assembly connecting PCB and transmitter chip. Fig. 4c shows a microscope image of the monolithic
209 transmitter chip. Electronics and plasmonics were integrated on the same chip. A zoom-in to the plasmonic devices
210 is shown in the last subfigure, see Fig. 4d.

211 The electronic chip features five output positions, which are driven simultaneously. This allows the
212 implementation of multiple photonic components for evaluation – among which are the two plasmonic MZM
213 concepts presented above. This placement of multiple modulators is only possible for modulators with small
214 capacitances, whose simultaneous operation does not affect the electrical signal quality along the output
215 transmission line. Such an adaption of the electronic MUX would not be possible with alternative photonic
216 concepts.

217 A major challenge for monolithic integration is the high temperature environment in proximity to
218 electronics. Recent demonstrations showed temperature stability in organic-based plasmonic modulators up to
219 75°C[41], while the electronic chips reach 150°C at the core and up to 125°C at the output stage. Thermal modelling of
220 the transmitter chip allowed for improved placement of the modulators along the output transmission line (see
221 Methods). Still, to prevent degradation at high temperatures, a nonlinear organic electro-optic material

222 2:1 HLD1:HLD2 was developed[45]. A crosslinking procedure stabilized the organic material such that it can withstand
223 temperature above 120°C (see Methods). On-chip temperature measurements verified uncooled operation of the
224 monolithic transmitter at local temperatures above 112°C.

225

226 ## Monolithic transmitter performance

227 The monolithic transmitter was tested in a data modulation experiment with symbol rates of up to 120 GBd
228 under uncooled ambient air conditions and without encapsulation. The experimental setup is schematically given in
229 Fig. 5. An RF synthesizer serves as a clock source for the electronic circuit, which generates a PRBS data sequence of
230 2^9-1 bits with symbol rate of twice the input clock frequency. An external laser serves as light source and delivers 5
231 to 11 dBm optical input power to the chip (measured in fiber before chip). Light is coupled in and out of the
232 monolithic transmitter through optical fibres. Two types of plasmonic MZMs (see section 4) were simultaneously
233 driven – a silicon-plasmonic MZM and an ultra-compact plasmonic MZM. The modulated optical signal was
234 transmitted over an optical fiber link to the receiver. The signal was amplified and filtered before being received
235 with direct detection by a single photodiode. Five million samples of the converted signal are captured using 63 GHz
236 real-time oscilloscope with 160 GS/s. Offline digital signal processing (DSP) was applied for signal recovery and
237 equalization. Fig. 5a and b show the eye diagrams of different data rates for the two MZM types (full details in
238 Methods). 120 GBd were modulated with the silicon-plasmonic MZM with a BER of $1.74 \cdot 10^{-2}$ and 100 GBd with the
239 ultra-compact design with a BER of $3.95 \cdot 10^{-2}$. The lower-speed performance of the ultra-compact MZM is
240 associated to a non-optimal operation point of the MZM, as the device is only tuneable to the ideal quadrature
241 operation point through a voltage bias. Here, a voltage bias in the electronic layer has been omitted in order to
242 guarantee maximum signal quality at highest speed. Still, both BERs are below $4 \cdot 10^{-2}$ as required for successful
243 soft-decision forward error correction[52].

244

245 # Conclusions

246 Our approach offers a solution to a key challenge in next generation communication networks — the
247 high-speed co-integration of electronics and photonics — and provides a route to overcome the speed limitations in
248 current transceiver systems. We developed a monolithic integration platform that combines high-speed BiCMOS
249 electronics with high-bandwidth plasmonics connected through direct on-chip interfaces. The platform offers
250 high-speed data transmission, achieving symbol rates beyond 100 GBd. This was achieved through the co-design of
251 electronics and photonics, including thermal design and a nonlinear organic electro-optic material. Both the
252 BiCMOS electronics and plasmonic technologies are not yet at their limits, and symbol rates beyond 200 GBd should
253 be possible.

254

255 # Methods

256 ## Electronic Advantages of Monolithic Integration

257 Due to the monolithical integration of photonics and electronics on a single chip, the design of the output
258 interface as shown simplified in Extended Data Fig. 1 can be adapted to the MZM load. In contrast, for systems with
259 an external MZM, the output impedance of the electronics (R_{T1}) is typically designed as 50 Ω to match the
260 characteristic impedance of transmission lines (TML). As the MZM (R_{T2}) is typically matched to 50 Ω to terminate
261 the far end of the external TML, the voltage swing at the MZM is only half the source voltage swing for an open
262 output ($R_{T2} \rightarrow \infty$). In case of the monolithically integrated plasmonic MZM, a termination at both ends is not
263 required as the size of the MZM is small and thus can be assumed as electrically lumped. Thus, a single termination
264 that acts as a simple load resistor is sufficient, which doubles the output voltage swing compared to an external
265 MZM without an increase in current consumption. In principal, because of the low MZM load capacitance, the
266 matching can also be chosen larger than 50 Ω, which even decreases the current consumption further. For the
267 current implementation, however, a concept is chosen, where an on-chip TML is matched at one end only by its
268 characteristic impedance of 50 Ω ($R_{T1} \rightarrow \infty$, $R_{T2} = 50$ Ω). This allows multiple positions to place the MZM and thus

269 gives a degree of freedom for the experiments by choosing an optimal position with respect to temperature, signal
270 quality and integration processing. In our experiments, four MZMs are positioned at dedicated positions along the
271 TML. In the design of the electronics, the MZM capacitance is modelled by an increase in the distributed TML
272 capacitance. The related TML inductance is designed for a wave impedance of 50 Ω. That allows for a single 50 Ω
273 termination at the end of the TML whereby the signal amplitude along the TML (i.e. at each of the MZMs along the
274 TML) is approximately constant.

275 In addition to the advantages of the single termination of the lumped MZM, the monolithic integration
276 significantly reduces parasitic inductances and capacitances of the output interface as the interconnect length
277 between output stage and MZM is much shorter than for a heterogeneous approach as neither bondpads nor
278 bondwires are required. This lead to a higher bandwidth at the MUX-MZM interface.

279 Adaption of BiCMOS Process & Post-Processing

280 To enable the monolithic integration of plasmonic modulators on a BiCMOS electronic chip, the standard
281 BiCMOS fabrication process has been adapted. Normally, the BiCMOS platform does not provide a flat topography
282 at the end of the backend of line (BEOL) process and inter-metal vias are not directly accessible. To enable
283 electronic-plasmonic integration, the top-metal2 interconnect level and passivation were omitted and the
284 chemical-mechanical polishing process was optimized to allow for both low resistance access to the interconnect
285 vias (about 2 Ω per electrode or 16 Ω per via) and a smooth surface for modulator post-processing with a root mean
286 square roughness of 0.35 nm.

287 The post-processing of the plasmonic modulators was performed directly on top of the BiCMOS electronic
288 chip and aligned to the driver's output vias. The passive silicon-photonic structures were etched into a 220 nm thick
289 silicon layer, which was deposited at 300°C in plasma-enhanced chemical vapour deposition. The plasmonic
290 modulators were structured using a lift-off process for 150 nm of gold deposited by electron-beam evaporation. In
291 a last step, the OEO material was deposited by spin-coating. In order to stay below the thermal budget of a BiCMOS
292 electronic chip, all processes were performed at temperatures not exceeding 300°C.

293 ## Specifications of the Transmitter Module

294 The main specification of a transmitter module is its performance in terms of maximum symbol rate, which
295 was targeted in this demonstration. However, side specifications such as energy consumption and active device
296 area are becoming more and more relevant with increasing integration. Extended Data Fig. 2 shows both active
297 area and power consumption for each of the electronic circuit parts. The final 2:1 SEL and the high-speed clock
298 distribution (50 GHz) are the critical electronic components that have to be integrated on the transmitter chip. The
299 other circuit parts are optional and are implemented to show advanced functionalities and for testing purposes.
300 First, a 4:2 MUX is implemented in order to allow external data input at 25 GBd as in former data centre standards
301 for NRZ. Second, a circuit for input data alignment allows compensating for a timing skew on-chip. Third, a
302 reference clock out is added as an optional feature for clock synchronization in the measurement system. Further, a
303 frequency doubler serves as an alternative way to reach high-speed clock frequencies exceeding externally available
304 speeds. Last, an on-chip PRBS generator offers convenient and fast testing capabilities without external data input
305 and complements the external data inputs. Regarding the power consumption, the consumed energy-per-bit
306 amounts to 28 pJ/b for the critical on-chip circuit parts and 99 pJ/b for the full transmitter electronics including all
307 optional features. To analyse the data rate per unit area, the footprints of the plasmonic modulators have to be
308 measured. The area of the silicon-plasmonic MZM covers 13,000 μm^2, while the ultra-compact plasmonic MZM
309 occupies an extremely compact area of only 400 μm^2. By adding these values to the active area of the critical
310 electronic components, a data rate per unit area of 2.39 $Tb/s/mm^2$ for the silicon-plasmonic and of 2.65 $Tb/s/mm^2$
311 for the ultra-compact transmitter is found.

312 ## High Temperature Environment

313 Monolithic transmitters experience a high temperature environment due to power consumption on
314 smallest areas. This has a significant influence on the transmitter performance. The temperature distribution on a
315 transmitter chip has therefore been computed in simulations. The power is dissipated mainly in the transistors and
316 resistors in the electronic layers and the released heat is conducted to the chip backside, which is coupled to a heat
317 sink using a thermally conductive adhesive. The thermal model consists of the chip, which is discretized as an FEM
318 tetrahedral mesh, and the adhesive modelled by its thermal surface resistance to the heat sink, which is considered

319 as a constant temperature constraint. As the adhesive coverage of the chip backside is not known exactly, two
320 cases are considered: ideal and reduced thermal conduction to the heat sink. The temperature map for the reduced
321 case is depicted in Extended Data Fig. 3. A maximum temperature of 156°C has been simulated at the core, which
322 decays just below 100°C towards the chip edges. Multiple output positions to place the modulator have been
323 implemented. Beneath every odd output position and beneath the MUX core, a temperature diode has been placed
324 to measure the local on chip temperature. The measured values from a purely electronic chip and a post-processed
325 transmitter chip are stated in the table inset of Extended Data Fig. 3. The electronic chip thereby agrees well with
326 the ideal conducting simulation, while the post-processed transmitter chip experiences about 20°C higher
327 temperatures. The same difference is found in simulations for lower thermal conduction to the substrate.
328 Therefore, the temperature rise is assumed to be caused by the adhesive for transmitter assembly on the PCB.

329 Temperature-Stable Nonlinear Organic Electro-Optic Material

330 Temperature-stable nonlinear organic electro-optic (OEO) materials are a requirement for stable operation
331 of monolithic integrated plasmonic modulators. Besides temperature stability, the OEO material should maintain its
332 high electro-optic activity and large intrinsic bandwidth. The OEO material composite 2:1 HLD1:HLD2 exhibits
333 exactly these properties[45]. The material's glass temperature can rise by up to 100°C to a maximum of 175°C using a
334 crosslinking procedure while keeping a maximum thin-film electro-optic coefficient r_{33} of about 286 pm/V at
335 1310 nm wavelength. A thermostability measurement over 500 hours at 85°C in a vacuum oven confirmed the
336 long-term stability (99%) of the organic material.

337 In this work, we applied the OEO material 2:1 HLD1:HLD2 in an actual device and demonstrated data
338 modulation at temperatures above 112°C. The OEO material was poled with a poling field of 180 V/µm and
339 crosslinked at 150°C. Note that the monolithic modulators were connected to the electronics during this process.
340 The in-device temperature stability was evaluated by steadily increasing the chip temperature and measuring the
341 modulation efficiency using a sinusoidal signal at 60 GHz phase modulated onto an optical carrier at 1550 nm
342 wavelength. Extended Data Fig. 4 depicts the measurement results. The in-device OEO performance shows stable
343 operation up to 140°C after which the performance starts to degrade. The small dip at about 120°C is associated to
344 fluctuations in the measurement setup due to fiber instabilities because of thermal fluxes.

345 ## Characterization of Monolithic Modulators

346 The two plasmonic modulator concepts were characterized in optical transmission measurements. Typical 347 silicon-plasmonic MZMs achieve fiber-to-fiber insertion losses of 17 dB. In this monolithic implementation, the 348 insertion losses are higher, which is attributed to the following reasons. First, monolithic integration requires the 349 use of polycrystalline or amorphous rather than crystalline silicon in the photonic sections. Second, longer Mach-350 Zehnder configurations were chosen to guarantee sufficient modulation margin. The monolithic silicon-plasmonic 351 modulators were measured to deliver 25 dB total insertion loss (fiber-to-fiber) at a wavelength of 1549 nm with a 352 large extinction ratio exceeding 35 dB. Through cut-back measurements, the losses can be attributed to 5.5 dB per 353 grating coupler, 1 dB per photonic-plasmonic converter and 12 dB plasmonic propagation loss in a 20 µm long and 354 75 nm wide plasmonic slot waveguide. The ultra-compact plasmonic MZM was showing fiber-to-fiber losses of 355 16.5 dB in test structures. These losses are assigned to 6.5 dB plasmonic propagation loss, 4.5 dB per grating 356 coupler and y-splitter, and an extra 1 dB fiber array insertion loss. In the monolithic version, the total transmission 357 was −27 dB (on-state equivalent). The additional losses come from a longer plasmonic modulator section (14 dB in a 358 24 µm long modulator) and slightly lower grating coupler and splitter efficiency (6 dB). With progress in technology, 359 we anticipate total insertion losses to reach values below 10 dB for plasmonic modulators. Lower losses can be 360 achieved e.g. by introducing a differential signal operation[42], which will allow to reduce the modulator length by a 361 factor two, or by improving the nonlinear efficiency of the crosslinked OEO material[45]. Thus, the fundamental 362 plasmonic losses can be reduced below 5 dB. Further, by transferring the plasmonic modulator technology to 363 photonic fabrication sites, the fiber-to-chip coupling losses can be reduced to values below 2 dB alongside with a 364 reduction in silicon waveguide propagation losses[53].

365 The electro-optic performance of plasmonic modulators using the OEO material 2:1 HLD1:HLD2 was 366 measured on a reference plasmonic phase modulator. For this purpose, the OEO material was stabilized for 367 high-temperature environments using a crosslinking procedure, aged for 28 days and measured at 100°C. At 368 60 GHz, a voltage-length product of $V_\pi L$ = 240 Vµm was extracted for a phase modulator. For the monolithic Mach-369 Zehnder modulators demonstrated in this work, it can be halved to 120 Vµm and corresponds to a V_π voltage of 6 V. 370 From the voltage-length product, a nonlinear electro-optic coefficient r_{33} = 100 pm/V is estimated.

Externally Driven Monolithic Modulator

On the monolithic transmitter chip, separate modulators for external drive have been integrated as a reference for the characterization of the monolithic modulators, which are internally driven by the MUX. These modulators have not been connected to the underlying BiCMOS circuit, but equipped with contact pads to be externally driven via an RF probe. The passive characteristics were almost identical to the aforementioned integrated devices. Total insertion losses (IL) of 25 dB and an extinction ratio of 30 dB were measured. For the data modulation experiment, see Extended Data Fig. 5, the on-chip electronics has been turned off to measure the modulator performance at ideal room temperature. A 100 GBd electrical signal is generated using random bit sequence generator and an external DAC (MICRAM DAC4). The signal is then amplified and applied to the modulator via an RF probe. A tuneable external cavity laser source (9 dBm maximum output power, 100 kHz linewidth) generates the optical carrier at 1550.6 nm. The power of the laser can be adapted to power levels between 3 and 16 dBm by means of an amplifier. A subsequent band-pass filter (0.6 nm, IL ≤ 0.7 dB) suppresses the amplifier noise. This way, the modulator's performance can be tested for a large dynamic range of input powers. The plasmonic modulator converts the electrical signal onto the optical carrier before the data is transmitted over a back-to-back optical fiber link. At the receiver, the modulated signal is amplified to 10 dBm, band-pass filtered (2 nm, IL ≤ 0.7 dB) and received in a direct detection scheme (70 GHz photodiode with 0.6 A/W responsivity, 63 GHz real-time oscilloscope with 160 GS/s). In-house offline DSP is applied for signal recovery and equalization. 100 Gb/s NRZ were transmitted with a BER below 10^{-5} and an SNR of 16.44 dB.

Monolithic Transmitter Data Modulation Experiment

The monolithic transmitter has been tested in a data modulation experiment. To evaluate the BER, five million samples of the modulated signal are captured using 63 GHz real-time oscilloscope with 160 GS/s. Offline DSP has been used for signal recovery and equalization. For the latter, a linear equalization with 101 filter taps and nonlinear mapping with pattern length of 7 have been applied as required for high-speed data modulation and compensation of nonlinearities in the complete communication system. Note that the first few filter taps show the most significant improvement[42].

For the silicon-plasmonic MZM, data experiments with 50, 100 and 120 GBd were performed at a wavelength of 1551.7 nm with chip input powers of 8, 11 and 11 dBm, respectively. This corresponds to power ranges of 1.5 to 4.5 dBm into the modulator on the chip, -10.5 to -7.5 dBm at the modulator output and -17 to -14 dBm in the optical fiber at the output. 50 GBd were modulated with a BER of $1.93 \cdot 10^{-5}$ (SNR of 13.14 dB) below the KP4 FEC limit of $2 \cdot 10^{-4}$ [54]. 100 and 120 GBd were modulated with a BER of $9.21 \cdot 10^{-3}$ (SNR of 8.14 dB) and $1.74 \cdot 10^{-2}$ (SNR of 7.20 dB), respectively. Both BERs are below the SD-FEC limit of $4 \cdot 10^{-2}$ [52].

For the ultra-compact plasmonic modulator, 50 and 100 GBd data modulation was tested using an optical carrier at a wavelength of 1559 nm with 5 and 9 dBm chip input power. The corresponding powers are -1.5 and 2.5 dBm at the modulator input, -15.5 and -11.5 dBm at the modulator output, and -22 and -18 dBm in the fiber at the output. 50 GBd were modulated with a BER of $1.36 \cdot 10^{-3}$ (SNR of 10.14 dB) below the hard-decision FEC limit of $3.8 \cdot 10^{-3}$ [55] and 100 GBd with a BER of $3.95 \cdot 10^{-2}$ (SNR of 5.48 dB) below the SD-FEC limit.

Data Availability Statement

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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524

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529 ## Author Contributions

530 U.K., C.H. and J.L. designed the plasmonic platform. C.U., H.H. and M.M. designed the BiCMOS electronic
531 platform. U.K., C.U., H.H and Y.F. developed the monolithic integration process. C.H., W.H. and M.A. contributed to
532 the design and testing of the monolithic modulator. W.H., B.B., B.I.B. and A.J. contributed to the data modulation
533 experiment. H.X., D.L.E. and L.R.D developed the temperature-stable organic material. E.M. and B.P. contributed to
534 the design process. L.Z., S.L. and A.K. coordinated the wafer fabrication process. D.T., N.K. M.M. and J.L. designed
535 and coordinated the project. All authors contributed to drafting of the manuscript.

536 ## Competing Interest

537 C.H., W.H., B.B. are involved in activities toward commercializing high-speed plasmonic modulators at
538 Polariton Technologies Ltd. The other authors declare no competing interests.

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555 ## Figure Captions

556 Fig. 1. Monolithic electronic–plasmonic high-speed transmitter. High-speed SiGe BiCMOS electronic layers (blue)
557 with a top plasmonic layer (red) monolithically integrated on a common substrate (black) and connected through
558 on-chip vias (cylinders). The electronic circuit performs a 4:1 power multiplexing onto a single high-speed data rate
559 channel. Data inputs are either external or from an on-chip PRBS generator. The optical layer comprises plasmonic
560 MZMs that convert the electrical signals onto intensity-modulated optical carriers. The zoom-in shows an
561 ultra-compact monolithically integrated MZM directly driven by high-speed electronics. The compact dimensions of
562 plasmonic devices demonstrate the perspective towards densest integration of highly parallelized transmitters as
563 anticipated for future optical communication links.

564

565 Fig. 2. Electronic 4:1 power multiplexer performance. **a** Simplified block diagram of the electronics. The inset shows
566 a DLL element comprising an adjustable time delay, a master-slave-D-flipflop (MSDFF), a phase detector (PD) and a
567 low-pass filter (LPF). **b-c** electrical eye diagram measurements. Scaling: 2 ps/div, 200 mV/div. **b** 100 GBd on-chip
568 reference eye diagram. **c** 120 GBd on-chip eye diagram compared to a 120 GBd eye diagram via a bondwire
569 interface.

570

571 Fig. 3. Monolithic integrated plasmonic Mach-Zehnder modulators. **a** Ultra-compact plasmonic MZM with a
572 footprint of $29 \times 6\ \mu m^2$ for co-integration with electronics. The inset shows a schematic of the grating coupler for
573 direct fiber-to-slot conversion. **b-c** SEM images of the actual monolithic modulators before OEO material
574 deposition. **b** Silicon-plasmonic MZM and **c** ultra-compact plasmonic MZM. **d** Eye diagram of a 100 GBd data
575 modulation experiment of a monolithically integrated MZM on the same chip using an external driver. 100 Gb/s
576 NRZ-OOK were modulated with a BER $< 10^{-5}$.

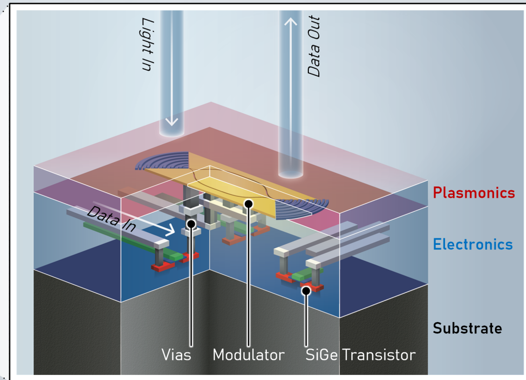
577

578 Fig. 4. Blow-up of the monolithic transmitter assembly. **a** Full transmitter assembly with PCB, DC supply pins and RF
579 connectors. **b** Monolithic transmitter chip connected via bondwires to the PCB. **c** Monolithic transmitter chip.
580 **d** Zoom-in onto the output stage with the plasmonic MZM devices on top of the electronic driver circuits.

581

582 Fig. 5. Data modulation experiment with monolithic transmitter. The transmitter is operated using on-chip PRBS
583 generation. The symbol rate thereby corresponds to twice the input clock. Optically, light from a laser source is
584 coupled to the plasmonic MZMs, where it is modulated before being transmitted via a fiber link. At the receiver, the
585 optical signal is amplified and filtered before being launched to a direct detection receiver. **a** Eye diagrams and SNR
586 for 50, 100 and 120 GBd as obtained with the silicon-plasmonic MZM. **b** Eye diagrams and SNR for 50 and 100 GBd
587 measured with an ultra-compact plasmonic MZM.

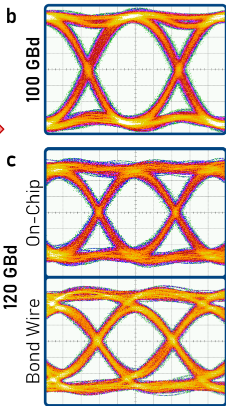
Plasmonics
A Externally Driven MZM
B Silicon-Plasmonic MZM
C Ultra-Compact MZM



SiGe BiCMOS Electronics
A Electrical Data In
B PRBS Generator
C Frequency Doubler
D Clock In
E 4:2 MUX
F 2:1 PMUX
G Clock/2 Out

Substrate

Monolithic Electronic-Plasmonic High-Speed Transmitter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τ
MSDFF
LPF
PD
DLL
PRBS
MZM
DLL
DLL
DLL
DLL
Data
Output
Data
Inputs
4:2
MUX
2:1
SEL
τ
τ
Clock
Input
f
2f
b
100 GBd
c
On-Chip
120 GBd
Bond Wire

a

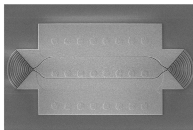
Ultra-Compact Plasmonic MZM

OEO

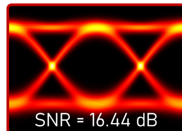
SiO_2 Si Au

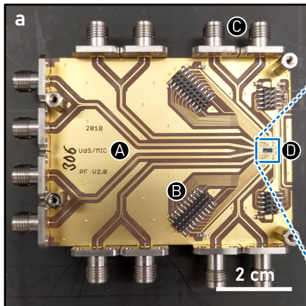
b Silicon-Plasmonic

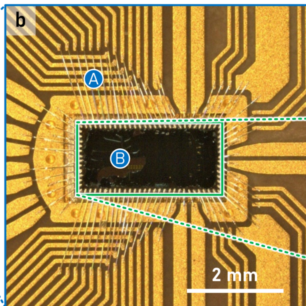
c Ultra-Compact

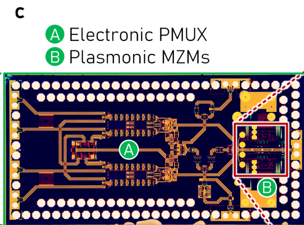


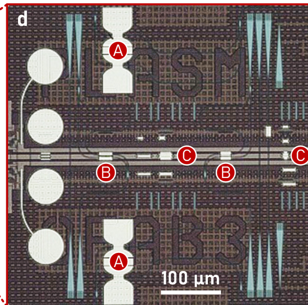
d 100 GBd NRZ




a
2018
UdS/MIC
PF V2.0
2 cm
A Printed Circuit Board
B DC Supply Pins
C RF Connectors
D Monolithic Transmitter


b
2 mm
A Bond Wires
B Monolithic Transmitter


c
A Electronic PMUX
B Plasmonic MZMs
1 mm


A Externally Driven MZM
B Silicon-Plasmonic MZM
C Ultra-Compact MZM
d
100 µm

Synthesizer

Clock In

Laser

Light In

Sources

Monolithic High-Speed Transmitter

0 1 1 0 1 0

Data Out

Optical Amplifier

Optical Filter

Direct Detection

Offline DSP

Receiver