High-performance waveguide-coupled Ge photo detectors for a photonic BiCMOS Technology

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Abstract:

In this paper we give an overview about IHP's work in ePIC technology development with focus on the integration of a waveguide-coupled germanium p-i-n photodiode with very high -3 dB bandwidth.

I. Introduction

Monolithic integration of Si photonics has been pursued for some time, chiefly on base of CMOS technologies [1, 2]. However, the question arises what electronic baseline technology fulfils best future communication system requirements. Looking beyond 100G systems, baud-rates exceeding 50GBd are needed for 400G transceivers. High-speed transistors are therefore a prerequisite for high-performance ePIC (electronic photonic integrated circuits) technology. A key device figure of merit is the product of transit frequency and breakdown voltage ($f_T \times BV$) in which state-of-the-art SiGe heterojunction bipolar transistors (HBTs) outperform scaled NMOS transistors, the CMOS workhorses for RF. In result, SiGe HBTs are often preferred over NMOS for high-speed analogue circuits.

SiGe BiCMOS has not only an RF performance advantage of 2–3 generations over CMOS [3], wherefore SiGe bipolar or BiCMOS technologies are presently often deployed for broadband applications in high-speed discrete photonics [4], but also provides sufficient voltage swing to drive the photonics.

IHP's photonic BiCMOS is a monolithic ePIC technology which combines high-performance HBTs with high-speed photonic devices for electronic-photonic submodules for next generation communication networks (Fig. 1). Here, the main features of the new technology are described, focusing on the germanium photo detector on the receiver side.

II. Photonic BiCMOS

In the RF domain, parasitic resistances, inductances and capacitances present limits to ultimate drivability, energy efficiency and speed of ePICs. The integration of the photonic devices such as waveguides (WG), modulators, and Ge photodiodes in the frontend-of-line (FEOL), i.e. at the same level with transistors, allows for a strong reduction of integration related parasitics because backend-of-line (BEOL) interconnect metals are used to connect photonic devices with electronic circuits. Pad capacitances and bond-related inductances are minimized or even avoided. The co-use of the 5 metal layers BEOL metal-stack is economically favorable in comparison to dual-backend approaches where electronics and photonics are processed independently and then are co-packaged.

The baseline BiCMOS process for photonic integration is a 0.25µm-technology. The conflicting substrate requirements of BiCMOS and photonics are resolved by a mixed substrate technology, the local-SOI approach, described elsewhere [5].

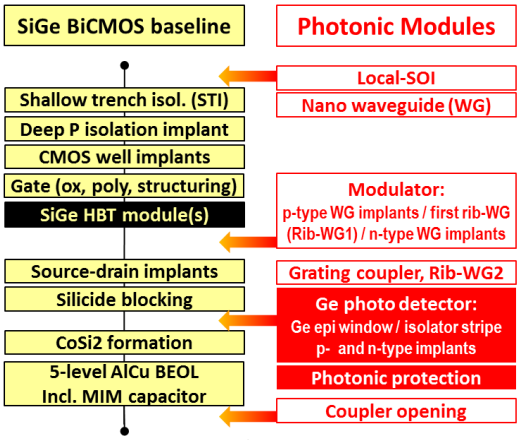

Fig. 1 Photonic BiCMOS process flow: Photonic modules are integrated in a SiGe BiCMOS baseline process.

III. Germanium Photo Detector Integration

A core device of the new photonic BiCMOS process is an integrated Ge p-i-n photodiode (Ge-PD). Based on a first PD generation with about 30GHz bandwidth and 0.8A/W responsivity, a new, much improved Ge-PD was integrated in the process [6]. Compared to the first one, the new PD offers more than two times higher bandwidth. The process flow of the detector module is illustrated in Fig. 2. The new PD structure results of a layout variation only, i.e. its fabrication does not need any process changes compared to the old device.

Small signal frequency response measurements were performed at zero-bias and under reverse bias of 2V. The increase in the -3dB bandwidth under all bias conditions is quite obvious when comparing the new to the previous PDs (Fig. 3).

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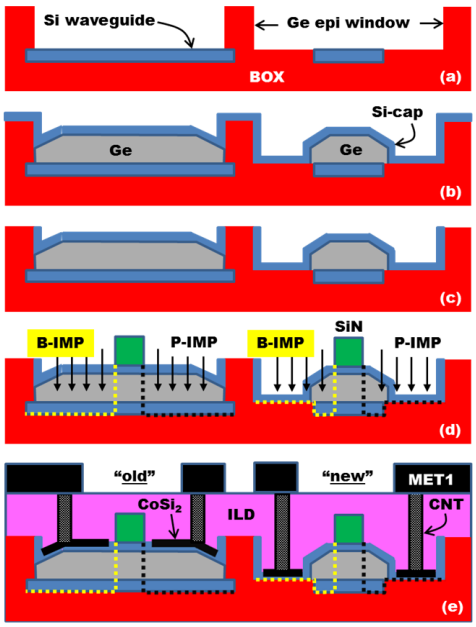

Fig. 2: Fabrication flow for first and latest Ge-PD generation.

The bandwidth improvement results from a reduction of the lateral dimensions of the doped Ge regions and the incorporation of non-doping implants that were used for diffusion length manipulation [7]. Both measures lower the impact of "slow" photo carrier diffusion. The first measure also reduces free carrier absorption. The separation of the absorption (Ge) from contact regions (Si) in the new diode structure also prevents metal absorption. Both measures are beneficial for the responsivity.

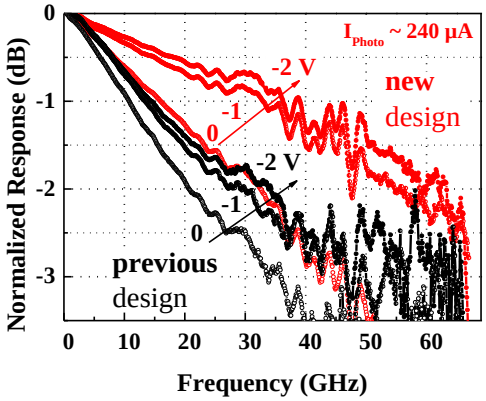

Fig. 3: Normalized frequency response of the previous and the new photo detector generations, obtained from small-signal measurements (67GHz LWCA, 1.55µm)

The diodes are fabricated from a Ge layer, selectively grown on a Si waveguide (Fig. 2, a-b). The epitaxy is carried out after the BiCMOS source-drain anneal (T_{Peak}>1000°C), but before the cobalt silicide module. In this way melting of the Ge layer and mixing it with underlying Si material is prevented. Moreover, any metal contamination of tools used for Ge epitaxy and pre-epitaxy wet cleaning is excluded. B and P implantation steps applied to form the lateral p-i-n structure are also carried out before silicide formation (Fig. 2, d). To achieve a Ge layer with low defect density (a prerequisite for low diode dark currents), layer deposition is carried out after a prebake step and under use of a cyclic annealing applied during the layer growth [8]. This additional thermal budget leads to several effects: dopant de-activation increases the SiGe-HBT base resistance and thus strongly lowers maximum oscillation frequency (f_{max}). By replacing the baseline SD-RTA by a spike-anneal (with higher temperature but shorter anneal time) dopant activation is improved and dopant diffusion is lowered. Besides degraded f_{max} values, also polysilicon resistors deviate from the baseline specification and the threshold voltage of the PMOS transistors were strongly reduced. Further, increased dopant diffusion has a negative effect in particular on the NMOS transistor short-channel V_{th} behavior. The following measures to counter these effects were applied: an increased NWELL doping level improved the PMOS behavior and a reduction of the NMOS source-drain implantation dose improved the NMOS behavior. In result, the photonic BiCMOS device behavior is now quite close to that of the baseline which enables the re-use of the baseline-PDK for the BiCMOS devices of the ePIC process.

IV. Conclusions

This contribution reviewed the integration of the Ge photo detector, a key component of IHP's photonic BiCMOS process. Performance issues of electronic devices and of the germanium detector itself were discussed and countermeasures were presented.

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