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Scaling Optical Interconnects Beyond 400 Gb/s

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Abstract *We present our vision towards scaling optical interconnect signalling rates to 200 Gb/s per lane within European project plaCMOS. The concept of a CMOS-compatible integration platform combining photonic, plasmonic and electronic functions is introduced and recent progresses are reported.*

Introduction

Datacenter traffic is growing in double-digit rates, underpinning the pressing need for higher speed optical interconnects. The first 400 Gb/s products, operating at 100 Gb/s per lane (50 Gbaud PAM4), are now emerging and the industry grapples to identify technologies that can keep pace with soaring bandwidth demand in view of next generation 800 Gb/s and 1.6 Tb/s systems expected before 2025[1].

Migration beyond 400 Gb/s is expected to benefit from a paradigm shift in system design that is leaning away from front-panel pluggable optics, and adopting optical engines closer to the switch ASIC. A manifold of reasons is fuelling this evolution, spanning from size and heat dissipation in the pluggable to signal integrity considerations, as the transition to higher symbol rates requires several retimers between the ASIC and the optical transceiver. Besides, as the switch capacity exceeds 12.8 Tb/s it becomes particularly challenging to escape the bandwidth from the electrical pads of the processor (i.e. from the BGA package)[2] and the availability of compact optical modules directly connected to the ASIC could be a viable way to mitigate this bandwidth bottleneck[3].

European project plaCMOS (www.placmos.eu) was conceived in order to tackle these challenges and deliver a photonic integration technology tailored to the requirements of future optical interconnects in terms of speed, size, power consumption and cost potential. The project concept is described in the following section and builds upon its partners' track record in silicon photonics, plasmonics and microelectronics. The plaCMOS multidisciplinary approach introduces profound innovations to the application domain by scaling signaling rate to 200 Gb/s per lane and shrinking the size of transceivers to the micrometer range, enabled by the introduction of plasmonic modulators. To allow the practical use of plasmonics in optical interconnects, plaCMOS will adopt a CMOS-compatible layer stack and fabrication approach that is suitable for CMOS volume manufacturing. The project will demarcate from previous polymer-based plasmonic modulators towards an environmentally-stable ferroelectric thin-film implementation. To reduce parasitics and simplify packaging plaCMOS will monolithically integrate photonics and electronics using

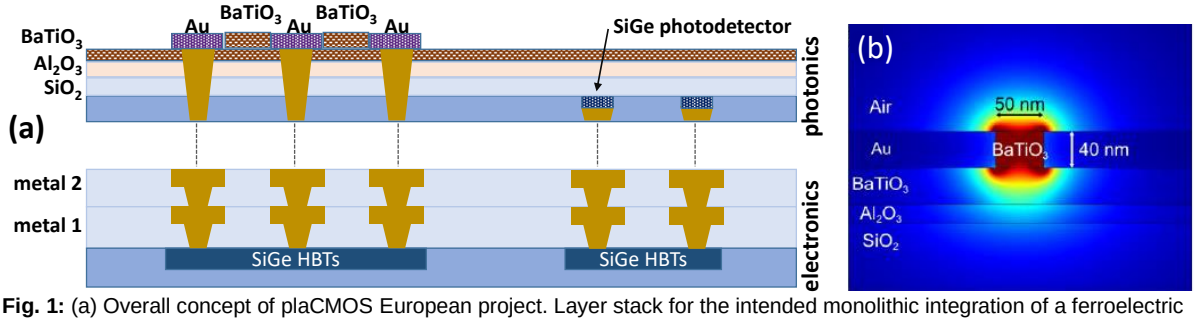

Fig. 1: (a) Overall concept of plaCMOS European project. Layer stack for the intended monolithic integration of a ferroelectric plasmonic modulator with germanium photodetectors and SiGe BiCMOS electronic power MUX and DEMUX. (b) layer stack of the plasmonic section and simulated optical mode.

Fig. 2: (a) SEM image of ferroelectric plasmonic Mach-Zender modulator; (b) 72 Gb/s eye diagram and measured BER before equalization; (c) 72 Gb/s eye diagram and measured BER after equalization.

advanced wafer bonding processes.

plaCMOS overall concept

The integration concept of plaCMOS is shown schematically in Fig. 1. In a nutshell, plaCMOS will pursue small-proximity wafer scale integration of novel ferroelectric-based plasmonic-photonic modulators, SiGe photo-detectors and BiCMOS electronics in a super-fast, micrometer-scale optical engine capable of transmitting and receiving at 200 Gb/s per lane. The plaCMOS integration platform is based on silicon photonics and can therefore leverage the extensive research in the field to add more functionalities. Optical multiplexing is pursued in plaCMOS in the wavelength (i.e. WDM) and space domain (i.e. using multi-core fibers) as complementary means to scale transceiver bandwidth, parallel to increasing the symbol rate. In the following sections the main building blocks of plaCMOS will be introduced and current progresses will be outlined. The project builds upon a solid technology base of its partners, part of which was developed in its predecessor EU project PLASMOFAB (www.plasmofab.eu/).

Ferroelectric Plasmonic Modulator

plaCMOS is developing plasmonic modulators based on Barium Titanate ($BaTiO_3$) thin films deposited on silicon. $BaTiO_3$ possesses a very high $\chi^{(2)}$ nonlinearity that allows fabrication of very compact and efficient modulators[4]. A Mach-Zehnder (MZ) device architecture is targeted, consisting of two ferroelectric phase modulators and multimode interference (MMI) couplers for splitting the light into the MZ modulator's arms. Access to the plasmonic phase modulators is facilitated by tapered mode converters.

A prototype of plaCMOS ferroelectric modulator was fabricated recently based on 10-µm-long phase modulators[5]. An 80-nm-thick $BaTiO_3$ film was deposited by molecular beam epitaxy on an SOI wafer, which was subsequently bonded with a highly resistive silicon wafer covered with a 3 µm SiO_2 layer. The original (handling) SOI wafer was stripped and the buried oxide was removed. The silicon photonic elements and the $BaTiO_3$ strips were structured by electron-beam lithography and gold electrodes were applied.

The fabricated ferroelectric plasmonic Mach-Zehnder modulator prototype achieved a V_π of 14.5 V and an overall insertion loss of 25 dB which is subject to improvement by optimizing the main sources of loss (sidewall roughness, plasmonic-to-photonic mode converters, grating couplers). The device was driven at 72 Gb/s by a digital-to-analog converter (DAC) with 72 GSa/s sampling rate and 16 GHz bandwidth. The electrical test sequence was amplified to 2.8 V_p and was introduced to the modulator in dual-drive configuration. The signal was detected in a 70 GHz photodiode and digitized with a 62 GHz, 160 GSa/s oscilloscope. The bit-error-rate (BER) was measured after offline processing that involved timing recovery, resampling, least mean square (LMS) equalization and hard decision. The BER was $7.66 \cdot 10^{-4}$ and $5.68 \cdot 10^{-5}$ before and after equalization, which is compatible with a 7% overhead hard-decision FEC.

SiGe BiCMOS power MUX

plaCMOS is developing a multiplexer (MUX) and demultiplexer (DEMUX) circuit on SiGe BiCMOS technology as an integral part of its plasmonic-photonic-electronic platform. Monolithic integration of the electronics with the plaCMOS plasmonic modulator allows minimization of bandwidth-limiting parasitic L-C elements. The ultra-short plasmonic modulator acts as a lumped capacitive load of only a few fF, therefore no 50-Ω end-termination is required.

A preliminary MUX prototype was recently demonstrated[6], performing 8:1 multiplexing into a 100 Gb/s NRZ signal. The MUX was co-designed with the modulator but has not been co-integrated yet. The 8:1 MUX is implemented as two 4:1 MUXs followed by a selector stage, whereas each 4:1 MUX consists of three 2:1 MUXs in a tree architecture. A power-multiplexer (PMUX) configuration was implemented achieving a differential output swing of 2.5 V_{pp}, sufficient to drive directly the plasmonic modulator.

The PMUX was fabricated in IHP SG13G2 SiGe BiCMOS process (f_T=300 GHz, f_{max}=500 GHz). The chip was assembled into an RF evaluation

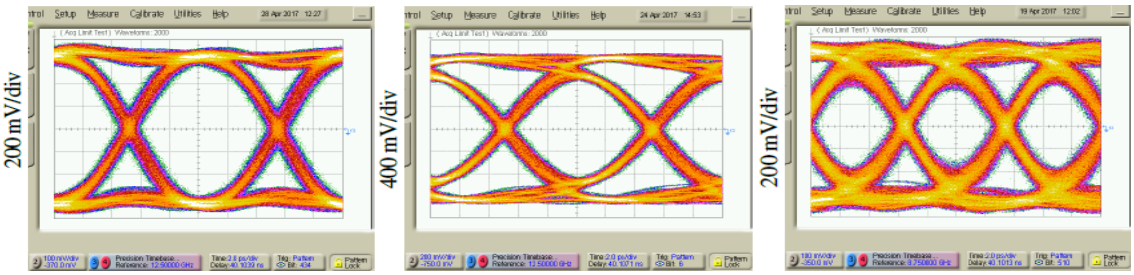

Fig. 3: Measured on-die differential output eye diagrams at (a) 100 Gb/s, with differential output swing of 1.2 V_{pp}; (b) 100 Gb/s, with differential output swing of ~2 V_{pp}; 140 Gb/s, with differential output swing of 1.2 V_{pp}. Timebase is 2 ps/div.

board providing K connectors for all high-speed I/Os except for the PMUX output which was probed. The PMUX was tested at 100 Gb/s and exhibited clear eye openings with 310 fs_{rms} jitter (Fig. 3 (a)). Voltage swing was 1.2 V_{pp} differential at the oscilloscope's 50-Ω load, which is doubled when connecting the modulator's impedance. Further measurements at 140 Gb/s are shown in Fig. 3 (c), verifying the technology's scalability.

Plasmonic waveguides

Plasmonics is emerging as a key technology for shrinking the size of photonic integrated circuits (PICs) and for dramatically improving their power efficiency, owing to stronger light-matter interaction. To counterbalance the high propagation losses of plasmonic waveguides, co-integration with photonic platforms is targeted, most notably silicon photonics. Following proof of concept demonstrations with noble metals recent efforts focus on CMOS-compatible plasmonics, using copper, titanium nitride and aluminum[7].

The feasibility of plasmonic waveguides to carry high bandwidth WDM signals was recently demonstrated by plaCMOS partners[8]. An 80 nm × 7 µm Al surface plasmon polariton (SPP) waveguide was created in a Si_3N_4 platform. The SPP waveguide was formed inside a cavity, directly on top of the buried oxide layer, whereas coupling to the Si_3N_4 was achieved with a 7.5 µm linear waveguide taper serving as a plasmo-photonic interface. In and out coupling to the chip was facilitated with TM grating couplers on the Si_3N_4 waveguide layer. Plasmonic propagation loss was measured at 0.087 dB/µm corresponding to a record high plasmonic propagation length L_{spp} of 50 µm, whereas the plasmonic to photonic interface loss was 4.4±0.3 dB. A 200 Gb/s (8×25 Gb/s) WDM data stream was transmitted through the chip obtaining error-free operation with a power penalty of 0.15±0.05 dB at BER of 10^{-9}, verifying the concept's suitability for WDM interconnects.

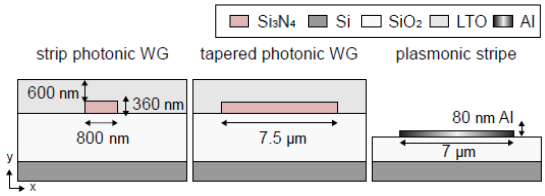

Fig. 4: Cross-sections of Si_3N_4 and Al waveguides.

Conclusions

We presented the vision of European project plaCMOS for scaling optical interconnects beyond 400 Gb/s. A monolithic integration platform combining silicon photonics, plasmonics and SiGe BiCMOS electronics is under development aiming to leap forward with signalling rates of 200 Gb/s per lane. Preliminary results exhibit promising performance of the main building blocks in the plaCMOS concept.

Acknowledgements

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References

[1] The 2018 Ethernet Roadmap, https://ethernetalliance.org/the-2018-ethernet-roadmap/.

[2] Ali Ghiasi, "Large data centers interconnect bottlenecks," Opt. Express, Vol. 23, p. 2085 (2015).

[3] M. S. Achter et al., "WaveLight: A Monolithic Low Latency Silicon-Photonics Communication Platform for the Next-Generation Disaggregated Cloud Data Centers," Proc. HOTI, Santa Clara (2017).

[4] S. Abel et al., "A hybrid barium titanate-silicon photonics platform for ultra-efficient electro-optic tuning," J. Lightwave Technol., Vol. **34**, no. 8, p. 1688 (2016).

[5] A. Messner et al., "Integrated Ferroelectric Plasmonic Optical Modulator," Proc. OFC, Th5C.7, Los Angeles (2017).

[6] C. Uhl et al., "A 100 Gbit/s 2 Vpp power multiplexer in SiGe BiCMOS technology for directly driving a monolithically integrated plasmonic MZM in a silicon photonics transmitter," Proc. BCTM, Miami (2017).

[7] R. Zektzer et al., "Experimental demonstration of CMOS-compatible long-range dielectric-loaded surface plasmon-polariton waveguides (lr-dlsppws,", Optics Express, Vol. 22, p. 22009 (2014).

[8] G. Dabos et al., "CMOS plasmonics in WDM data transmission: 200 Gb/s (8 × 25Gb/s) transmission over aluminum plasmonic waveguides," Opt. Express, Vol. 26, p. 12469 (2018).