DOI: 10.1109/MTTW51045.2020.9245066

5G and beyond: Multi Baseband PSSS Architecture for 100 Gbps Wireless Communication

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***Abstract*—In this paper, our concepts for high-speed wireless transceivers that might achieve 100 Gbps in the near future are shown. The targeted carrier frequency is 240 GHz, and the parallel sequence spread spectrum (PSSS) is proposed as a modulation scheme. Although the PSSS is very rarely used for data communication, we show some exciting concepts for the practical realization of high-speed analog PSSS circuits. The PSSS has several advantages when used in high-speed applications. Moreover, we extend the basic PSSS concept by the idea of baseband signals combining. This significantly reduces processing effort and allows to process the baseband signal in parallel. Each baseband processing core can additionally use a parallel bank of AD and DA converters, so that processing of ultra-high-speed signals with relatively large bandwidth is further simplified.**

Keywords— high-speed THz communication, wireless, baseband processing, parallel sequence spread spectrum, baseband signals combining

I. INTRODUCTION

The sub-terahertz (sub-THz) band of 200-300 GHz allows utilizing a large bandwidth for wireless communication. This is one of the key elements to achieve high data rate using a conventional transmission at spectral efficiency in the range of 2 to 5 bits/s/Hz. This relatively low spectral efficiency allows avoiding very complex transmission schemes that can be difficult to realize in the THz band, and at the speed of 100 Gbps. First of all, we face the problem of high attenuation and short distances that are supported by the THz transmitters. In general, the free-space path loss rises with the square of the carrier frequency. At the carrier frequency of 300 GHz, we calculate an attenuation of ca. 102 dB for a 10m link. Moreover, manufacturing power amplifiers for the targeted band is difficult and requires technology with high cutoff frequency and maximum oscillation frequency. Thus, the power delivered by the sub-THz transmitters is relatively low as compared to 5 GHz and 60 GHz bands. Secondly, the data rate of ≥100 Gbps makes the ADC, DAC, baseband, and data link layer processing very demanding. In order to process such fast data streams, we need to process each data bit in the time shorter than 10 ps. For example, the access time of a standard DDR memory installed in today's PC is in the range of ca. 40 ns [1], so the access time is one order of magnitude longer. Although the sub-THz band and high-speed wireless communication are in the focus of several research groups, the addressed topic is very challenging. It demands new processing ideas that can work at a very high speed. Thus, in this paper, we present our view for high data rate wireless communication at sub-THz channels. We propose multi baseband parallel sequence spread spectrum (PSSS) processing, which is rarely used for data communication. Moreover, we show multi baseband processing that allows to split the baseband bandwidth to a number of independent processing chains. Each chain can be realized as an independent processing core implemented as separated silicon ASIC. Thus, we enable "multi-processor" baseband processing, which is new in in conjunction with PSSS.

All the ideas described here are not yet fully realized and integrated. Nevertheless, we conducted some experiments, which confirm that this processing can work in a real ASIC implementation. Unfortunately, so far, we cannot prove that the practical realization of our vision can outperform the classical OFDM and single-carrier transmission schemes in any of the critical aspects (data rate, complexity, power consumption, transmission range, bandwidth efficiency, etc.). Instead, it is a future oriented vision that needs to be further investigated, optimized and compared with state of the art.

II. Related Work

Firstly, we go through available publications about PSSS. Later, we show frontends and data link layer processor that can be used for a complete 100 Gbps demonstrator.

A. Parallel Sequence Spread Spectrum (PSSS)

The idea of using PSSS for wireless communication is not new but relatively rare. In [2], the authors show a PSSS communication scheme dedicated to industrial wireless communication at a data rate of a few Mbps (≈7.2 Mbps [2]). The central aspect investigated there are code division multiple access and robustness of spreading systems in general. They show a practically realized platform [3] and transmission experiments at a data rate of up to 17.9 Mbps. Although the system supports a low data rate as compared to our application, the authors fully validate their scheme by implementing a real demonstrator. Moreover, they have proven that PSSS can be applied for wireless communication.

An (ultra) high-speed PSSS communication scheme has been investigated as well. One of the most promising transmission experiments is shown in [4], where a hardware in the loop experiment is performed. A data rate of 20 Gbps at BER of $5.4 \cdot 10^{-5}$ has been measured. Although the authors investigate many aspects of fully integrated transmitter and receiver designs [5]–[8], we could not find any publication that shows the complete system fully integrated (transmitter and receiver with all synchronization elements). This indicates that the construction of a 100 Gbps PSSS baseband processor is challenging. Later in this paper, we show our concept that significantly relaxes the demands of analog and digital PSSS circuits.

B. THz frontends (up- and down-converters)

PSSS as such is just a modulation scheme that produces a baseband signal. This signal needs to be up- and down-converted into the sub-THz band. For this reason, we employ BiCMOS circuits made in 130 nm technology [9]. In [10], a fully integrated 240 GHz frontend is shown. The circuit has been tested and supports a bandwidth of 35 GHz for the transmitter, and 55 GHz for the receiver. It has been proven that it allows establishing a robust link with 100 Gbps throughput [11].

Another THz frontend that is used for high-speed PSSS experiments in the sub-THz band is shown in [12]. The results of these experiments are reported in [13], where the authors achieve 80 Gbps with 4 bit/s/Hz PSSS modulation. The authors use a Tektronix AWG (arbitrary waveform generator) and sampling scope. Thus, the setup consists of commercial measurement devices and Matlab offline processing algorithms. It does not contain any specific circuits designed and fabricated for PSSS transmission. The LO signal is shared between the RX and TX, so the synchronization algorithms are not demonstrated.

C. Data link layer processing and forward error correction

The proposed PSSS scheme and RF-frontends allow transmitting data bits encapsulated into frames. However, there is still a need to control bit errors and correct them according to the link quality. For this reason, we developed our own data link layer processor, which runs in real-time on an FPGA [14], and also has been fully characterized in 28 nm Global Foundries CMOS technology [15]. The solution supports data rates up to 145 Gbps and is fully compatible with PSSS modulators [16]. The most important aspect of the presented work is the low-energy Reed-Solomon forward error correction engine combined with link adaptation algorithms. The solution changes the number of redundancy symbols according to the link quality. The maximal accepted BER is 2×10^{-2}.

III. Proposed Communication Architecture

Before going into details about the proposed scheme, we explain how the PSSS (parallel sequence spread spectrum) works.

A. PSSS processing for data communication

In general, PSSS has been proposed as a spreading technique for different communications systems [3], [17]–[19]. Fig. 1 depicts a simplified diagram of a PSSS-encoder. PSSS spreads the signal over the frequency band. Briefly, it consists of parallel spreaders and spreading sequences, denoted as $SEQ\ 1, SEQ\ 2, \cdots, SEQ\ N$ in Fig. 1. All PSSS codes are mutually orthogonal.

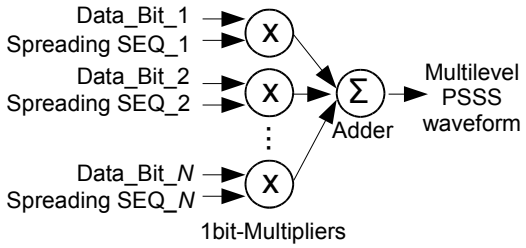

Fig. 1. Parallel sequence spread spectrum (PSSS) encoder.

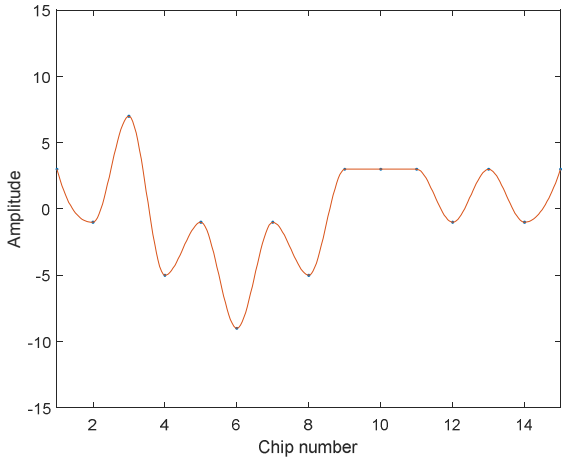

Fig. 2. Example of 1 bit/s/Hz PSSS waveform in the time domain (amplitude modulation).

The input data bits, denoted by *D*:

$$\mathrm{D} = \{ \mathrm{d}_1, \mathrm{d}_2, \mathrm{d}_3, \ldots, \mathrm{d}_\mathrm{N} \}, \mathrm{d}_\mathrm{k} = \begin{cases} +1 \\ -1 \end{cases}, \quad (1)$$

are multiplied by orthogonal sequences (e.g., cyclically shifted Barker codes or m-sequences), represented as:

$$\{ \mathrm{a}_1, \mathrm{a}_2, \mathrm{a}_3, \ldots, \mathrm{a}_\mathrm{N} \}, \mathrm{a}_\mathrm{k} = \begin{cases} +1 \\ -1 \end{cases}, \quad (2)$$

and then added in the time domain, resulting in:

$$\mathrm{C} = \mathrm{D} \times \mathrm{A}, \quad (3)$$

where matrix *A* is defined by:

$$\mathrm{A} = \begin{bmatrix} \mathrm{a}_1 & \mathrm{a}_2 & \mathrm{a}_3 & \ldots & \mathrm{a}_\mathrm{N} \\ \mathrm{a}_2 & \mathrm{a}_3 & \cdots & \mathrm{a}_\mathrm{N} & \mathrm{a}_1 \\ \mathrm{a}_3 & \cdots & \mathrm{a}_\mathrm{N} & \mathrm{a}_1 & \mathrm{a}_2 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \mathrm{a}_{\mathrm{N}-1} & \mathrm{a}_\mathrm{N} & \mathrm{a}_1 & \cdots & \mathrm{a}_{\mathrm{N}-2} \\ \mathrm{a}_\mathrm{N} & \mathrm{a}_1 & \mathrm{a}_2 & \cdots & \mathrm{a}_{\mathrm{N}-1} \end{bmatrix}, \quad (4)$$

and the multivalent elements of *C* are:

$$\mathrm{C} = \{ \mathrm{c}_1, \mathrm{c}_2, \mathrm{c}_3, \ldots, \mathrm{c}_\mathrm{K} \}, \ \mathrm{c}_\mathrm{k} \in \langle -\mathrm{N}, \ldots, \mathrm{N} \rangle, \quad (5)$$
$$\mathrm{c}_\mathrm{k} = \sum_{\mathrm{i}=1}^{\mathrm{N}} \mathrm{a}_{(\mathrm{k}+\mathrm{i}-1) \bmod \mathrm{N}} \, \mathrm{d}_\mathrm{i}.$$

This results in a multilevel amplitude waveform (denoted by *C*), which carries *N* data bits in *N* multilevel-chips (Fig. 2).
Thus, in contrast to the direct sequence spread spectrum (DSSS) systems, the rate of the PSSS modulated data is unaffected, assuming modulation at the same spectral efficiency for both techniques.
At the receiver side, the received baseband sequence becomes *C'*:

$$\mathrm{C}' = \mathrm{C} + \mathrm{Noise} + \mathrm{Interferences}, \quad (6)$$

$$\mathrm{C}' = \{ \mathrm{c}'_1, \mathrm{c}'_2, \mathrm{c}'_3, \ldots, \mathrm{c}'_\mathrm{K} \}.$$

The receiver correlates the *C'* signal with spreading sequences stored in matrix *A,* by performing:

$$\mathrm{R} = \mathrm{C}' \times \mathrm{A}. \quad (7)$$

The integration of the correlation values of the *R* vector allows to decide whether the received bits are 0s or 1s. Higher-order modulations are also possible. We suggest to sample and process the resulting baseband signal in parallel by *N* analog to digital converters, as shown in Fig. 3 (similar architecture was already proposed in [6], [8]). This significantly relaxes the ADC processing effort for high bandwidth systems and is one of the main advantages of using PSSS in our system.

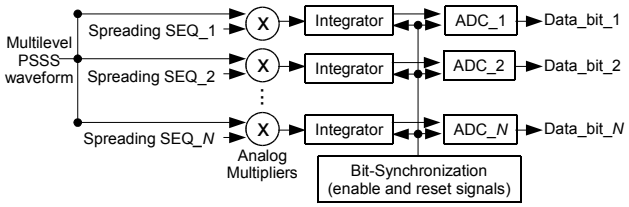

Fig. 3. Parallel sequence spread spectrum (PSSS) decoder. Figure adapted by authors from [6] and [8].

Fig. 2 depicts an analog waveform in the time domain produced by a 1 bit/s/Hz PSSS modulator. This is the simplest PSSS scheme that employs amplitude modulation only. Higher spectral efficiency is possible as well but requires to construct dedicated spreading sequences that have strong cyclic-autocorrelation properties, and are strongly orthogonal to each other at the same time. We still investigate this topic and search for new sequences that fulfil this requirement. One of the methods suitable for the construction of such sequences is given in [20], where the authors use a kind of genetic algorithm to find suitable codes. It is worth mentioning that similar code construction methods were popular in military radar applications. Thus, there is a large pool of publications that investigate comparable sequences from the mathematical perspective. Instead, we follow numerical methods and genetic algorithms. Nowadays, a standard PC can check thousands of different codes in a second. The sequences employed here are relatively short, and the set of binary sequences is tiny. Therefore, for future developments, we target to employ codes with floating-point coefficients. To the best of our knowledge, such codes have never been investigated for such applications.

For our target system, to relax the timing requirements for the analog PSSS and ADC circuits, we propose to split the PSSS processing among five parallel cores. Therefore, each PSSS-baseband core needs to support ca. 20 Gbps. This data rate is more realistic than processing the complete 100 Gbps in a single circuit. Details of this idea are elaborated in the next section.

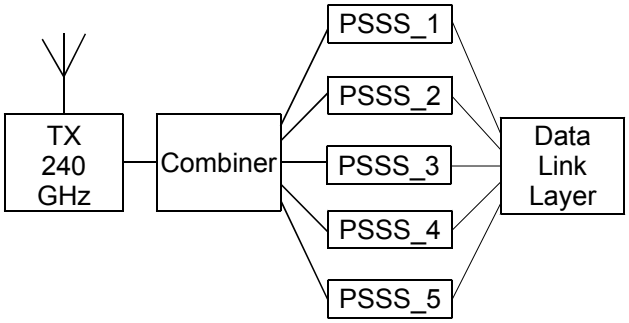

Fig. 4. Proposed multi-core (multi-processor) PSSS processing - transmitter.

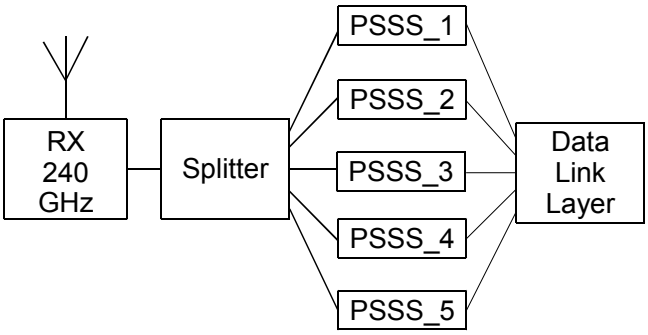

Fig. 5. Proposed multi-core (multi-processor) PSSS processing - receiver.

B. *Five-core PSSS processing*

Together with PSSS, we propose analog combiners/splitters to join/divide the baseband signal among five processors/cores. After that, we are able processing the signal entirely in parallel, as shown in Fig. 4 and Fig. 5. Each PSSS baseband processor needs to process 'only' 20 Gbps (5 × 20 Gbps = 100 Gbps). Moreover, this system allows to use up 5 × 15 parallel ADCs. Thus, the ADC bandwidth is significantly relaxed. Each PSSS processor that employs codes of the length of 15 needs exactly 15 ADCs (N = 15 in Fig. 1 and Fig. 3, according to the results shown in [8]). Due to the reason that we insert five PSSS cores in parallel, the total number of parallel ADC is 5 × 15 = 75. Such a high number of converters can be instantiated only in a highly integrated chip. Assuming that 4 bits/s/Hz modulation is used, the individual ADCs can work at sampling speed as low as ca. 1 GSps.

The proposed multi-core (multi-processor) baseband processing can be applied, only if we instantiate an analog combiner and splitter between the frontend and the PSSS processing array (Fig. 4, Fig. 5).

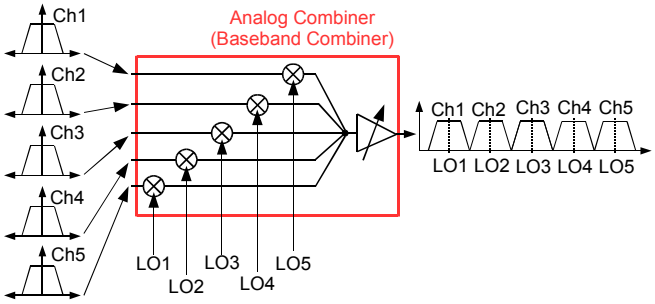

Fig. 6. Proposed analog baseband combiner [21], [22].

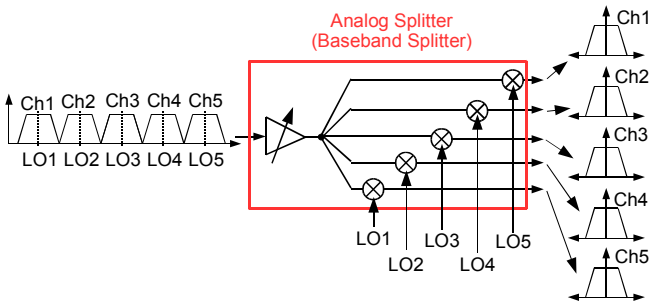

Fig. 7. Proposed analog baseband splitter [21], [22].

C. *Analog basband combiner/splitters*

The analog baseband combiner/splitter (Fig. 6, Fig. 7) allows to merge and split the individual baseband signals on the transmitter and receiver side respectively. The combiner is designed as a dedicated BiCMOS chip in 130 nm technology. The combining functionality is realized by a set of analog mixers working with specifically tuned local oscillators, LO1-LO5, as shown in Fig. 6. Thereafter, the signal is added and amplified.

The proposed analog combiner/splitter allows to sample and process the baseband-signal in parallel chains. This reduces the effort for the baseband-processing and ADC/DAC sampling. In our case, the effort is reduced by five times. We divide the complete signal bandwidth to five computational chains and process it by five independent BB processors. Thus, the demands for each individual baseband are reduced by five times. The PSSS modulation reduces the sampling rate by a factor of 15 additionally [8]. This is especially important for communication systems that operate at >100 Gbps and require ultra-fast converters. We also investigate PSSS-31 circuits with a spreading sequence length of 31. The longer codes show better spreading performance, and allow to use 31 converters in parallel. However, such architecture requires significantly more complex PSSS circuits.

The combined baseband signal has to be split into individual channels on the receiver side. Therefore, we need an analog splitter (Fig. 7), which is a mirrored version of the combiner. Although the combiner and splitter have similar functionalities and comparable functional blocks, both elements have to be individually designed, tuned, and fabricated. This means that two analog circuits for the baseband combining/splitting have to be made.

IV. Conclusion

In this paper, we show our vision of constructing ultra-high-speed transceivers dedicated to 100 Gbps wireless communication at the sub-THz band. It is a future oriented scheme that needs to be further investigated, optimized and compared with state of the art. To the best of our knowledge, such PSSS baseband has never been investigated together with baseband signal combiners. Thus, in our concept, we can build a parallel computation array for PSSS processing. This relaxes the demands for analog PSSS circuits. Moreover, we significantly reduce the demands for ADCs and DACs. This scheme is attractive for high-speed communication, where ADC and DAC performance is critical, and cannot be realized by standard converters. Here, we show how to divide the 100 Gbps signal into parts, and process it by parallel converters. Although the parallel processing for high-speed analog PSSS is already known [6], [8], we additionally improve the concepts by baseband combining. Thus, we believe that our ideas bring the high-speed PSSS communication one step closer to reality.

Currently, it is difficult to decide whether PSSS processing for such applications makes sense. This will not

be proven, until the first complete PSSS transceiver is practically realized and characterized against state of the art. Thus, we emphasize the fact that the methods shown here are not demonstrated in a practical application yet. Special care has to be taken before applying it in a real system.

V. Future Work

At this point, we cannot show any designed and fabricated PSSS circuits that operate at the targeted data rate and carrier frequency. Moreover, the construction of PSSS algorithms with IQ modulation is poorly investigated. Therefore, one of the first research challenges is to design a practical circuit that has spectral efficiency higher than 1 bit/s/Hz and works with very low IQ leakage. This demands new pairs of spreading sequences, which have very low cross-correlation and very strong cyclic autocorrelation at the same time. We target to search such codes not only in the binary domain, but most probably, we need to define the code alphabet in the real domain. This extends the set of possible solutions infinitely. The binary codes give a small set of possible sequences for the PSSS-15, and all these solutions can be tested relatively quickly on a standard PC by using brute force methods. To investigate the spreading sequences with real coefficients, we plan to employ genetic algorithms. This also is a non-standard method of constructing such codes, which we would like to verify soon.

Baseband combiners and splitters with <2 GHz bandwidth per channel are already known [21], [22], the question is if we can increase the number of parallel channels, and increase the bandwidth at a relatively low area and power consumption overhead. One of the main problems in the design of such circuits is channel isolation. Thus, the concept has to be investigated according to SNR degradation, when applied to RF signals with very large bandwidth (e.g., 25 GHz).

Acknowledgment

This work is supported in part by the European Union, Horizon 2020 research program, project 5G-COMPLETE, under grant agreement no. 871900 (modular baseband processing approach), and in part by the German Research Foundation (DFG), project PSSS-FEC, project no. 442607813, LO 2709/1-1 (PSSS-communication elements).

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