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Development of a 200 mm Wafer Silicon Nitride PIC Environment for Graphene Electro-Absorption Modulators

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Abstract

The demand for optical communication and data transfer is rapidly increasing, emphasizing the need for research on new materials and technology development in this field. This study describes the development of silicon nitride (SiN) grating couplers and waveguides on a 200mm wafer scale as a basis for the graphene-based optical modulators. The research presents results on the coupling efficiency and the influence of bottom and top cladding on the propagation loss of the light. This work is an important step for SOI free photonic-integrated-circuit (PIC) platforms and the development of high-speed, low-power and cost-effective communication applications.

1. Introduction

Graphene-based modulators have attracted significant attention in recent years due to their potential for high-speed and low-power operation, making them a promising candidate for use in optical communication and computing systems [1]. Graphene modulators are devices that modulate the intensity or phase of light using graphene as the active material. These modulators have the potential to revolutionize optical communication and computing systems due to their high speed, low power consumption, and compatibility with existing silicon-based technology. However, to realize their full potential, efficient light coupling and guiding is essential. By enhancing the coupling efficiency, these devices can achieve higher modulation depth, lower insertion loss, and faster switching speed. Thus, making them more competitive for use in optical communication and computing systems. This is where silicon nitride development comes into play. Silicon nitride is a widely used material in the field of photonics due to its excellent optical properties, including low optical loss, high refractive index, and compatibility with standard fabrication processes. SiN waveguides have an advantage over doped Si, as it does not require doping, and its refractive index is lower than that of Si. Moreover, SiN does not rely on SOI wafer substrates and could be flexibly integrated on various semiconductor substrates. Increasing the dimensions of the SiN waveguide material can increase the interaction between two graphene layers, and thus enhance light modulation. As previously mentioned, the refractive index of SiN is lower than that of Si, with n(SiN) being approximately 2 and n(Si) being around 3.8 [2]. This difference in refractive index results in a strong confinement of light propagation through the waveguide, leading to lower insertion losses. Additionally, SiN waveguides are less sensitive to edge roughness, which helps to achieve low propagation loss and are more tolerant for fabrication imperfections. For in- and out-coupling of light to the waveguide, the corresponding grating couplers are required. The period and etch depth of the grating couplers need to be optimized to enable efficient coupling to the waveguide.

This research introduces the key results of the development of SiN waveguide for the development of the dual graphene modulator on 200mm wafer compatible with front-end-of-line (FEOL) CMOS technology. The performance of grating couplers for operation in the O-band wavelength range will be discussed as well. Furthermore, the effect of bottom and top cladding on light propagation through the SiN waveguide will be presented.

2. Experimental Results and Discussion

Firstly, for the development of SiN waveguide, SiO_2 film, as a bottom cladding, was deposited by plasma enhanced chemical vapor deposition (PE-CVD). The thickness of SiO_2 layer was varied from 1200 nm to 2100 nm. The thickness range was based on the performed computational simulations for the operation at the wavelength of 1310 nm. Secondly, the 450nm SiN layer was deposited by PE-CVD at 400°C temperature. The patterning of the SiN waveguide by photolithography and reactive ion etch (RIE) steps were realized to form the core of the SiN waveguide (Fig. 1a). Following processing step was the deposition of 600 nm SiO_2 layer, which then was polished down to 410 nm during chemical mechanical polishing (CMP) process. For the top cladding the same PE-CVD SiO_2 films with the thicknesses in the range of 500-2000 nm were deposited.

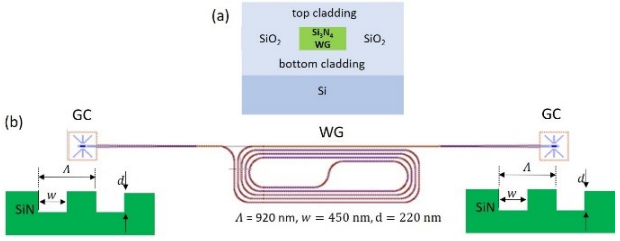

Fig. 1 (a) the schematic representation of cross-section of the SiN waveguide imbedded into SiO_2. (b) The design of 3 cm SiN waveguide and the corresponding grating couplers (GCs).

For the light to be coupled into the waveguide (WG) grating couplers (GCs) with the period of the Λ=920 nm and the etching depth of d = 220 nm were developed and realized

through a photolithography and RIE processing steps (Fig. 2).

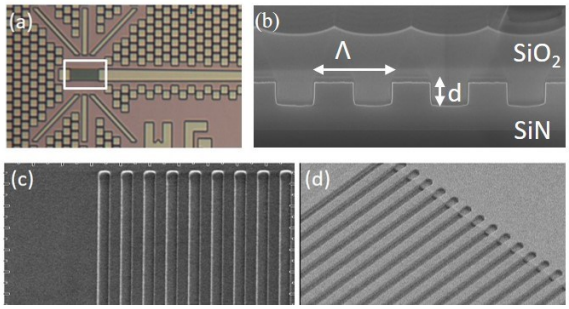

Fig. 2 The fabricated GC in SiN waveguide: (a) optical micrograph, (b) SEM cross section, with SiO_2 top cladding layer, (c) SEM top view, (d) SEM tilted view.

The main figure of merit, for characterization of waveguide functionality, is the insertion loss determined from the difference of light intensity/power between the incident and transmitted light.

In order to determine the possible influence of the thickness of bottom and top cladding material (PE-CVD SiO_2 in this case) the insertion loss measurements were performed on the waveguide test structures with the lengths of 1 cm, 2 cm, 3 cm and 6 cm (Fig. 3) [3].

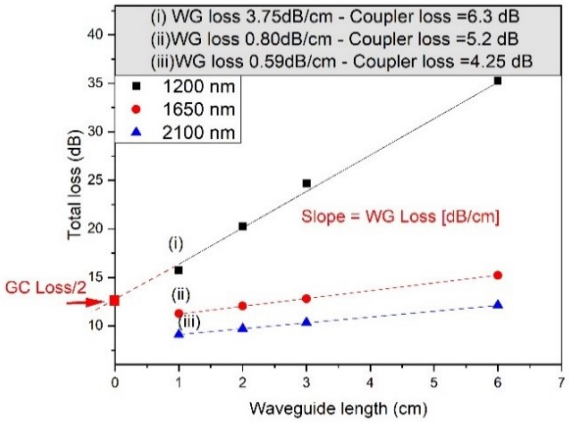

Fig. 3 The influence of bottom cladding on waveguide and grating coupler loss.

It was determined, that thicker bottom cladding of 2100 nm SiO_2 leads to lower loss of the waveguide. The insertion loss per grating coupler was determined from the intercept point in loss vs waveguide length dependence, while the slope was used to determine the insertion loss of the waveguide [dB/cm]. The best waveguide loss of 0.59 dB/cm and correspondingly 4.25 dB per grating coupler were measured for 2100 nm SiO_2 oxide used as bottom cladding. Whereas higher losses were obtained if thinner bottom cladding of 1200 nm or 1650 nm were employed in the stacking structure (Fig. 3).

The influence of top cladding was investigated for the SiO_2 thicknesses of 500 nm, 1200 nm and 2000 nm. The variations of waveguide and grating coupler loss on 200 mm wafer were 0.58-0.61 dB/cm and 4.16-4.47 dB, respectively. The thickness effect on WG and GC loss was not so significant in comparison to the bottom cladding effect. Despite the homogenous loss distribution over the wafer, the top cladding of 1200 nm resulted in the lowest values of 0.58 dB/cm and 4.16 dB for waveguide and grating coupler loss, respectively. The results are in the agreement with simulations which resulted in the coupling loss of 4.8 dB at 1310 nm (Fig. 4.).

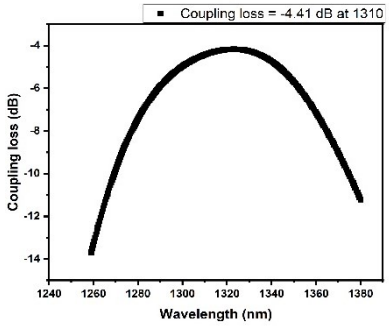

Fig. 4 The simulated coupling loss at 1310 nm wavelength.

The Fig. 5 shows the total propagation loss (loss per WG + 2 GCs) distribution over 200 mm wafer for 1 cm long WG. The standard deviation (1 sigma) of the obtained results is 0.22.

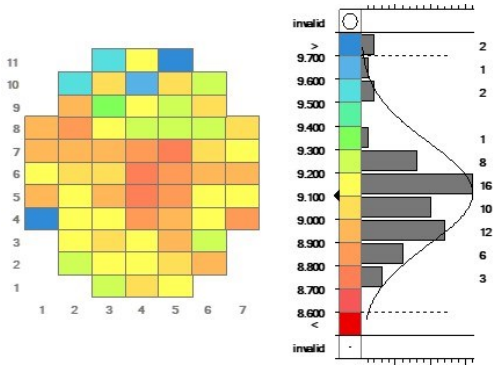

Fig. 5 The total loss distribution over 200 mm wafer.

3. Conclusions

In this research the SiN waveguide and grating couplers were developed for the application of graphene electro-absorption modulator in optical communication field. The lowest WG loss of 0.58 dB/cm and 4.16 dB per GC were obtained for the thicknesses of 2100 nm and 1200 nm used as bottom and top SiO_2 cladding, respectively.

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Acknowledgements

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References

[1] H. Agarwal, B. Terres, L. Orsini, A. Montanaro, V. Sorianello, M. Pantouvaki, K. Watanabe, T. Taniguchi, D. Van Thourhout, M. Romagnoli, F.H.L. Koppens, Nat. Comun. **12**, 1070 (2021).

[2] Z. Zhang, M. Yako, K. Ju, N. Kawai, P. Chaisakul, T. Tsuchzawa, M. Hikita, K. Yamada, Y. Ishikawa, K. Wada, Sci. Technol. Adv. Mater. **18,** 283–293 (2017).

[3] A. Peczek, Ch. Mai, G. Winzer, L. Zimmermann, 2020 IEEE 33rd International Conference on Microelectronic Test Structures (ICMTS), 1-3 (2020), doi: 10.1109/ICMTS48187.2020.9107905.