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Abstract

The reliable and compact modeling of RRAM devices is crucial for supporting the development of novel technologies including them. The latter includes a wide range of applications, such as in-memory computing in neuromorphic networks or memristive logic. A major advantage of the considered HfO2- based RRAM devices is their CMOS-compatibility, which allows them to already be utilized in present applications. However, one problem with RRAMs is that their fabrication still leads to device variabilities. This makes it challenging to test the functionality of aspiring technologies utilizing them in an experimental fashion. This work is dedicated to the compact modeling and efficient emulation of 1T-1R RRAM devices. Specifically, we aim to provide an enhanced model, based on the Stanford-PKU model, that can be used on any simulation platform such as SPICE, VERLIOGA, or even standard ODE solvers to simulate multilevel capable RRAM devices. Furthermore, we provide an algorithmic model, based on the wave digital concept, which allows for emulating the considered RRAM device in real-time. Using the latter, we show the hysteresis of our enhanced model to exhibit astounding resemblance with real device measurements.

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***Index Terms*—RRAM, 1T-1R, modeling, wave digital emulation, memristive systems, neuromorhpic**

***Abstract*—The reliable and compact modeling of RRAM devices is crucial for supporting the development of novel technologies including them. The latter includes a wide range of applications, such as in-memory computing in neuromorphic networks or memristive logic. A major advantage of the considered HfO_2-based RRAM devices is their CMOS-compatibility, which allows them to already be utilized in present applications. However, one problem with RRAMs is that their fabrication still leads to device variabilities. This makes it challenging to test the functionality of aspiring technologies utilizing them in an experimental fashion. This work is dedicated to the compact modeling and efficient emulation of 1T-1R RRAM devices. Specifically, we aim to provide an enhanced model, based on the Stanford-PKU model, that can be used on any simulation platform such as SPICE, VERLIOG-A, or even standard ODE solvers to simulate multilevel capable RRAM devices. Furthermore, we provide an algorithmic model, based on the wave digital concept, which allows for emulating the considered RRAM device in real-time. Using the latter, we show the hysteresis of our enhanced model to exhibit astounding resemblance with real device measurements.**

I. Introduction

Resistive Random Access Memory (RRAM) devices are two terminal devices with the capability of rapidly switching between several resistance states. This ability is attributed to their memory property, which relates to the formation process of a conductive filament [1]. These devices have been popularized over the recent years, as they have been shown to be suitable candidates for a wide range of applications [2]–[5]. In particular, they are well-suited for neuromorphic applications in which they are commonly used to mimic the behavior for biological synapses [6]–[8]. However, their fabrication is an ongoing topic of research, which still requires some time to reach a state of maturity [9]–[11]. In this context, device variabilities, such as device-to-device and cycle-to-cycle variabilities, are currently issues [12], [13] that hinder experimental pre-investigations of modern technologies with these devices. Moreover, RRAMs are gaining popularity mainly due to the possibility to monolithically integrate them within the CMOS process, which makes their reliable modeling essential for the majority of research that is oriented towards designing circuits including them. For that reason, a lot of work has been (and still is being) invested into the reliable and compact modeling of these devices, such that, to our knowledge, more than 10 different models have been developed to describe their dynamical behavior. A collective study discussing the similarities, differences, and features of many of these models has been recently carried out [14].

In this work, we aim to address three different problems, which we have observed in the context of modeling and simulating RRAMs with the well-established Stanford-PKU model [15]. First, we have noticed that simulations, which are purely based on the mathematical equations appearing in the said model, do not yield the desired hysteresis. This is because the model does not take the NMOS-transistor into consideration, which is a part of the 1T-1R architecture. Thus, we introduce modifications to the model, so it can be used on any simulation platform such as SPICE or even standard numerical integrators without having to use the NMOS-transistor. Second, the reset process of the Stanford-PKU model is very different from the one of the real device. In particular, the shift in the reset voltage that is exhibited by multilevel capable RRAMs has yet to be considered in the model. Therefore, we introduce a simple modification to the model, which brings the reset process much closer to that of the actual device. Third, while simulations might be useful for pre-investigating memristive circuits utilizing RRAMs, they tend to become very slow as the number of memristors increases. Furthermore, they do not allow tuning parameters during runtime and can not be used as placeholders for RRAMs in actual circuits for design purposes. For that reason, we introduce a software wave digital emulator. Wave digital algorithms are known for their massive parallelism, high robustness, and fault tolerance [16]–[18], which allows real-time capable emulation of large networks, even with memristors [19]. More details on this concept are given in section IV.

The remainder of this paper is organized as follows: We start with a description of the considered HfO_2-based RRAMs

in section II, where we explain the physical phenomenon behind their functionality. In section III, we introduce the modifications that we have made to enhance the baseline Stanford-PKU model. Section IV briefly recapitulates the wave digital concept and demonstrates the wave digital model used for emulation purposes, which yields the results presented in section V. Here, we also discuss the differences between our enhanced model and the baseline Stanford-PKU model and justify the modification that we have made. Finally, section VI gives a conclusion and summarizes the main contributions of this work.

II. Experimental Description

The RRAM devices under study are arranged in a one-transistor-one-resistor (1T-1R) structure. It consists of a NMOS transistor (1T) fabricated in the 130 nm CMOS technology node, connected in series to a metal-insulator-metal (MIM) stack with memristive features (1R). Fabricated on Metal 2 of the back-end of line (BEOL) of the CMOS process, the MIM integrates a TiN/Al:HfO_2/Ti/TiN stack in which top electrode (TE) and bottom electrode (BE) are both composed of 150 nm thick TiN layers deposited by sputtering. The $7\,\mathrm{nm}$ Ti layer was grown below the TE also by sputtering, acting as oxygen-scavenging capping layer that enhances the switching capabilities of the dielectric layer (i.e. retention, resistance window, switching speed) [20]. The insulator consists of a $6\,\mathrm{nm}$ Al-doped (about 10%) HfO_2 dielectric layer grown by atomic layer deposition (ALD). The MIM structures were patterned with an approximate area of $0.4 \mu\mathrm{m}^2$. To enable the switching properties of the active dielectric layer, it is necessary to carry out a forming procedure. This operation is performed by applying a positive voltage to the TE of the RRAM devices unchaining an electrical breakdown that moves the device from its pristine state to the low resistive state (LRS). With this initial step, a predominant conductive filament (CF) composed by oxygen vacancies is built for the first time, suddenly allowing the current flow through the 1T-1R structure. Consecutively, the device can be moved to the high resistive state (HRS) by means of the reset operation. This is achieved applying a negative voltage able to move the oxygen vacancies towards the TE, disrupting the main CF and creating the gap distance between the filament's tips. This process is reversible by means of the set operation. The latter consists of applying a positive voltage to the TE able to move the oxygen vacancies towards the BE re-building the CF and allowing the current flow through the device again (see Figure 1). The role of the NMOS transistor is not only to impose a compliance current level to protect the RRAM device against current overshoots when accomplishing the forming and set operations, but also to enable the multilevel-cell (MLC) [21]. Tuning the gate voltage of the transistor during the set operation allows modulating different current compliance levels to control the CF's conductivity. That is, the higher the compliance current imposed during the set operation the more conductive the LRS is. In this work, we target four different conductive levels, namely HRS, LRS1, LRS2 and LRS3, being LRS3 the most conductive state and HRS the highest resistive state. The three LRSs are programmed setting the gate voltage to $1.0\,\mathrm{V}$, $1.2\,\mathrm{V}$, and $1.6\,\mathrm{V}$ during the set operation. The HRS is achieved setting the gate voltage to $2.7\,\mathrm{V}$, which (maximally) reduces the series resistance of the NMOS transistor during the reset operation. For further experimental details, the interested reader is referred to [13].

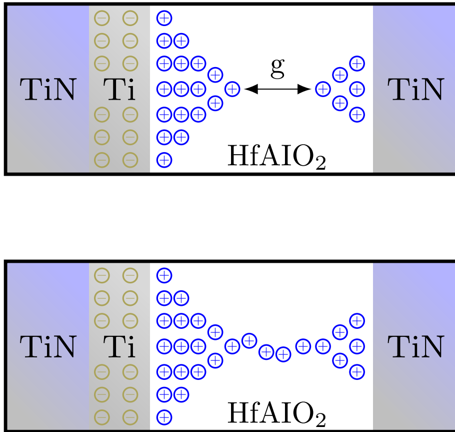

Fig. 1: A sketch of the HfO_2-based RRAM device and its gap distance in the high resistance state (top) and in the low resistance state (bottom). Here, g denotes the gap distance in the conducting filament, which is greater than zero in the high resistance state and equals to zero in the low resistance state.

III. Electrical Model

A prerequisite for wave digital emulation is the synthesis of a so-called reference circuit. The latter denotes the underlying electrical model, which is based on a physical or mathematical description of the considered circuit. In this section, we start by recapitulating a known model for describing multilevel RRAM devices and then demonstrate the modifications that we have made to obtain an enhanced model.

A. Stanford-PKU Model with Multilevel Capability

The Stanford-PKU model is a well-established mathematical model for the dynamical behavior of RRAM devices. The model attempts to describe the change in the device's gap distance $\mathrm{g}(t)$ depending on the voltage $u(t)$ across the device:

$$\dot{\mathrm{g}}(t) = -\mathrm{v}_0 \exp\left(-\frac{E_\mathrm{a}}{k_\mathrm{B}T}\right) \sinh\left(\gamma \frac{\mathrm{d_a}}{\mathrm{d_{ox}}} \frac{e}{k_\mathrm{B}T} u(t)\right) . \quad \text{(1a)}$$

Here, the gap distance is limited to be in the interval $\mathrm{g}(t) \in [\mathrm{g_{min}}, \mathrm{g_{max}}]$, where $\mathrm{g_{min}}$ and $\mathrm{g_{max}}$ denote the minimal and maximal gap distance, respectively. The constant E_a is the activation energy, k_B is the Boltzmann constant, $\mathrm{d_a}$ is the atom spacing, e is the charge constant, $\mathrm{d_{ox}}$ is the dielectric thickness, and v_0 is a velocity fitting parameter. The device temperature T is modeled to be a function of the dissipated power $p(t)$,

$$T = T(p) = T_0 + p(t) R_\mathrm{th} , \quad \text{with} \quad p(t) = u(t) i(t) , \quad \text{(1b)}$$

where T_0 denotes the room temperature, $i(t)$ is the current flowing through the device, and R_{th} is the device's thermal resistance. The variable γ is the field local enhancement variable that accounts for the material's polarizability depending on the current gap distance:

$$\gamma = \gamma(\mathrm{g}) = \gamma_0 - \beta \left[\frac{\mathrm{g}(t)}{\bar{\mathrm{g}}}\right]^{\alpha} . \tag{1c}$$

Here, γ_0, β, $\bar{\mathrm{g}}$, and α are all fitting parameters. Finally, the current flowing through the device is given by

$$i(t) = I_0 \exp\left(-\frac{\mathrm{g}(t)}{\mathrm{g}_0}\right) \sinh\left(\frac{u(t)}{U_0}\right) , \tag{1d}$$

where I_0, g_0, and U_0 are fitting parameters. For a better understanding of the role of all fitting parameters that have appeared up to this point, the interested reader is referred to [12], [15].

In [12], the classical Stanford-PKU model has been extended to incorporate the multilevel capability of modern RRAM devices. This is a method of controlling the low resistance state (LRS) in dependency of the gate voltage u_{g} of the NMOS-transistor. The latter sets the compliance current, which presumably, allows for a widening of the conductive filament with increasing drain current [12], [22], [23]. To take this phenomenon into consideration, the minimal gap distance is modeled to be anti-proportional to the applied gate voltage:

$$\mathrm{g}_{\min} = \mathrm{g}_{\min}(u_{\mathrm{g}}) = \frac{1}{E_{\mathrm{th}}} \frac{W/L}{u_{\mathrm{g}}} + \mathrm{d}_{\mathrm{th}} . \tag{2}$$

Here, W/L accounts for the aspect ratio of the NMOS transistor, while E_{th} and d_{th} are parameters of the 1T-1R device, to fit the model experimental multilevel measurements.

In the following section, we introduce a modified version of the Stanford-PKU model (with multilevel capability), whose dynamics is closer to those of the actual device. We would like to highlight the enhancements in the reset process, which we will show to be remarkably closer to the real device.

B. An Enhanced Memristor Model

In the following, we aim to mathematically describe a 1T-1R device as a general memristive system, see for example [24], [25]. To this end, we associate the gap distance $\mathrm{g}(t)$ with the unitless internal state of a memristive system:

$$z(t) = \frac{\mathrm{g}(t)}{\mathrm{g}_{\max}} , \quad \text{with} \quad z(t) \in [z_{\min}, 1] , \tag{3a}$$

$$z_{\min} = z_{\min}(u_{\mathrm{g}}) = \mathrm{g}_{\min}(u_{\mathrm{g}})/\mathrm{g}_{\max} . \tag{3b}$$

Here, we have normalized the gap distance, so the internal state $z(t)$ is limited to be between $z_{\min}$ and 1. The Stanford-PKU model describes the RRAM device as a voltage-controlled device, hence our model is that of a voltage-controlled memristive device,

$$i(t) = W(z,u)\, u(t) , \tag{3c}$$

$$W(z,u) = \frac{I_0}{U_0} \exp\left(-\frac{z}{z_0}\right) \mathrm{sih}\left(\frac{u}{U_0}\right) , \tag{3d}$$

$$\dot{z} = f(z, u, u_{\mathrm{g}}) , \tag{3e}$$

where we define $\mathrm{sih}(0) = 1$, otherwise $\mathrm{sih}(u) = \sinh(u)/u$ and $z_0 = \mathrm{g}_0/\mathrm{g}_{\max}$. The function $W(z,u)$ is the so-called memductance, which describes the conductivity of the device in dependency of the applied voltage and its internal state. The nonlinearity of the dynamical state equation is given by:

$$f(z,u,u_{\mathrm{g}}) = -\frac{\mathrm{v}_0(u,u_{\mathrm{g}})}{\mathrm{g}_{\max}} \exp\left(-\frac{E_{\mathrm{a}}}{k_{\mathrm{B}}T}\right) \dots \\ \sinh\left(\gamma(z,u)\frac{\mathrm{d_a}}{\mathrm{d_{ox}}}\frac{e}{k_{\mathrm{B}}T}\left[u - \mathrm{sgn}(u)\, u_{\mathrm{th}}\right]\right) , \tag{3f}$$

$$\mathrm{sgn}(u) = \begin{cases} 1, & u > 0 \\ -1, & u < 0 \\ 0, & u = 0 \end{cases} . \tag{3g}$$

Essentially, this equation corresponds to the baseline gap evolution equation (1a) of the Stanford-PKU model. However, we have now introduced a few changes. First, we have a threshold voltage u_{th}, which (uniformly) effects the device's switching behavior during the set and reset process. Furthermore, the velocity parameter v_0 is now a function of both the applied voltage u and the gate voltage u_{g},

$$\mathrm{v}_0(u,u_{\mathrm{g}}) = \mathrm{v}_0\sigma(u) + [1-\sigma(u)]\frac{\mathrm{v}_0}{\zeta^{\eta(u_{\mathrm{g}})}} , \tag{3h}$$

$$\eta = \frac{u_{\mathrm{g}} - u_{\mathrm{g},0}}{\hat{U}} , \quad \sigma(u) = \begin{cases} 1 , & u \geq 0 \\ 0 , & \text{otherwise} \end{cases} , \tag{3i}$$

where $\hat{U}$ is a voltage normalization constant, $u_{\mathrm{g},0}$ is a voltage fitting parameter, ζ is unitless fitting parameter, and $\sigma(\cdot)$ denotes the step function. This modification allows the velocity parameter v_0 to have different values during the set and reset process. Controlling the velocity parameter is essential for bringing the reset process of the model closer to that of the actual device. A similar modification is made to the field local enhancement variable γ, which is now a function of the applied voltage u in addition to the internal state,

$$\gamma(z,u) = \gamma_0(z,u)\,\sigma\left(\frac{1}{\hat{E}}\frac{\gamma_0(z,u)|u|}{\mathrm{d_{ox}}} - \frac{E_{\min}}{\hat{E}}\right) , \tag{3j}$$

$$\gamma_0(z,u) = \gamma_0\sigma(u) + \gamma_{\mathrm{r}}[1-\sigma(u)] - \beta\left[\frac{z}{\hat{z}}\right]^{\alpha} , \tag{3k}$$

where $\hat{z} = \bar{\mathrm{g}}/\mathrm{g}_{\max}$. Weighting the field local enhancement with the step function $\sigma(\cdot)$ ensures that the internal state z representing the gap distance only changes when the electrical field within the dielectric layer exceeds some threshold value $E_{\min}$. Here, we have normalized the argument of the step function by the constant $\hat{E}$. Moreover, the field local enhancement variable is now allowed to be different during the set and reset process, as can be verified from the definition of $\gamma_0(z,u)$. The variables γ_0 and γ_{r} denote the values of the field local enhancement variable during the set and reset process, respectively.

Now, we would like to briefly sketch the fitting methodology for the suggested model. Essentially, the fitting procedure is the same described in [12]. We suggest to start fitting the parameters for the lowest possible gate voltage, which corresponds to the lowest resistance state (LRS1), such that both the set and reset process fit the device's behavior. Here, we recommend using a constant velocity v_0, but a variable

field local enhancement variable $\gamma_0(z,u)$, just like in (3j). Once the optimal fitting parameters are found, one should then introduce a variable velocity parameter (3h) and fit the parameters ζ, $u_{g,0}$, and $\hat{U}$.

Basically, the changes introduced to the baseline Stanford-PKU model allow for dealing with the asymmetry of the memristive switching. The latter is especially noticeable in multilevel RRAM devices (with multiple low resistance states), which require a higher reset voltage, when their LRS is set to be smaller by the applied gate voltage. We would like to stress that the gate voltage should not be changed during the reset process, which is something that is usually applied in practice to minimize the resistance of the NMOS transistor [13]. This is because our model changes the velocity parameter in dependency of the gate voltage that is applied during the set process. If the gate voltage is changed during the reset process then the model forgets this information due to the static relation between v_0 and u_g in (3h), which would make the part of the hysteresis corresponding to the reset process to deviate from real measurements. The only way to remember the initially applied gate voltages would be by introducing another differential equation (i.e. a form of memory). However, this would convolute the model, which is why we prefer to avoid it.

IV. Wave Digital Emulation

HfO_2-based RRAM devices are generally inexpensive CMOS-compatible devices [13] making them quite attractive for neuromorphic technology [3]–[5]. In this context, their bipolar switching behavior can be especially useful for implementing synaptic learning [26], for example, by the mechanism of Spike-Timing-Dependent-Plasticity (STDP) [27]. However, the stochastic nature of these devices leads to noticeable behavioral variability, which can hinder pre-investigations of large circuits including them. For that reason, it can be beneficial to exploit mathematical models, like the one presented here, which can be embedded into different simulation environments. While simulations can indeed be quite useful for pre-investigating memristive circuits, their efficiency usually decreases as the number of memristor increases [28]. Therefore, we suggest exploiting the wave digital concept [18], which is a very powerful platform-independent tool for emulating the behavior of large electrical circuits. This statement is supported by the concept of multidimensional wave digital algorithms [16], which allows emulating many electrical components (even with different parameters) in a highly parallel fashion. For example, many wave digital algorithms have been proposed for mermristive circuits on graphs [29], one-port or two-port coupling networks (crossbars) [30], [31], and diffusively coupled oscillators (resistive or memristive) [19], [32]. Lastly, a major advantage of the suggested concept is its real-time capability, which allows implementing the associated algorithms on Application-Specific-Integrated-Circuits (ASICs) or Field-Programmable-Gate-Arrays (FPGAs) and using these devices to replace the actual memristors within the circuit. This allows the designer to let the considered circuits undergo experimental tests prior to their production.

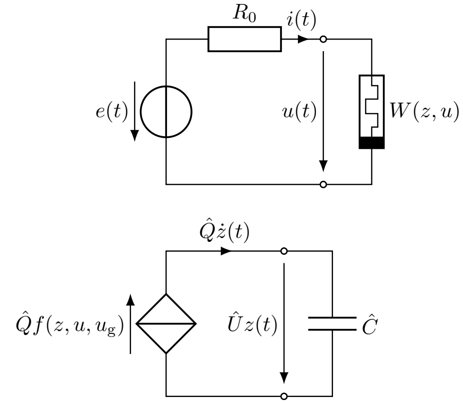

Fig. 2: Emulation scenario, where the bottom circuit represents a circuit-theoretical method of calculating the internal state. The constants $\hat{C} = 1\,\mathrm{F}$ and $\hat{Q} = 1\,\mathrm{C}$ are normalization constants with the unit of capacitance and charge, respectively.

To obtain a wave digital algorithm, one must transform a given reference circuit into a discrete model, a so-called wave flow diagram. This transformation preserves the energetic properties of the reference circuit, which, in particular, implies that passivity is carried over to the discrete model [17]. Another benefit, among many others, is the ability of parametric changes during runtime. This has allowed us to apply a live parameter fitting to obtain a suitable set of parameters for the considered device, cf. [33]. Now, transforming a given reference circuit into the wave digital domain means that the circuit must first be port-wise decomposed, where the following bijective mapping relation is applied to the resulting one- and multiports:

$$a = u + Ri \quad \text{and} \quad b = u - Ri\,, \quad \text{with} \quad R > 0\,. \tag{4}$$

Here, a and b denote the incident and reflected wave, respectively, while R is the so-called port resistance [18]. Reactive elements, such as capacitors or inductors, must first be discretized by means of numerical integration, commonly the trapezoidal rule [17], [18]. To test the enhanced model, we

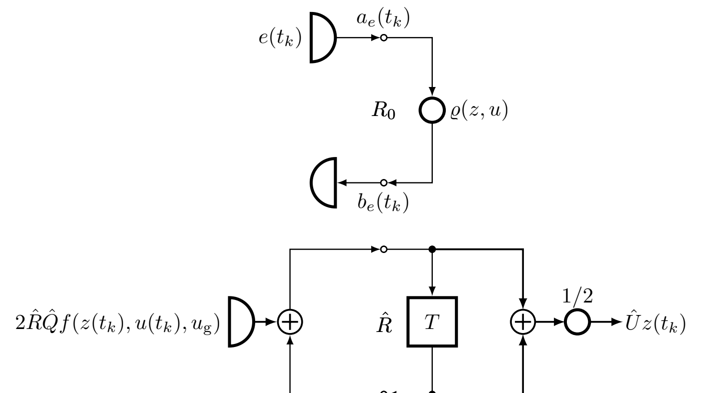

Fig. 3: Wave flow diagram corresponding to the scenario depicted in Fig. 2.

consider the emulation scenario depicted in Fig. 2. Here, we interconnect a real voltage source with the internal resistance

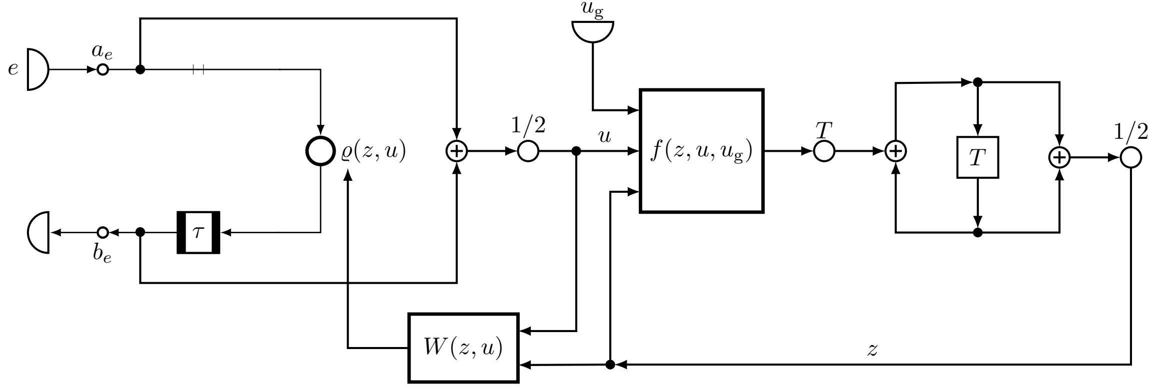

Fig. 4: Explicit wave flow diagram corresponding to the scenario depicted in Fig. 2 that deals with the numerical integration of the internal state as well as algebraic loops.

R_0 directly to the RRAM device, which is represented by the memristor with the memductance $W(z,u)$. The lower part of Fig. 2 demonstrates an electrical interpretation of an integrator, which is used to integrate the right handside of the state equation (3f). Considering the numerical discretization, which the circuit must undergo to obtain the associated wave digital model, we introduce a discrete time instant $t_k = t_0 + kT$, with $k \in \mathbb{N}$, reference time t_0, and sampling period T. The wave digital model corresponding to the considered test circuit is presented in Fig. 3. Here, the upper part results from the direct translation of the upper circuit in Fig. 2, i.e. the voltage source translates to a wave source supplying the voltage wave $a_e = e$, while the memristor translates to the reflection coefficient $\varrho(z,u)$. The lower part represents the numerical integration of the state equation by the trapezoidal rule,

$$\hat{U}z(t_k) = \hat{U}z(t_{k-1}) + \hat{R}\hat{Q}\dots \\ [f(z(t_k),u(t_k),u_\mathrm{g}) + f(z(t_{k-1}),u(t_{k-1}),u_\mathrm{g})] \,, \quad (5)$$

where $2R = T/C$. At first glance, the algorithm seems quite straightforward. However, one must consider the algebraic loops that arise due to the implicitness of the reflected wave b_e:

$$b_e = \varrho(z,u)a_e \,, \quad \text{with} \quad (6a)$$

$$\varrho(z,u) = \frac{1 - W(z,u)R_0}{1 + W(z,u)R_0} \,, \quad u = \frac{a_e + b_e}{2} \,. \quad (6b)$$

As can be seen b_e depends on itself due to the dependency of the memductance $W(z,u)$ on the voltage u. In the context of wave digital structures, this type of implicit relationship is usually referred to as an algebraic directed delay-free loop [34].

To resolve this loop, we make use of a fixed-point iteration, which corresponds to the strategic insertion of an additional delay in the wave flow diagram. A semi-explicit representation of the wave digital algorithm including the additional delay (designated with τ) is presented in Fig. 4. The representation is only semi-explicit, because it does not cover the calculation of the device temperature T and the field local enhancement variable γ, but rather summarizes their calculation into the block computing the right handside of the state equation. For more details on the evaluation of wave digital structures with fixed-point iterators, we refer the interested reader to [34].

V. Emulation Results and Discussion

The previously discussed wave digital model of Fig. 4 is now used to emulate the behavior of IHP's RRAM device, cf. [13]. Here, we used the parameters presented in [13] as a starting point towards finding new parameters for our enhanced model. The resulting set of parameters is given in table I. In

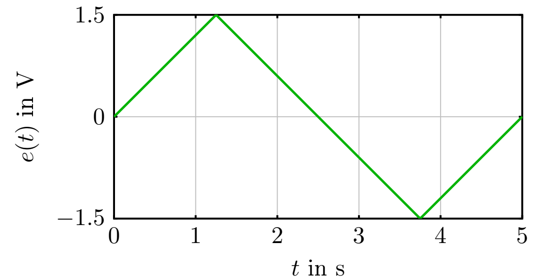

Fig. 5: Input signal $e(t)$ of the circuit in Fig. 2.

both the emulation scenario and the experiments, we applied a voltage sweep using the triangular-shaped input depicted in Fig. 5. Furthermore, all memristors were initialized with the initial state $z = 1$ corresponding to the high resistance state (HRS).

Our emulation results are depicted in Fig. 6. The left column presents results with the enhanced RRAM model, while the right column presents results with the baseline Stanford-PKU model using the parameters given in [13]. In every plot, we have drawn the (i,u)-curves stemming from 10 device measurement, the average of these measurements, and the (i,u)-curve of the new model. As can be seen from the left part of Fig. 6, the (i,u)-curves of the new model show an astounding resemblance to those of the real device. In particular, we would like to draw the reader's attention to the similarities in the reset process, which previously was a large discrepancy that has been pointed out in a previous work [13]. Here, we see that the model accurately captures the shift in

Physical Parameters				
$E_\mathrm{a} = 0.6\,\mathrm{eV}$	$e = 1\,\mathrm{eV}$	$k_\mathrm{B} = 1.38 \cdot 10^{-23}\,\mathrm{J/K}$	$\mathrm{d_a} = 0.25\,\mathrm{nm}$	$T_0 = 298\,\mathrm{K}$

Device Parameters			
$W = 150\,\mathrm{nm}$	$L = 130\,\mathrm{nm}$	$\mathrm{d_{th}} = 0.35\,\mathrm{nm}$	$E_\mathrm{th} = \frac{25}{13}\,\mathrm{V/m}$
$R_\mathrm{th} = 1500\,\Omega$	$\mathrm{d_{ox}} = 6\,\mathrm{nm}$	$E_\mathrm{min} = 1.4\,\mathrm{GV/m}$	$\mathrm{g_{max}} = 1.8\,\mathrm{nm}$

Fitting Parameters						
$U_0 = 0.45\,\mathrm{V}$	$u_\mathrm{th} = 0.31\,\mathrm{V}$	$u_{\mathrm{g},0} = 1\,\mathrm{V}$	$\alpha = 2.9$	$I_0 = 1\,\mathrm{mA}$	$\bar{\mathrm{g}} = 1\,\mathrm{nm}$	$\mathrm{g_0} = 0.285\,\mathrm{nm}$
$\beta = 4.25$	$\mathrm{v_0} = 0.01\,\mathrm{m/s}$	$\gamma_0 = 40$	$\gamma_\mathrm{r} = 26$	$\zeta = 70$	$\hat{U} = 0.2\,\mathrm{V}$	$\hat{E} = 1\,\mathrm{V/m}$

TABLE I: Physical, device, and fitting parameters of the modeled HfO_2-based RRAM device.

the device's reset voltage for different gate voltages. Large deviations between the enhanced model and the actual device can be observed for higher voltages after the set process. This is because we have not modeled the series resistance of the NMOS-transistor, which dominates the behavior of the device, once the memristor switches to a LRS. Essentially, the NMOS acts as a current limiter setting the compliance current. To model its effect, one could add a nonlinear resistor in series with the memristor, which describes the effective resistance of the NMOS in dependency of the gate voltage and the voltage across the device, see [25].

Now, looking at the right column of Fig. 6, we see that simulations, which are purely based on the baseline model, result in a much different hysteresis than that of the actual device. The same results were observed when simulating the model with LTspice and different ODE solvers. The difference in the width of the hysteresis is caused by the computation of the field local enhancement variable γ, which should only be different from zero, when the electric field exceeds the threshold E_min. However, even when we considered the latter, we obtained very sharp set and reset processes, which are impractical. These results have a very simple (mathematical) explanation: shortly before the set/reset process, the argument of the $\sinh(\cdot)$ function in (1a) is very large such that the time derivative of the state variable is also very large, which causes a rapid switching from the HRS to the LRS. For that reason, we introduced the fitting voltage parameter u_th, which mitigates the effects of the large argument causing a smoother transition from the HRS to the LRS. Since, the voltage offset should always minimize the function's argument independent of the voltage's polarity, we pre-multiplied the fitting voltage with $\mathrm{sgn}(u)$. Finally, to obtain a more similar reset process, we made the velocity parameter $\mathrm{v_0}$ dependent on the gate voltage applied during the set process. When the applied gate voltage is higher, the velocity parameter should become exponentially smaller. This results in a larger reset voltage and a smoother transition to the HRS.

VI. Conclusion

In this work, we have introduced an enhanced model and a wave digital emulator for mimicking the dynamics of multilevel capable RRAM devices. The Stanford-PKU RRAM model served as a basis for obtaining an enhanced model form RRAM devices. The latter was then used to derive a platform-independent and real-time capable emulator that can even replace the RRAM in actual circuits. Here, our goal is to support the design of circuits including RRAM devices. Finally, we have shown the new model to indeed be capable of mimicking the dynamics of RRAM devices in a more accurate manner. Contrary to the baseline model, we have shown that both the set and reset process are now much closer to that of the actual device. Furthermore, we extensively discussed why some modifications to the baseline were needed, so the model can be used on any simulation platform.

We would like to stress that the wave digital emulator is not restricted to a single device. In fact, one could use the proposed method to emulate a whole memristive network by using the methods discussed in [19], [30], [32]. This allows the efficient emulation of large memristive networks including RRAM devices with which we hope to support the development of aspiring computation technologies, such as neuromorphic computing or memristive logic.

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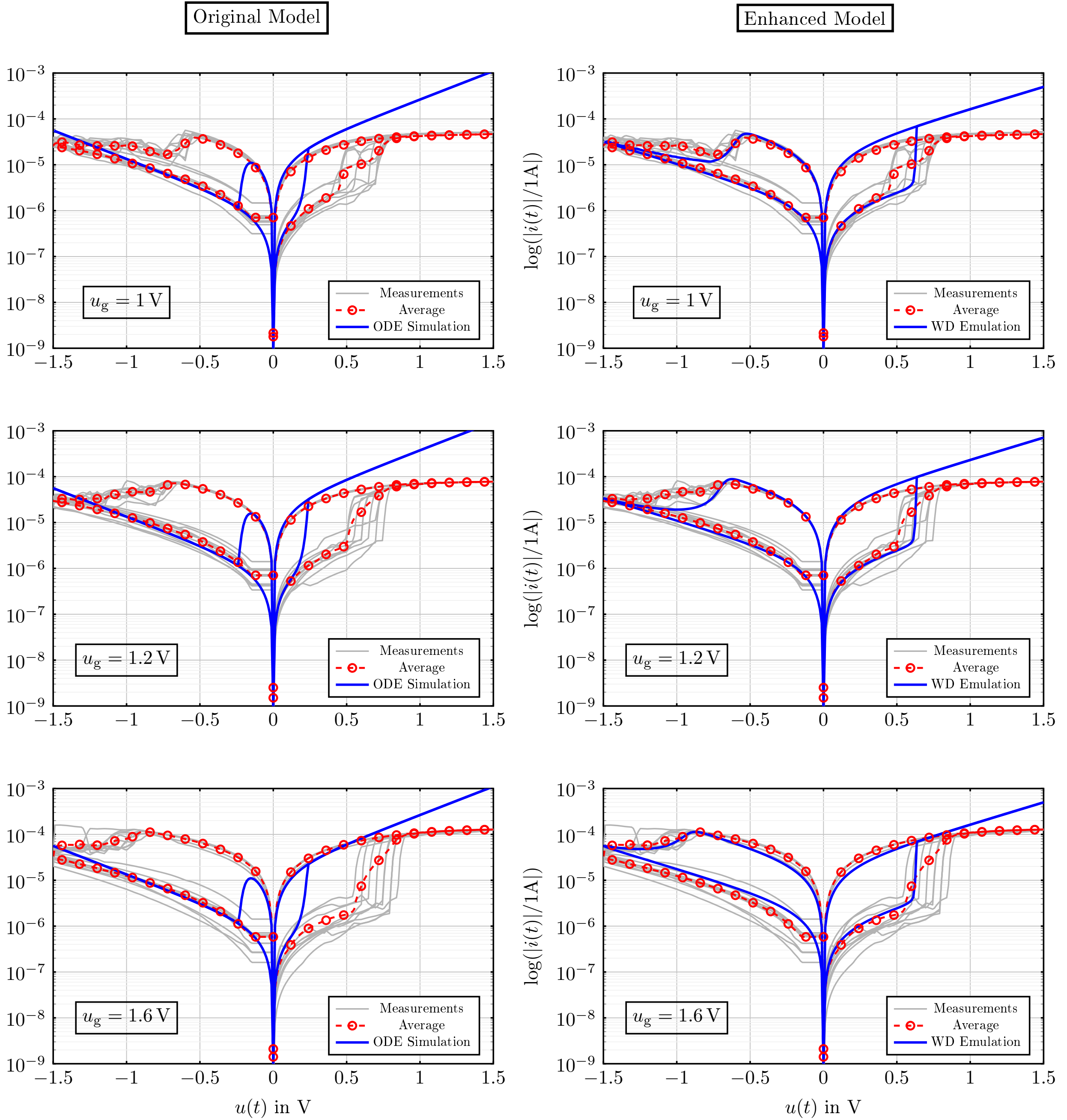

Fig. 6: Wave Digital (WD) emulation as well as ODE simulation results for three different gate voltages u_g using the enhanced RRAM model and the original model. Each plot depicts 10 device measurements (gray), the average of the 10 measurements (dashed red), and the results of the wave digital emulation (blue).

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