Fabrication of gate electrodes for scalable quantum computing using CMOS industry compatible e-beam lithography and numerical simulation of the resulting quantum device

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ABSTRACT

Universal quantum computers promise the possibility of solving certain computational problems significantly faster than classically possible. For relevant problems, millions of qubits are needed, which is only feasible with industrial production methods. This study presents an electron beam patterning process of gate electrodes for Si/SiGe electron spin qubits, which is compatible with modern CMOS semiconductor manufacturing. Using a pCAR e-beam resist, a process window is determined in which structure sizes of 50 nm line and 30 nm space can be reproducibly fabricated with reasonable throughput. Based on electrostatic simulations, we implemented a feedback loop to investigate the functionality of the gate electrode geometry under fabrication-induced variations.

Keywords: Electron beam lithography, quantum computing, Si/SiGe, quantum dots, CMOS, e-beam

Contents

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1. INTRODUCTION

Error-tolerant universal quantum computers promise to process some categories of problems exponentially faster and to simulate quantum systems with large Hilbert spaces. The base unit of a quantum computer is the quantum bit (qubit). There are several approaches to define the qubits, particularly by means of superconducting circuits, color centers, trapped ions, topologically protected systems and semiconductor quantum dots (QDs).[1,2] This paper deals with QDs in silicon, which are qubits defined by the single electron spin confined to the QD in a magnetic field.[3] Solving computational problems, which are currently intractable for classical super-computer, often require hundreds of error-corrected logical qubits represented by millions of physical spin-qubits each confined to a QD,[4,5] but only a six spin-qubit chip has been demonstrated in silicon as of yet.[6] Hence, scaling up the number and interconnectivity of qubits is the essential challenge. There are several device architectures of silicon quantum computers suggested,[7–11] but they all have a very high number of gate electrodes to be fabricated in common. Most current efforts for scaling up quantum chips are limited by the low-yield and low-throughput fabrication processes in academic cleanrooms. Therefore, the scaling up with good reproducibility and fabrication yield is only possible in a highly automated industrial semiconductor fabrication environment. Moreover, classical semiconductor circuits produced in this environment combined with the quantum chip signal enable the readout and reinforcement of quantum technology.[10,12,13] Therefore, scalable quantum computing architectures which are compatible with industrial CMOS (complementary metal-oxide-semiconductor) silicon foundries are necessary.[14]

Spin qubits in silicon are excellent candidates for large scale quantum computing for several reasons. QDs are extremely dense compared to other qubit platforms and thus offer the potential for millions of qubits on a chip.[10] Moreover, silicon quantum-chips are compatibile with mature semiconductor fabrication technologies. Isotopically purified nuclear-spinless ^{28}Si is an excellent host material for spin qubits, for its weak hyperfine interaction and low spin-orbit coupling that reduce coupling to a noisy environment.[3,15] Consequently, silicon-based electron-spin qubits show single- and two-qubit gate,[16–21] as well as readout[22–24] fidelities reaching the prerequisite for topological quantum error correction.[20]

The most common approaches for Si-based qubits[25] are Si/SiGe heterostructures, planar metal oxide semiconductor (MOS) devices, fully depleted silicon-on-insulator (FDSOI) devices, and donors in purified silicon.[26] In Si/SiGe heterostructure spin qubits, electrons are vertically confined in a tensile-strained and isotopically purified ^{28}Si layer, which is epitaxially grown between two layers of SiGe. Lateral QD confinement is done by planar gate electrodes. Compared to MOS and FDSOI, Si/SiGe heterostructures ensure improved control as the upper SiGe layer separates the QDs from the defect-rich semiconductor/oxide interface.[11]

Semiconductor spin qubits have many similarities to scaled transistors and hence are advantageous for the integration into the semiconductor manufacturing process technology. There are approaches using all-optical[27,28] as well as e-beam "mix and match" lithography[29,30] integration approaches. E-beam lithography provides high resolution and flexibility of the exposed pattern, because no mask is required, unlike for optical lithography. In this paper we propose an e-beam lithography approach for Si/SiGe qubits which is compatible with a 200 mm industrial CMOS semiconductor manufacturing line.

In most studies on Si/SiGe heterostructures for qubits, the gate electrodes are fabricated using academic e-beam lift-off nanostructuring. This fabrication technique suffers from low yield, poor uniformity, high particle load and hence is not applicable on an industrial scale.[31–38] In this study we apply subtractive electrode fabrication, using plasma etching, which is common for industrial CMOS fabs.[39] Our work is process-oriented and dedicated to the CMOS compatible gate electrode fabrication process and electrode geometry for Si/SiGe qubits, which has not been described in detail before.

The geometry and dimensions of gate electrodes needed for semiconductor QDs vary depending on the applied semiconductor host material and working principle of the electron confinement. To make the quantisation of the electron number in a structure measurable, the spatial confinement of an electron must lead to a level splitting larger than the thermal energy and strong enough to prevent several minima to form due to disorder. Both criteria favor a small effective electron mass. For planar silicon devices having strong confinement in the

crystallographic (100) direction (growth-direction of the Si/SiGe heterostructure), the relevant effective mass is 0.19 m_0, where m_0 is the free-electron mass.[3] The critical feature parameters differ between Si-MOS and Si/SiGe qubits: the closer proximity of the inversion-layer to the gate electrodes in Si-MOS results in typically sharper potentials and stronger disorder. Tunnel-coupling between QDs, which is at the heart of 2-qubit manipulation, thus requires very narrow gates. In many devices this is not achieved and consequently devices lack control of the tunnel-barrier.[40] In Si/SiGe heterostructures, on the other hand, the 30 nm to 50 nm SiGe spacer-layer leads to a widening of the QD potentials.[3] Since this effect limits the sharpness, a reduction of the gate widths below approx. the thickness of the spacer and oxide yield no further advantage. Hence, in this work we optimise the lithography fabrication process targeting a gate electrode width of 30-50 nm, and a pitch which is feasible for e-beam nanostructuring, etching and consequent top gate material deposition. In general the gap between the gate electrodes shall be as small as possible to have good electrostatic control, to screen oxide defects and to achieve higher orbital splitting of the QDs.

In summary, this work is focused on the setup of a CMOS industry compatible e-beam lithography fabrication approach of the gate electrodes for Si/SiGe heterostructure spin qubits. The gate electrode width should range from 30 nm to 50 nm. The distance between the electrodes should be as small as possible from the processing point of view (e-beam lithography process, and consequent etching, gate oxide and self-aligned TiN gap filling). Sections 2.1 and 2.2 show the desired device and electrode geometry, as well as process flow. Section 2.3 describes the CMOS compatible e-beam lithography process applied for the patterning of the gate electrodes. In the results section, Section 3, we first describe the feasibility and overall process window of the e-beam nanostructuring process targeting the 30-50 nm line width and smallest possible pitch. Secondly the obtained knowledge about the lithography process window is applied for further process optimisation to fabricate a specific gate electrode geometry, as described in 2.1. Finally, electrostatic control of QD occupation, tuning tunnel-barriers and robustness against fabricational imperfections are simulated by a finite-element COMSOL model of the device.

2. MATERIALS AND METHODS

2.1 Gate electrode geometry for qubits

The gate electrode arrangement is shown in Fig. 1 a). In addition to the first, structured gate layer, a second metal layer is self-aligned to the first. The inner gates are fanned out to form pads that are later contacted by a higher metal layer (not shown in this picture) using vias. Four channels are formed in the direction of the implanted areas, which are controlled in the final device by additional accumulation gates in a higher layer. The main region of interest for this study is shown in Fig. 1 b) and contains the elements with critical feature size as well as larger gates that have an influence on the e-beam exposure via proximity effects. The active qubit region is shown in Fig. 1 c). It consists of two sets of five (or three) fine gate electrodes separated by a separation gate. Each adjacent set of three fine gates can form a quantum dot. Here, each QD can either be operated in transport mode as a charge-sensitive single-electron transistor (SET) or successively emptied down to the last electron, thus functioning as a qubit. The device is then operated by forming a SET on one side of the separation gate and a qubit on the other side, as exemplified by the red/green dot. Both quantum dots are capacitively coupled, which enables the electron occupation of the qubit-dot to be read out by the SET.
Furthermore, the five fine gates can be used to form two coupled qubit-dots on one side. This allows all the basic functinalities of a qubit (initialisation, readout, single/two qubit gates). The formation of SETs and qubit-dots at different positions, as highlighted by the dashed circles, allow to draw conclusions about the reproducibility of the gate electrodes and the homogeneity of the underlying heterostructure.

2.2 Fabrication process of gate electrodes

Fig. 2 represents the scheme of the fabrication flow applied in this study. Operational blocks, which are not part of this study (e.g. implantation/annealing of ohmic contacts, etching of a mesa, ...) are omitted in this Figure. The incorporated Si/SiGe heterostructure is isolated by an CVD deposited silicon dioxide (SiO_2) layer. Afterwards, a global titanium nitrate (TiN) layer and a sacrificial hardmask are deposited. This is covered with a chemically amplified resist with positive tonality (pCAR) and patterned via electron beam lithography. Using a pCAR the written line ends up as a space in resist after development. Afterwards, the resist mask is transferred

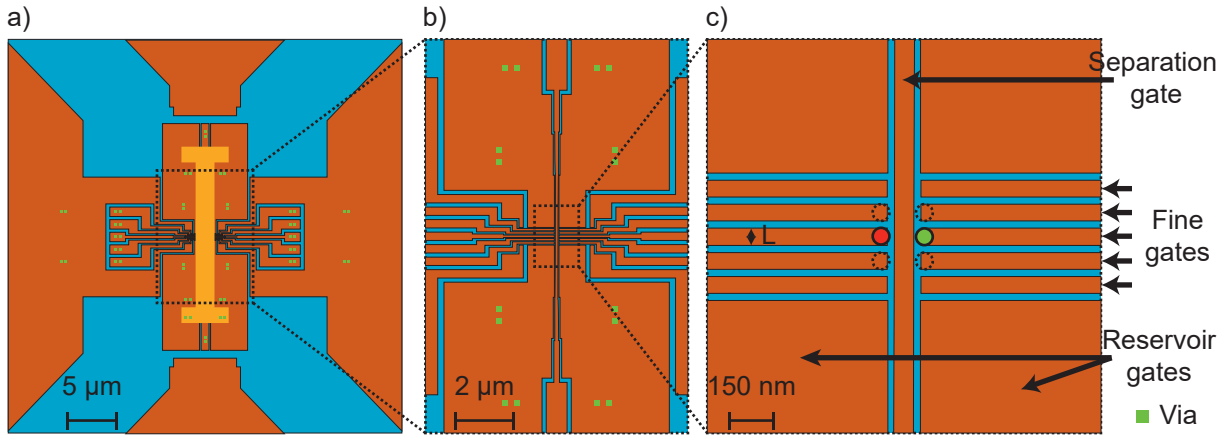

Figure 1. Studied gate layout with different zoom-ins: a) Gate fan-out up to pads designed to be contacted by higher metal layers later in the fabrication process (orange) with vias indicated as green squares. The second, self-aligned gate layer is highlighted in the middle of the image for improved visibility. b) Zoom-in with focus on the large area metal pads in close proximity to the active qubit region. The second gate layer is omitted to reveal the structure of the gates. c) Further zoom-in on the active qubit region, showing the two sets of five fine gates, separated by an additional gate and the four reservoir gates. As an example, a possible position of a SET (red) and that of a qubit dot (green) is shown. These can also be formed as desired at the dashed positions.

into the hardmask, which is subsequently used to pattern the TiN by reactive ion etching (RIE). This etching step introduces an etching bias ΔS, widening the spaces, which is used to adjust the final gate geometry. The deposited SiO_2 layer in the opened section acts as etch stop. The potentially damaged oxide is successfully removed in a further RIE step, followed by the conformal deposition of a second SiO_2 layer. A second TiN layer finally forms the self-aligned second gate layer.

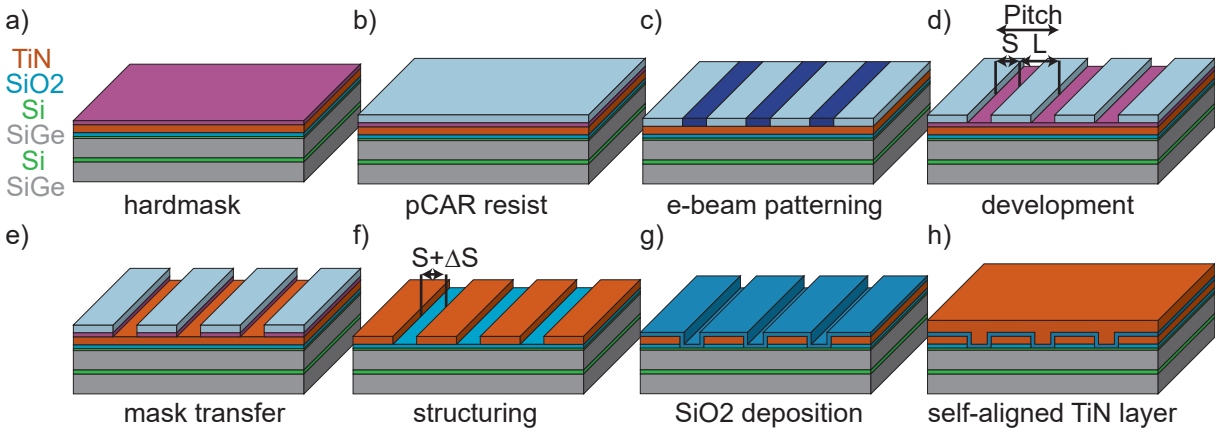

Figure 2. Process flow for device fabrication: a) The heterostrucutre is isolated by depositing SiO_2. On top of this, a global TiN layer G1 is deposited and capped by an sacrificial hardmask. b) The e-beam resist is spin coated on the wafer and c) subsequently patterned. d) After development, the written structure is transferred into the hard mask by reactive ion etching (RIE), f) which is afterwards used to pattern the TiN layer beneath, stopping at the SiO_2 layer. g) The potentially damaged oxide is successfully removed in a further RIE step, followed by the conformal deposition of a second SiO2 layer. h) A second TiN layer G2 finally forms the self-aligned second gate layer.

2.3 Electron beam lithography

For scaling up of the number of qubits a reliable, defect free, high-resolution nanopatterning process is indispensable. Furthermore, the process should be CMOS compatible, which implies among others strict metal

Table 1. Experimental details of the industry compatible nanopatterning process applied in present study, in comparison to the lab scale processing of the gate electrodes, taken from.[41]

	Lab scale e-beam nanostructuring	CMOS compatible e-beam nanostructuring
Patterning process	Additiv (lift-off)	Subtractiv*
e-beam Tool	Gaussian type Raith, 5200	VSB type Vistec SB3050DW
Beam shape	Gaussian	VSB
Resist type	CSAR	CAR, positive
Developer	AR 600-55 (MIBK Basis)	TMAH
Dose µC/cm^2	800 (extremely high to get good LER)	90
e-gun acceleration voltage kV	100	50
Beam current	150 pA / 3 nA	20 µA
Beam size	<5 nm	4 µm^2
Wafer size	6" Wafer	12" for the investigation of the proces window and stability, 8" for device fabrication

*CMOS compatible

contamination limits, no particle contamination and high throughput. Table 1 summarises the main characteristics of the CMOS industry compatible e-beam lithography system applied in this work. In comparison, an example is given of an e-beam device used in academic research, which was used to fabricate a structure for shuttling single electrons in conveyor-mode.[41]

An important aspect of the lithography process in our work is the application of CMOS compatible chemicals. CMOS compatibility defines weather the process or material is suitable for the standard CMOS semiconductor manufacturing. This definition implies many factors, for example low annealing temperatures to prevent dopant redistribution in the transistors or using specific materials to avoid any defect formation. All materials circulating in the semiconductor CMOS fabs should meet the specification of the maximum allowed element concentrations. Such resist, as well as developer and solvent which meet the CMOS requirements, are also used in this study.

CMOS compatibility also means minimal particle contamination on the wafer surface. The main issue with lab scale lift-off processes is the high particle load and low reproducibility, which are avoided in our work by application of a subtractive etch defined process. Additionally, the e-beam tool (Vistec SB3050DW) is constructed with fully automated wafer handling and alignment systems. This minimises the human contact with the wafers to be exposed, and reduces the time consuming manual handling. Fig. 3 shows fidelity and reproducibility of the 100 nm line/space (L/S) pattern exposed with e-beam over a 300 mm wafer. The measurement was done on structured resist with a CD-SEM tool from Applied Materials (Verity 4i).

The high throughput of our nanopatterning process (compared to other e-beam techniques) is further supported by the variable shaped beam (VSB) principle. The VSB tool has fixed shaped apertures defining the electron beam so that the actual pixel exposed onto a wafer is not a single Gaussian beam of tiny size, but a large beam which fills a particular shape of the exposure pattern (max. shot size 1.6 µm). As a result, the whole wafer with 232 chips containing support structures and 11 quantum devices per chip with an overall exposure area (Fig. 4 a)) of 1358.36 mm^2 requires around 13 hours of e-beam exposure time with the used system. The exposure time for one quantum device with an area of 0.036 mm^2 (see Fig. 4 c)) is just 2 seconds, as calculated from the exposure time for all quantum devices (2 h 23 min) divided by the 232x11 quantum devices per wafer.

Exposure time is also saved due to the application of CAR. CAR contains a photoacid generator (PAG). PAG exposed with electron beam produces protons H+. Each generated proton acts as a catalyst and initiates the avalanche of the consequent reactions of deblocking the resin from the large organic radicals, making it soluble in the aqueous developer. Hence CAR requires significantly lower exposure dose and time than nonCAR due to the impact of PAG.[42]

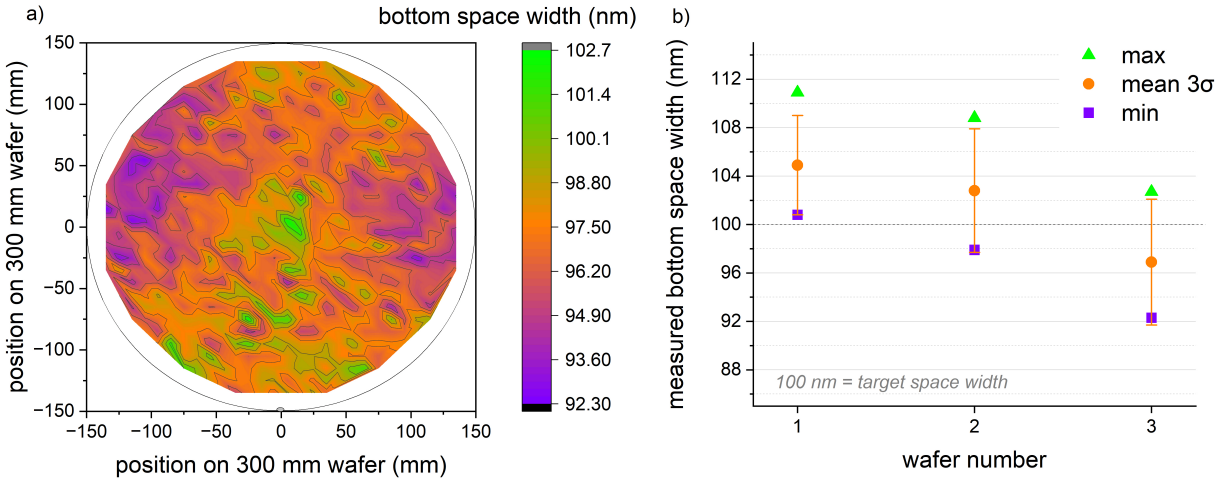

Figure 3. Parameters of the process stability on 300 mm wafers - pattern fidelity, uniformity and wafer to wafer reproducibility. Distribution of a 100 nm trench width with pitch 1/1 a) measured with CD-SEM over the 300 mm wafer b) for three different wafers.

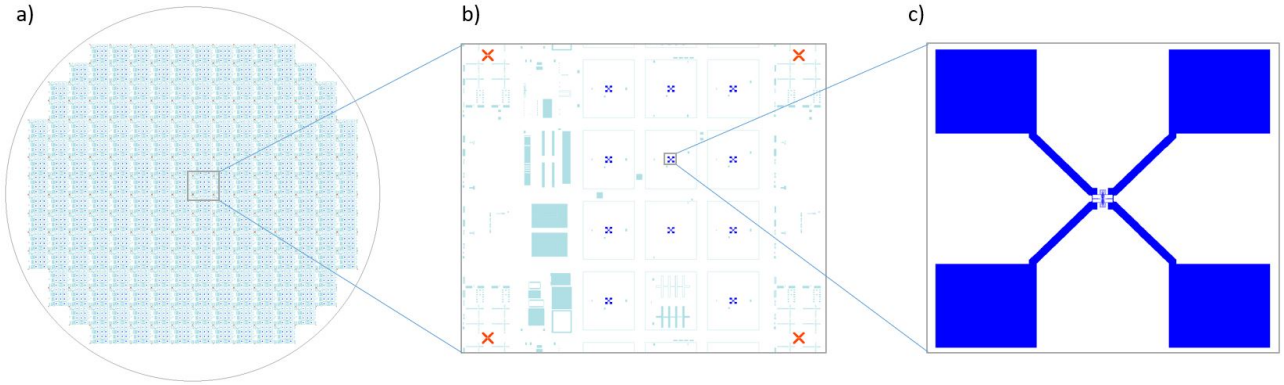

Figure 4. a) Wafermap - arrangement of the 232 chips on a 200 mm wafer, b) layout exposed by e-beam lithography on one chip 1 mm x 1 mm, containing support and device structures, c) layout of the device with four contact pads and gate electrodes in the middle. For further zoom in see Fig. 1.

Besides sufficient throughput and CMOS compatibility, the fabrication of a high numer of gates electrodes for qubit control requires high spatial resolution. This is realized by the specific properties of CAR resists, together with the low resist thickness (ca. 70 nm).

It is also worth mentioning, although not in the scope of this paper, that an optimised resist processing including coating, adhesion, development condition as well as pre and post baking are crucial for the lithographic step.

Last but not least, Proximity Effect Correction (PEC), which is described in detail in reference,[43] plays an essential role in the spatial resolution and pattern quality.

3. RESULTS AND DISCUSSION

3.1 Exploration of the e-beam patterning parameter space

In this part we describe the investigation of the e-beam lithography process window to find a stable and reproducible working window matching the desired gate size around 30-50 nm and smallest possible space in between. For precise illumination of the e-beam lithography process window under optimised conditions, we exposed a

special layout matrix, containing variation of line (bar) and space (trench) - (L/S) dimensions: space varies from 20 nm to 50 nm, and L/S ratio varies from 0.5 to 20, as shown in Fig. 5. The space dimensions after the resist development step were systematically measured by CD-SEM.

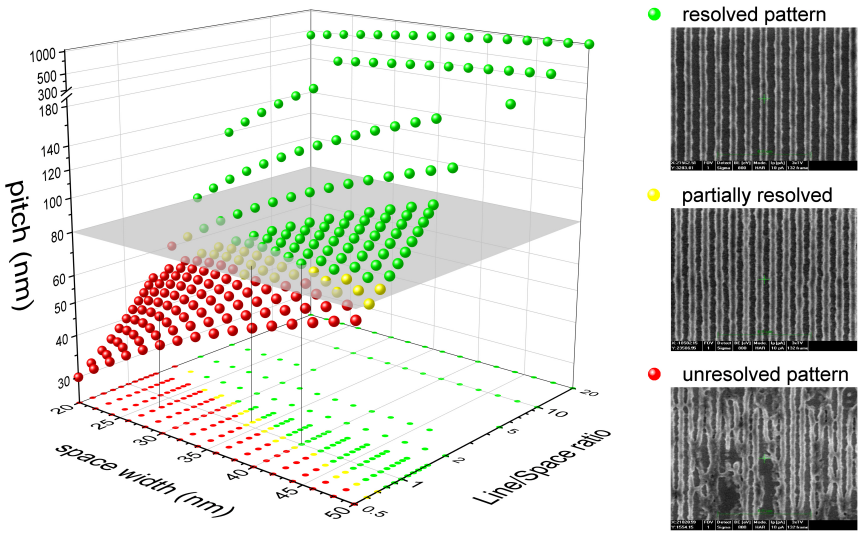

Figure 5. Lithography process window obtained after evaluation of the systematic CD-SEM measurement of the space width (trench width) in the resist mask on the gate stack for various L/S dimensions. The colours represent the quality of the pattern. Grey surface represents the transition region around pitch of 80 nm from unresolved to resolved L/S combination. Three CD-SEM images show examples of L/S pattern in resist.

The results of the CD-SEM measurements are shown in Fig. 5. The pattern quality, given by the color of the data points, is shown in dependence of space width, line/space ratio and pitch. Green represents a stable fidelity for this space - pitch combination even with ±5% exposure dose variation. Yellow indicates that the pattern fidelity is given at least under best dose condition. A deviation of the exposure dose might lead to bridging between resist structures (under exposure) or pattern collapse (over exposure). Red shows that there is no possibility to resolve this space – pitch variation in the chosen resist.
From the matrix in Fig. 5 one can see that at L/S ratio of 1 the space down to a 40 nm can be achieved, resulting in 80 nm pitch. The smallest S in our investigation is 20 nm. But to resolve this space a L/S ratio of at least 3 is required. That means that to ensure proper resolution, the distance between the 20 nm trenches should be at least 60 nm, corresponding to a pitch of 80 nm. When we bring the spaces closer to each other the L/S ratio is getting smaller and pitch decreases. For 30 nm spaces the smallest possible L/S ratio is around 1.7. So the minimal possible bar between the 30 nm trenches is around 50 nm. This is close to the desired gate electrode width. In general one can conclude that the L/S ratios and trench width combinations that result in a pitch of 80 nm or more achieve resolved patterns. (see Fig. 5 the 80 nm pitch is marked with the grey surface cutting the plot).

For proof of pattern stability, Fig. 6 a) shows the fidelity of the resist pattern within a small exposure dose variation. If the pattern is stable when varying the dose in the range of ±5%, a certain amount of deviation in pattern dimensions will not result in a damage of the resist structure. This is visible in Fig. 6, where all points are acquired by CD-SEM measurement on well resolved patterns. The deviation from the target value at nominal dose of 90 $\mu C/cm^2$ is not higher than 2.2 nm for all structure types. It can be concluded that the pattern is stable in case of some process instabilities (for example dose or resist thickness fluctuations). Good pattern fidelities for various pitches also show that the proximity effect correction is well adjusted and correctly compensates electron scattering effects. However, it should be taken into account that at 5 % dose variation the space width may be affected by 4-6 nm.

Fig. 6 b) jumps ahead and shows the same dependence as 6 a), but for the various gate electrode geometries. In this case the size of the resist pattern decreases at higher dose because the line width was measured with

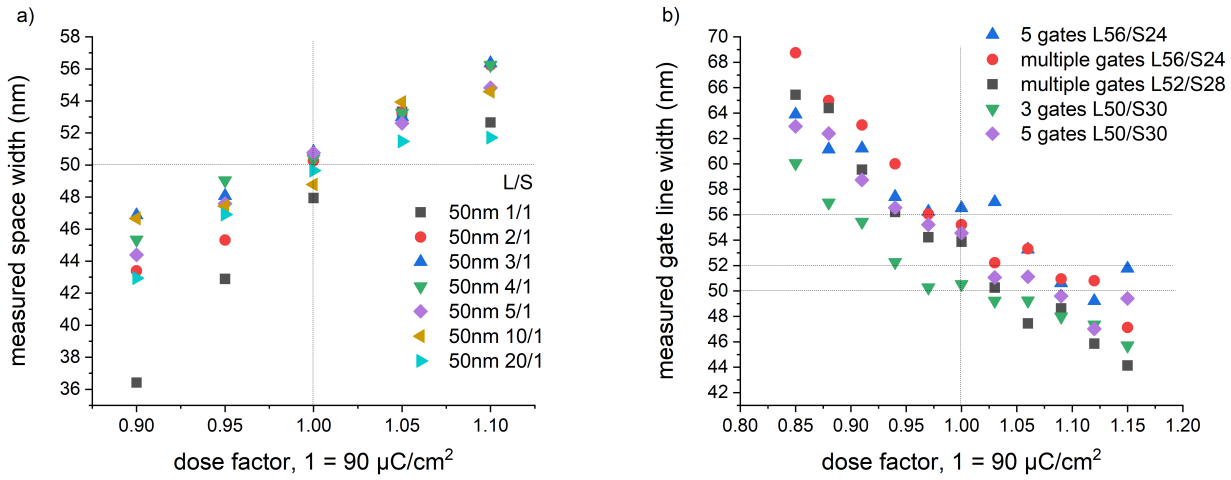

Figure 6. Dependence of the resist pattern width measured with CD-SEM on the applied e-beam exposure dose. a) 50 nm target space width (trench width) with various pitches L/S from 1/1 to 20/1. b) Gate line width (bar width) with various electrode number and L/S dimensions.

CD-SEM unlike plot a), where the space width was measured. So, the width of resist trench increases a) and the width of resist bar decreases b) at higher dose. Nonetheless, also in b) we observe that a variation of the exposure dose in the range of 5 % causes variation of the gate width from 2 to 6 nm, depending on the geometry. Fig. 6 b) reveals that the width of three finger gate electrodes reacts differently than five- and multiple finger. This is the effect of electron scattering from the neighborhood, which is different for these patterns: a three finger structures are subjected to more scattering effects from adjacent exposed areas and hence result in narrower measured resist bars.

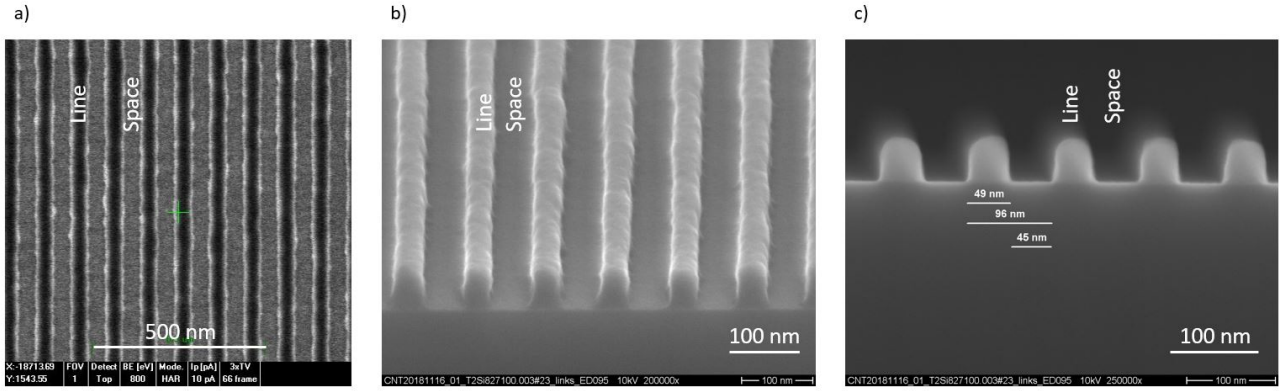

Figure 7. 50 nm L/S pattern in resist with pitch 1/1, a) top view, field of view FOV 1 µm mesured with CD-SEM, b),c) tilted and cross section view correspondingly measured with SEM S5000 from Hitachi.

To verify the reliability of the CD-SEM measurement, the cross section of the 50 nm L/S=1 resist pattern was acquired by SEM. Fig. 7 presents the top view CD-SEM image and SEM images of the 50 nm resist lines cross sections. The cross section SEM measurement (Fig. 7 c)) is in a good agreement with the space values measured by CD-SEM (Fig. 6 a)). From the cross section one can observe that the resist thickness is lower than 70 nm. However, the cross-sectional SEM method is not reliable enough for measuring resist thickness because the resist material is shrunk by the electron beam during SEM measurement. The ellipsometer measurements of the resist thickness over the wafer showed 70 nm thickness, and after resist development the thickness reduced to 67 nm. The dark erosion of the applied resist is around 3 nm. The measured with CD-SEM line edge roughness LER of the resist lines on their bottom revealed 3 nm.

Summarising this part, with application of given resist and optimised processing conditions the target gate width of 50 nm can be reliably achieved at the pitch of at least 80 nm and above. Hence, the minimal possible space between the 50 nm gate electrodes is 30 nm. It should be considered that after etching the gate width slightly reduces due to the etching of the side walls. So the distance between the gates (space) is getting correspondingly wider after etching (see also Fig. 2 ΔS). This aspect will be discussed in the following section in detail.

3.2 Exploration of the optimal gate electrode geometry

In this part the lithography process is further optimised for specific gate electrode geometry with around 50 nm gate electrode width and pitch of 80 nm.

Following parameters of the device geometry were considered during the study: exposure area around the gate electrodes, gate electrodes width and space in between, gap distance from the gate electrode to the separation gate and 3D gate electrode shape after etching.

E-beam exposure area around the gate electrodes It was observed that the quality of the gate electrode structures in resist is vastly affected by the area exposed close to them. Fig 8 shows the comparison of the two layout variants: a) complete area around the electrodes is exposed, b) just to the area which is needed to electrically isolate the electrodes is exposed, so the remaining resist after development can be seen in the SEM images. Exposed area without resist will be free of TiN layer after etching. So, in case of a) the electron backscattering has larger impact as compared to b) due to the larger exposed surface. This is directly reflected on the process window as can be seen in Fig. 8. As described in the previous section green framed images are well resolved and CD is on target, even at slight dose variations. Yellow framed images show the resolved, but unstable at slight dose variation, or partially collapsed pattern. Finally red frame means unresolved region. Consequently, variant b) is selected for further experiments because it provides a wider process window. This does not limit the qunatum device performance as the exposed area would have otherwise been covered by the self-aligned second metal layer. Moreover, by adding unique contacts to the metal plates, a greater flexibility for device tuning can be achieved this way.

Gate electrode width and space in between Fig. 8 presents the influence of the gate electrode width and space in between, which were varied keeping the pitch of 80 nm constant. It is observed, that at constant pitch the width of line and space defines the pattern quality: The thinner the line (gate electrode width) the worse is the pattern, i.e. it collapses. At a line width of L=38 nm (Fig. 8 b)) one can observe a pattern collapse, and at a line width of L=60 nm the pattern looks stable and smooth. The transition point is around dimensions of L=50 nm and S=30 nm. This result is in agreement with the results obtained from the test pattern described in the previous section. Fig. 9 presents the fidelity and wafer to wafer repeatability of the three-gate a), and five-gate b) electrode structure with L/S 50nm/30nm after resist development. This result shows that the gate width deviation after the lithography processing can vary in the range of ± 3 nm.

Distance from the gate electrodes to the separation gate Besides L and S, the gap distance from gate electrode to the separation gate and the separation gate width are essential for the device performance. On the other hand, these values are not restricted by the lithography process and can be chosen more flexibly. One should only take into account that, when electrodes are too close to the separation gate (< 14 nm), they may start to merge. Therefore, the distance was chosen based on simulations to ensure a robust formation of quantum dots (QDs) (see Sec. 4 for the information about the optimal gap distance, as well as about the separation gate width).

Geometry of contact lines and pads Besides gate electrode geometry, we also adapted the shape of contact lines and pads. The common contact geometry applied for the Gaussian type e-beam in the lab scale is not perfectly applicable to the VSB-type e-beam tool. As indicated in the literature (e.g.[41]), the contacts of the lab scale geometry are tilted to various angles. For the VSB tool it is preferable to apply a 45° degree angles or avoid tilted structures at all. This may improve the pattern roughness and reduce the exposure time. The reason is that the VSB-type tool applies apertures with defined geometry, which is either rectangular or with 45° angle. Hence patterns with different than 45° and 90° angles or some curvilinear patterns need to be approximated with rectangular or 45°-triangular shapes, and can cause additional source of line edge roughness and longer exposure

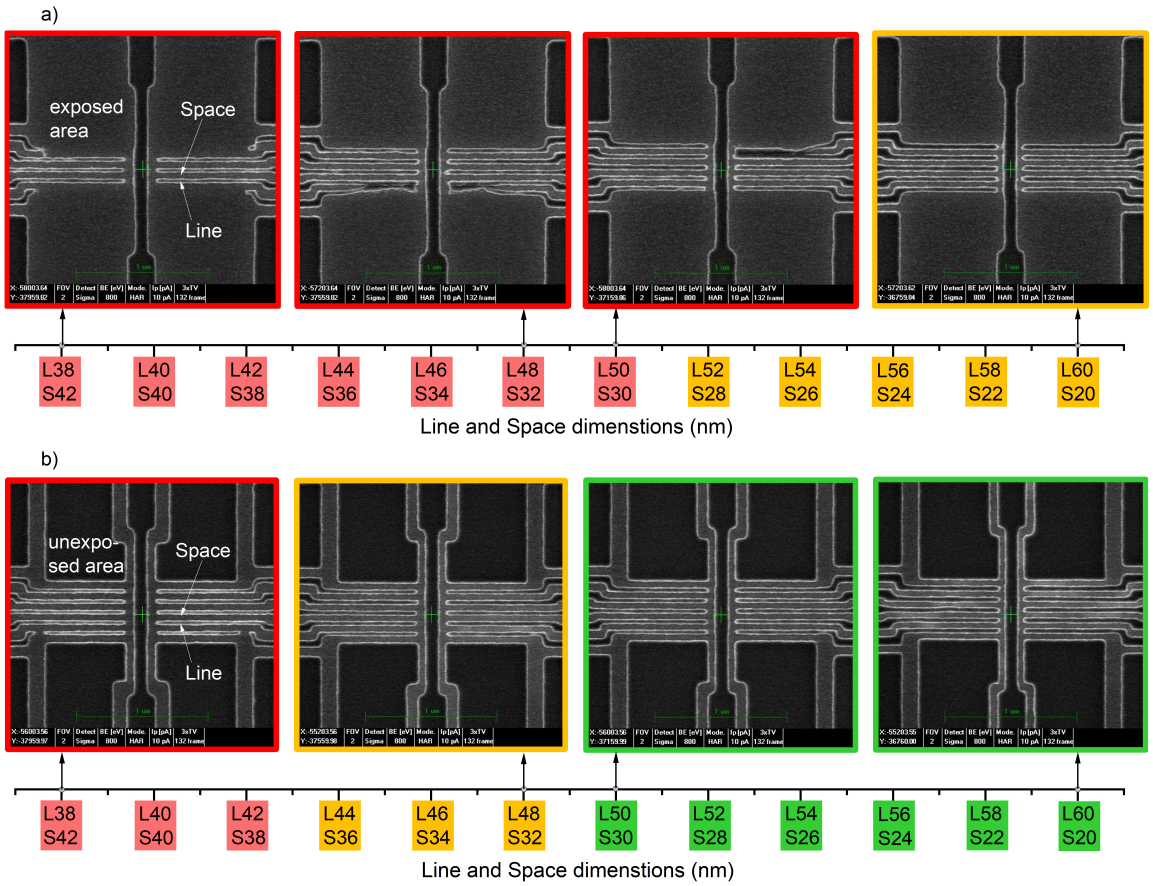

Figure 8. Lithography process window for two different gate electrode geometries and different L/S variations at constant pitch of 80 nm: with a) large and b) reduced exposure area around the electrodes. Green colour represents the optimal L/S ratios providing stable pattern in resist mask, yellow - pattern resolved only at some exposure dose, red - unresolved pattern, pattern collapse.

time. Therefore we applied mostly rectangular shapes for the complete device (see Fig. 1 a) and b)). For the quantum performance this modification is irrelevant, and the fanout can be chosen freely.

Gate electrode 3D shape after etching When speaking about electrode geometry it should be considered that after etching (transfer of the resist mask into the gate electrode material TiN) the lines are getting narrower because they are also etched from the side walls. Hence the spaces are getting wider. In present study, we observed an etch bias ΔS of about 12 nm. That means, that 50 nm line and 30 nm space in the resist transform after etching into a 38 nm line and 42 nm space. After SiO_2 deposition the space width reduces to 32 nm. The widening of the space by etching comes as an accommodation for the subsequent deposition of the self-aligned TiN layer (Fig. 2 (h)): The greater the distance between the electrodes, the better the gap can be filled with TiN. Ideally, this distance should be at least 35 nm to ensure reliable filling (Fig. 2 (f)). In addition, the slightly positive sidewall angle of the etched gate electrodes is used to allow homogeneous TiN deposition without voids that would occur with negative sidewalls.

Fig. 10 a) and d) represents the final optimised gate electrode arrangement after etching into the resist mask. The cross-sectional images b) and e) show the gate width of around 40 nm (ca. 38 nm). The images illustrate also that the gate width fluctuates, which is explained by the line width roughness (LWR) observed in f). To avoid or reduce the LWR it is reasonable to reduce the etch bias or reduce the exposure dose to get wider lines which do not wobble. Nonetheless, the final stack measured by TEM c) shows a good agreement with the desired structure. Fig. 10 c) corresponds to the schematic image in Fig. 2 h). The width of the fine gates in G_1 is

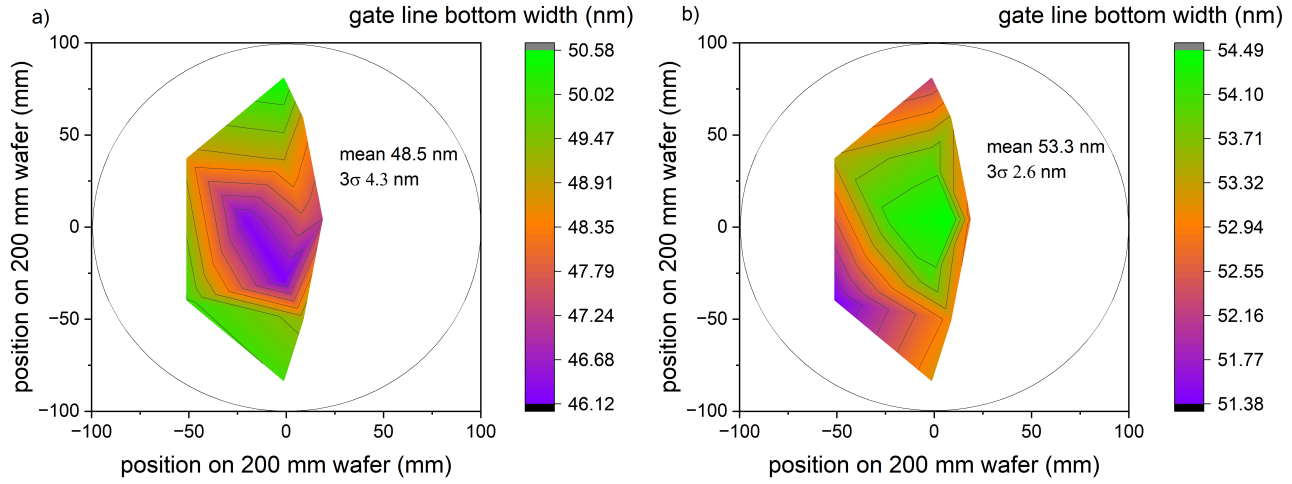

Figure 9. Gate pattern uniformity after development of the e-beam exposed resist, measured with CD-SEM on the a) 3 gate electrode structure, and b) on the 5 gate electrode structure.

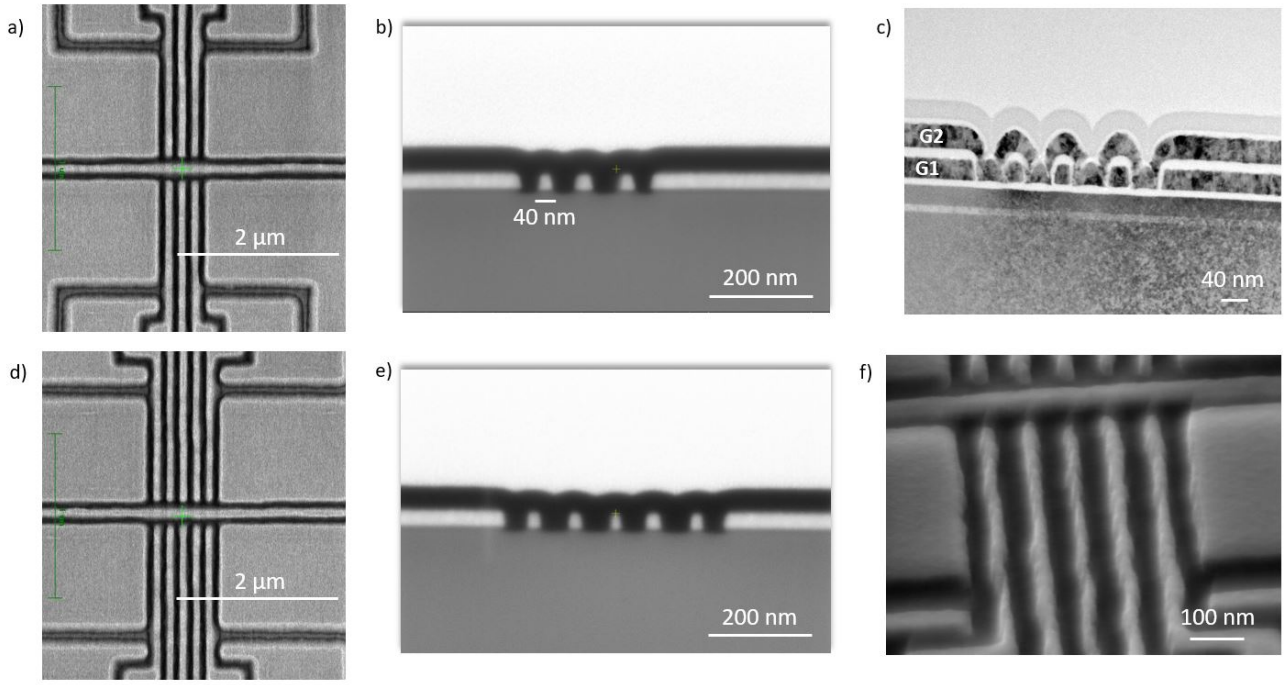

Figure 10. Images of the final gate electrode devices with optimised geometry (L=50 nm S=30 nm post litho, and L=38 nm post etch). All images were acquired after etching step. Etching was performed at Infineon FAB in Dresden. a), d) CD-SEM images of the final G1 structure after etching with three and five gates correspondingly. b), e) FIB cross section SEM images of the G1 electrodes after etching. c) TEM image of the complete gate structure according to the Fig. 2 h). f) tilted view of the etched five gate electrode arrangement.

slightly below 40 nm, and G_2 shows a good gap filling without voids due to the positive side wall angles of the G_1.

To summarise, the ideal gate electrode geometry after the lithography step, under the condition of reduced surrounding exposure area, is L=50 nm and above, S=30 nm and below, at constant pitch of 80 nm (see Fig. 8 b). Larger pitches between the 50 nm electrodes are also possible. The space of 30 nm is widened by the etching process, resulting in $w_{G1} = 38\,\text{nm}$ gate electrode width in TiN layer for the structured layer. After deposition of

5 nm SiO_2, the remaining space between the G1 electrodes is $w_{G2} = 32\,\text{nm}$, which is then subsequently filled with TiN (see Fig. 2 g) and h)). In the sum L, S and SiO_2 layer result in a 80 nm pitch. These geometrical parameters, along with the positive taper angle and the line width variations are studied in terms of corresponding qubit performance by COMSOL simulation, as described in the next section.

4. SIMULATIONS

For the gate layout in Fig. 1, we estimate suitable geometrical parameters such as gate pitch, widths, and spacing. These considerations are based on the general behavior of QDs in Si/SiGe, as described in Sec. 1. Starting from the estimated device parameters in the previous section, we establish geometric boundaries within which the device could be reliably fabricated. In this section, we adjust the simulation using the gate electrode geometry after the etching step described in Sec. 3.2 and verify the functionality of the gate pattern in terms of QD confinement, capatitive cross-coupling and tunnel-barriers to reservoirs: The gate pattern is designed to form a QD on one side, which can be tunnel-coupled to two electron reservoirs. On the other side, a single electron transistor (SET) shall be formed, which is capacitively coupled to the QD and thus operates as a proximate charge detector of the QD. The goal is to maximize the sensitivity of the SET to the QD and to control the QD filling down to the zero to few electron regime, which requires narrow tunnel barriers and a sufficiently strong confinement. As the gate pattern is designed to be symmetric with respect to the separation gate, the location of QD and SET can be swapped. By swapping the SET and QD functionality, the symmetry of the device in terms of local potential disorder or non-ideal electrode shapes can be tested.

Our finite-element simulation-model (COMSOL Multiphysics) of the device electrostatics is based on the e-beam lithography results, target etch bias and gate oxide (GOX) thickness. It includes the structured gate layer G_1 (as shown in Fig. 1 c)), as well as a second, self-aligned gate layer G_2 (indicated in Fig. 1 a)). The schematic cross-section of the device is shown in Fig. 11 a). A structured gate width of $w_{G1} = 38\,\text{nm}$ and a $w_{GOX} = 5\,\text{nm}$ thick conformally deposited oxide layer for electrical isolation between G_1 and G_2 are taken into account. We assume the patterning pitch of $P = 80\,\text{nm}$ for the structured layer. This results in a gate width of the self-align gates, interleaving the G_1 finger gates, of $w_{G2} = P - w_{G1} - 2 \cdot w_{GOX} = 32\,\text{nm}$. The Si/SiGe heterostructure is modelled with a homogeneous dielectric constant $\epsilon_{Si} = 13$ and the Si quantum well is implemented as charge density plane at a depth of $z_{2DEG} = 35\,\text{nm}$ below the semiconductor/oxide interface at $z = 0$.

We use Poisson equation to numerically solve self-consistently for the electron potential $V(x, y)$ and electron density $\rho(x, y)$ in the 2DEG using the semi-classical Thomas-Fermi approximation.[44] In order to account for the filling difference between the sensor QD of the SET, which is usually operated in a multi electron regime, and the qubit QD, operated in the single-electron regime, the electron density for the QD region (here right-hand side of the separation gate) is set to zero only in the QD region.

We use the following strategy to iteratively determine the voltages applied to a given gate-electrodes pattern within the simulation: Before tuning the QDs, we increase the voltages on the four reservoir plates and the two outermost fine gates of each side until a sufficiently high electron density is achieved. Then, we tune the gate voltages applied to the SET gates (highlighted in green in Fig. 11 b)) until the tunnel barriers of the SET to the reservoirs reaches a targeted potential shape. For the QD side (highlighted in red in Fig. 11 b)), we coarsely pre-tune the shape of the desired QD. Then, we iterate the calculation of first and second orbital by Schrödinger equation and fine-tuning of voltages until only the lowest orbital state is found below the Fermi-energy. All voltages refer to the middle of the band-gap of silicon[45] and all simulation parameters are summarized in Table 2.

After tuning the voltages by the simulation, the calculated electrostatic potential $V(x, y)$ and electron density $\rho(x, y)$ is obtained as shown in Fig. 11 b). The color plots are overlaid with the G_1 gate layout while G_2 is omitted but globally placed on top of the displayed device section. We are able to form two QDs in the potential, separated by the gate electrode. From the preliminary simulations, we find a separation gate width w_{Gsep} which is far away from fabricational boundaries. Therefore, the width of this gates is picked based on the following considerations: The width of the separation gate G_{sep} controls the capacitive coupling of the QD and the sensing QD of the SET. It also separates opposing electron reservoirs. We chose a well-balanced width of 60 nm, which allows to separate the electron reservoirs at $V_{sep} = 0\,\text{V}$ and thus simplifies the operation of the device. On the

Table 2. Simulation parameters used in the presented COMSOL model.

Description	Variable	Si/SiGe
Electrode width	w_{G1}	38 nm
Self-aligned width	w_{G2}	32 nm
Thickness oxide	w_{GOX}	5 nm
Pitch	P	80 nm
Separation gate width	w_{Gsep}	60 nm
Distance tip	d_{tip}	70 nm
Effective electron mass	m^*	0.19 m_e^*
Valley splitting	E_{VS}	70 μeV
Fermi energy	E_F	585 meV
Permittivity of heterostructure	ϵ_r	13
Permittivity of oxide	ϵ_{oxide}	4
Min. element Size (ES)	d_{min}	5 nm
Max. ES	d_{max}	60 nm
Min. 2DEG ES	$d_{min,2DEG}$	3 nm
Max. 2DEG ES	$d_{max,2DEG}$	10 nm
Depth of 2DEG	z_{2DEG}	35 nm

one hand, a larger gate width would reduce the capacitive coupling between QD and SET, and thus lowers the sensitivity of the charge detector. On the other hand, a smaller separation gate width would require more negative voltages to isolate the reservoirs from each other, resulting a higher potential difference to the surrounding gates and thus an increased chance of current leakage across gates.

Each dot is controlled by three of the five finger gates indicated in green (red) on the left (right) side of the separating gate. The distance between the tip of the fine gates and the separation gate was another input parameter not limited by fabrication. We found that $d_{tip} \approx 70$ nm is suitable, which is a bit larger than the typical diameter of a QD. By reducing d_{tip}, on the one hand, the accumulation control of the G_2 gate is more screened, which must be compensated by a more positive plunger gate voltage. This might conflict with upper bound of the plunger gate voltage around the accumulation threshold, since charge accumulation underneath the long plunger gate leading to an unintentionally deformed QD must be avoided. On the other hand, making d_{tip} too large would require strong negative voltages on the barrier gates to form the tunnel barriers as well as resulting in broader barriers. The left QD is visible in the electron density, while the right QD shows no accumulated electrons. This is consistent with the previously discussed goal of using the left QD as SET, sensing the charge occupation of the right QD, which operates in single electron mode.

We calculate the probability densities $|\Psi(x,y)|^2$ of the first and second orbital state (OS), by solving the Schrödinger equation in the potential of the right QD (shown in top (first OS) and bottom (second OS) panel of Fig. 11 c)). We observe the occurrence of a second maximum along the y-axis for the second orbital state. This orientation of the second OS is expected due to the elongated shape of the dot. We calculate the energy difference of the first and second eigenstate (denoted as orbital splitting) $\Delta E_{OS} = E_{OS,2} - E_{OS,1} = 1.0$ meV. Thus, the simulated QD-confinement is within the typical range of 1-1.5 meV,[46] which indicates that it is robust with respect to disorder-induced separation into several dots.

2-dimensional line cuts of the potential and charge carrier density are given in Fig. 11 d), corresponding to the SET (left/ green) and single electron dot (right/ red) following the path indicated by the dashed lines in Fig. 11 b). This path was calculated using *Dijkstra's algorithm*, minimizing a cost function combining the semiclassical Wentzel-Kramers-Brillouin approximation and a path-of-lowest-potential (see[47] for more information). We can form a set of two barriers for each QD, given by the regions above E_F (indicated by the dashed line), allowing localization of electrons inside the QDs. The position of the reservoirs close to the QD, as indicated by the

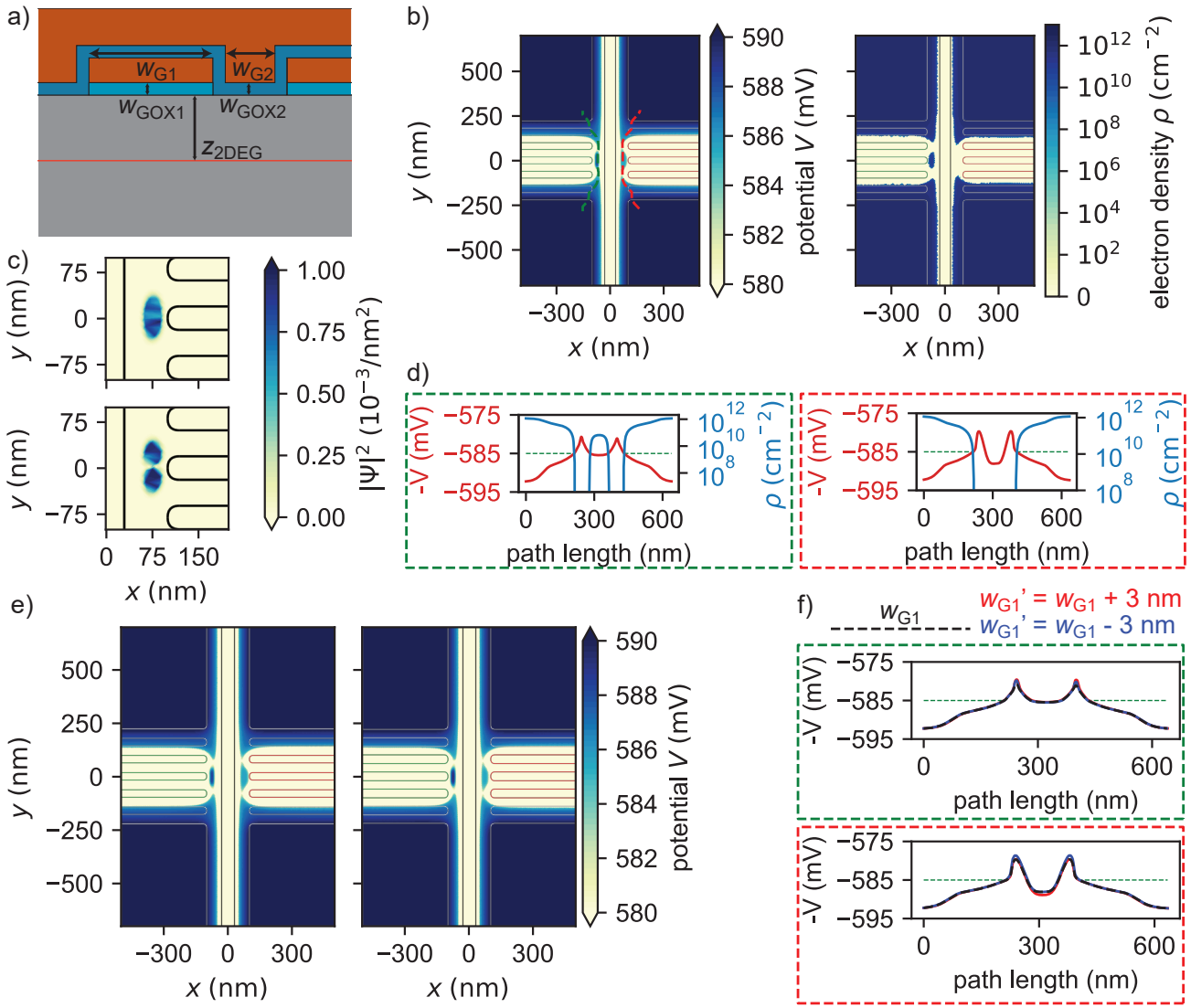

Figure 11. Simulation results: a) Schematic cross-section of the gate stack implemented into our simulation. b) Electrostatic potential $V(x, y)$ formed in the quantum well (left) and electron density $\rho(x, y)$ in the quantum well (right), overlaid with the G_1 gate layout (G_2 is not shown). c) Probability density $|\Psi(x, y)|^2$ of the first (top) and second (bottom) orbital state calculated by solving the Schrödinger equation on the simulated quantum well potential. d) Line cuts through the left (green) / right (red) QD along the path indicated by the colored dashed lines in panel b, respectively. e) Electrostatic potential formed in the quantum well for variations of the structured gate width of -3 nm (left) / +3 nm (right), after repeated gate voltage tuning. f) line cuts corresponding to the paths shown in b) for the original layout (dashed lines) as well as for the two studied variations.

rapidly increasing ρ on the other side of the barrier with regards to the QD, indicates a good capacitive coupling. Furthermore, we achieve electron densities up to 1×10^{12} cm^{-2}, indicating sufficient 2DEG accumulate far beyond the metal-insulator-transition.

In a next step, we consider the line width variation in the size of $3\sigma_w = 3$ nm of the patterning process, as shown in Fig. 9 b), and study its impact on the device. In this way, we ensure that the functionality of the device as a spin qubit is not compromised by unavoidable variations in the fabrication process. Therefore, we assume the positional accuracy of the e-beam to be sufficiently high and therefore keep the patterning pitch fixed to $P = 80$ nm. An increase/decrease in the width of the gate electrodes in the structured layer $w'_{G1} = w_{G1} \pm 3$ nm therefore results in a decrease/increase in the width of the self-aligned interleaved gates $w'_{G2} = w_{G2} \mp 3$ nm. We

repeat the simulation for the two extreme values to estimate the worst case. After applying these changes to the simulated gate geometry, the described voltage tuning process is repeated. The potential $V(x, y)$ obtained for the smaller (larger) structured gate width w'_{G1} is shown on the left (right) in Fig. 11 d). We were able to adjust the voltages for both directions of variation to recover the qubit/SET QD formation. This required voltage changes in the order of $\mathcal{O}(100\,\mathrm{mV})$ on the sets of three gates forming the QDs. This is consistent with voltage fluctuations observed in experimental studies of industrially fabricated quantum structures.[48] We obtain slightly increased orbital splittings of 1.1 meV and 1.2 meV and single-electron occupation, enabling well isolated operation of the qubit QD in the first OS.

In Fig. 11 f), we compare the potentials for the original gate electrode geometry and the two variants, obtained along the line cuts for the SET QD (green) and the qubit QD (red) as shown in Fig. 11 b). The original potential is plotted in black and dashed, while the potentials for smaller (larger) structured gate width are added in blue (red). Except for minor variations in the shape of the barriers, the applied voltage changes allowed the original potential for both variations to be reproduced.

Using simulations, we have successfully demonstrated shaping of a single-electron QD with sufficient confinement and a proximate charge-sensor tunnel-coupled to well-accumulated reservoirs within the fabricational boundaries and tolerated geometrical variations. These results affirm the viability and operability of the targeted device, and thus the fabrication process, according to our intended specifications.

5. CONCLUSION

In this work we setup a CMOS industry compatible fabrication process of gate electrodes for Si/SiGe heterostructure spin qubits based on e-beam lithography. Our work is dedicated to the e-beam lithography process and the interplay of pattern fidelity with gate electrode geometry. We developed a process providing high yield, uniformity, reproducibility and throughput of the resulting nanostructured electrodes. The following parameters of the qubit device geometry were considered during the study: exposure area around the gate electrodes, gate electrodes width and space in between, gap distance from the gate electrode to the separation gate and 3D shape of the gate electrode after etching. We observed that with given resist, reduced surrounding exposure area, and optimised lithography processing conditions a gate width of 50 nm can be reliably achieved for a pitch of 80 nm or more. We characterized the stability of the process and obtained a line width variation of $3\sigma_w = 3\,\mathrm{nm}$. Process details of the fabrication of the second, self-aligned gate layer resulted in line-to-gate transfer bias of 12 nm, when etching the resist pattern into the TiN gate metal, as well as positive flanks. Taking into account the 5 nm SiO_2 isolation layer, we obtain a final gate electrode width of $w_{G1} = 38\,\mathrm{nm}$ for the structured layer and $w_{G2} = 32\,\mathrm{nm}$ for the self-aligned interleaved gates on a pitch of $P = 80\,\mathrm{nm}$. We verified the operability of the device using a COMSOL Multiphysics model based on the obtained geometric parameters and successfully formed a qubit quantum dot (QD) and a charge-sensitive single-electron transistor (SET QD). The qubit QD could be brought to single-electron occupancy, showing a sufficiently large orbital splitting of 1 meV, and the tunnel barriers indicate favorable transport properties. With the simulations, we were able to show that the fabricated devices can be operated as intended, even when process variations were taken into account. This proves the applicability of our method for large-scale, high-throughput patterning of quantum devices.

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