SiGe BiCMOS Current Status and Future Trends in Europe

Pascal CHEVALIER
STMicroelectronics
Crolles, France
pascal.chevalier@st.com

Wolfgang LIEBL
Infineon Technologies
Regensburg, Germany
wolfgang.liebl@infineon.com

Holger RÜCKER
IHP
Frankfurt (Oder), Germany
ruecker@ihp-microelectronics.com

Alexis GAUTHIER
STMicroelectronics
Crolles, France
alexis.gauthier@st.com

Dirk MANGER
Infineon Technologies
Dresden, Germany
dirk.manger@infineon.com

Bernd HEINEMANN
IHP
Frankfurt (Oder), Germany
heinemann@ihp-microelectronics.com

Grégory AVENIER
STMicroelectronics
Crolles, France
gregory.avenier@st.com

Josef BÖCK
Infineon Technologies
Neubiberg, Germany
josef.boeck@infineon.com

***Abstract*—This paper reviews the advantages of SiGe BiCMOS technologies and their applications in the millimeter-wave to terahertz domains. The state-of-the-art covering both the Si/SiGe HBTs and the CMOS nodes is shown. Future perspectives and related main challenges are discussed with a focus on the ongoing European research activities through the presentation of the TARANTO project, whose main objective is to help developing 600 GHz f_{MAX} nanoscale SiGe BiCMOS platforms.**

Keywords—Si/SiGe HBT, BiCMOS, millimeter-wave, terahertz, optical, automotive radar, heterogeneous integration.

I. Introduction

CMOS scaling led to the pervasion of CMOS into many applications, including Radio Frequency and Analog Mixed Signal (RF/AMS). The continuous reduction of the gate length drove the increase of the current gain frequency f_T to such values that CMOS was expected to completely replace BiCMOS technologies several years ago already. It has not occurred up to now. Indeed, although the pervasion of CMOS for RF applications is incontestable, BiCMOS technologies, similarly to III-V technologies, remain a reference for RF and Millimeter-Wave (mmW) applications, and market drives the development of new BiCMOS technologies at the companies leading in RF/AMS. Objectives of this paper are to:

- Understand why BiCMOS remains attractive for many applications and provide examples;
- Present current state-of-the-art for both high-speed Si/SiGe Heterojunction Bipolar Transistors (HBT) and related CMOS nodes;
- Review the perspectives through the angle of the European research activities, Europe being a leader in this field for several years now.

The paper is therefore organized as follows. Advantages and applications of high-speed SiGe BiCMOS are reviewed in the first section. In particular, the assets of bipolar devices and more generally of BiCMOS versus CMOS are discussed. Examples of applications are mentioned. SiGe BiCMOS state-of-the-art, covering both the Si/SiGe HBT and the CMOS nodes is presented in a second section. Third section presents the research activities currently running in Europe in the frame of the ECSEL TARANTO project [1]. Context, objectives and organization of this project are detailed. The work done on technology development, which covers Si/SiGe HBT device performance improvement, monolithic BiCMOS platforms development and heterogeneous integration are more specifically discussed.

II. High-Speed BiCMOS Advantages and Applications

A. BiCMOS vs. CMOS

As mentioned in the introduction, the RF performances reported for advanced CMOS technologies [2] raise the question of the need for BiCMOS technologies. Key elements explain why BiCMOS technologies remain superior for many applications:

1) Extrinsic vs. intrinsic RF device performance: RF performance at device level are reported after de-embedding the parasitics coming from the metallization layers, which is a standard procedure to extract device models. However, the performance of wired devices is degraded compared to the one of a device without any metallization layers (in some de-embedding methodology only the contacts are kept in the 'intrinsic' transistor). This is especially true for MOS transistors [3], while the impact of de-embedding on bipolar transistor performance is negligible [4]. Indeed any additional parasitic capacitance of interconnects has a significant effect on the f_T of advanced node CMOS technologies, where the input capacitance is low [5]. Therefore, the direct comparison of *hf* performance between MOS and bipolar transistors must be done with caution since it does not account for the degradation due to the metal wiring stack. The latter strongly depends on the back-end-of-line (BEOL) of the technologies. Circuit designers usually prefer to compare the performance without de-embedding the metal wiring on top of the transistors, as discussed in [4] and [6]. As a consequence, the *hf* performance

of 28-nm FD-SOI NMOS transistor with an f_{MAX} of 330 GHz is not better than the one of the 55-nm BiCMOS SiGe HBT [2]. This effect is expected to further degrade for next CMOS nodes. In addition, FinFET transistors exhibit larger parasitic gate capacitance, which combined with the increase of the gate resistance further degrade the RF performance of MOS devices. Thus, it is admitted that the 'exploitable' RF performance of MOS technologies reached a peak at the 40 nm / 20 nm nodes.

2) Intrinsic device performance and reliability: Bipolar transistors are known to feature larger transconductance (g_m) and lower $1/f$ frequency noise. They also exhibit larger breakdown voltages (at equivalent speed) than MOS transistors and demonstrate a superior reliability. Indeed, MOS transistors reliability is limited by the hot carrier injection (HCI), which induces threshold voltage (V_T) and g_m degradations at high V_{DS}. HCI lifetime can be improved by either reducing the operating voltage or increasing the gate length, which both degrade the circuit performance [7]. Consequently, a larger output power (which is limited by the voltage/current swing, network losses and breakdown voltage) can be achieved with more reliability headroom in BiCMOS technologies compared to CMOS technologies.

3) Passive devices: Better passive devices are available in BiCMOS technologies. It is only due to the fact that BiCMOS technologies benefit from optimized BEOL that are usually not available in CMOS technologies. More generally, the dedication of BiCMOS technologies to RF and millimeter-wave applications leads to a better passive offer than for CMOS technologies.

4) Cost: BiCMOS technologies are usually built on CMOS nodes at least two generations behind the competing CMOS technologies. They benefit from lower development and wafer cost (although masks are added in BiCMOS). Practically, more volume will be required in CMOS to compensate for the higher mask set cost, which in fine makes BiCMOS more competitive for low to medium volume products. This advantage is however weighted by the die size, which depends on the digital density, meaning that the latest CMOS node will always offer a larger digital density compared to BiCMOS technologies.

B. Targeted Applications

It could be concluded from the CMOS / BiCMOS comparison presented previously that BiCMOS should be the default choice for RF/AMS applications for which large digital densities are not needed. However, it is clear that wherever CMOS can meet the applications specifications (without featuring the best performance) at a lower cost, it will replace BiCMOS (the same apply to BiCMOS vs. III-V technologies). It is worth mentioning that the ability of CMOS to compete with BiCMOS relies also on new digital-based design architectures less demanding for the analog performance. In addition, the digitalization of the circuits is expanding to the analog functions. Consequently, applications of BiCMOS technologies move to always increasing frequencies and/or very demanding (power, reliability, etc.) applications at lower frequencies for which CMOS can hardly compete with Si/SiGe HBTs. These applications, calling for both faster Si/SiGe HBTs and denser CMOS, encompass high-speed and high-data-rate communication systems, and smart mobility systems involved in the future fully automated transportation systems.

The related rapidly growing markets are automotive radars [8], electro-optical networking [9] or wireless backhaul and future potential applications fields like 5G communications and radar in a frequency range above 100 GHz. Different scenarios, based on RF massive MIMO (Multiple-Input Multiple-Output) hubs, refer to vehicle-to-vehicle and vehicle-to-infrastructure mmW high bit rate communications (up to 100 Gb/s) used both for vehicle infotainment and assisted/autonomous driving. This will put stringent constraints on the bandwidth, noise, linearity, output power and power-added efficiency (PAE) of the RF front ends operating up to the D-band (110-170 GHz). Current SiGe BiCMOS technologies already address these applications with, e.g., 77 GHz automotive radar or 100 Gb/s optical communications in production today. Next generations will deliver a better RF performance with faster Si/SiGe HBT and a larger integration thanks to denser CMOS while maintaining the cost competitiveness. Denser CMOS is an enabler for high resolution digital/analog conversion, which is key in many applications.

III. SiGe BiCMOS Current State-Of-The-Art

It comes out of the applications discussion that both the performances of Si/SiGe HBT and the CMOS node are the two key Figure of Merits (FoM) of BiCMOS technologies. A third one is the quality of the passive devices, which consequently contributes (and sometimes more than active devices) to the final performance of circuits. This section reviews these three key FoM.

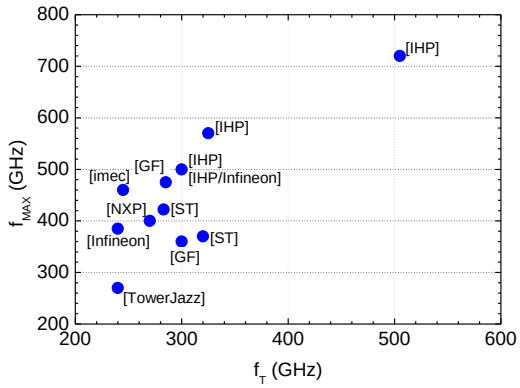


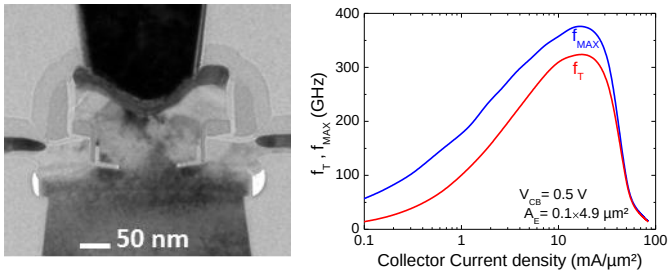
Fig. 1. Peak f_T and f_{MAX} values of high-speed SiGe HBT technologies (references are available in [10]).

A. Si/SiGe HBT State-Of-The-Art

A complete review of the Si/SiGe HBT state-of-the-art has been published recently in [10], from which the f_{MAX} vs. f_T plot presented in Fig. 1 is derived. This part presents a summary of the review done in [10] with a focus on industrial BiCMOS technologies i.e. in production or being under qualification for production (based on published and public data).

1) Performances of 'production-qualified' technologies: State-of-the-art SiGe BiCMOS technologies currently in production exhibit featuring f_T and f_{MAX} in the range of ~300 GHz and ~400 GHz, respectively. Self-aligned architectures are now the norm, the most popular one being the Double-Polysilicon Self-Aligned (DPSA) architecture using a Selective Epitaxial Growth (SEG) of the base (cf. Fig. 2, [11]).

This architecture is used in particular by Infineon Technologies [12], NXP [13] and STMicroelectronics [14][11]. Regarding the BiCMOS platforms in production today, best performance is reached in ST 55-nm BiCMOS (BiCMOS055) [11] with f_T = 320 GHz and f_{MAX} = 370 GHz and an associated collector-to-emitter breakdown voltage BV_{CEO} of 1.5 V. The average gate delay of a 23-stage CML ring oscillator is 2.3 ps. The DPSA-SEG architecture implemented in ST BiCMOS055 (B55), and inherited from ST BiCMOS9MW [14], is built on a standard, so-called, high-performance collector module featuring a N+ buried layer, a collector epitaxy, a collector sinker and deep trenches isolation. Three flavours of bipolar transistors, differenciated only by their collector, are available. A high-speed (HS) NPN is obtained by adding a selectively implanted collector (SIC), which is absent from the medium-voltage (MV) NPN. A high-voltage (HV) NPN, featuring an all-implanted collector (replacing the N+ buried layer), is also available. The SEG of the Si/SiGe:C base in an emitter window is used to get the self-alignment between the emitter and the base. The link between the intrinsic base and the extrinsic base is formed during the Si/SiGe:C SEG. An As in-situ doped mono-crystalline emitter is deposited after the formation of L-shaped inside spacers allowing the emitter width reduction down to 100 nm. The fabrication of the HBTs is completed by the patterning of the Polyemitter and Polybase and the realization of the steps common to CMOS, with in particular the source / drain (S/D) junctions spike annealing, NiSi formation, contacts and metallizations.



(a) (b)

Fig. 2. From [10] a) TEM cross section of a HS HBT in BiCMOS055 [11]. (b) Corresponding f_T and f_{MAX} vs. collector current density.

Among the other industrial technologies featuring the largest f_T and f_{MAX} are NXP BC90MW (f_T/f_{MAX} = 270/400 GHz) [13], using a DPSA-SEG architecture but with an implanted collector and GF BiCMOS9HP ((f_T/f_{MAX} = 300/350 GHz) [15], which features a self-aligned architecture with a non-selective epitaxial growth (NSEG) base epitaxy with elevated extrinsic base regions.

2) New generation of HBT architectures: The popularity of the DPSA-SEG is due to the relative simplicity of this architecture. Indeed, it relies on a good experience on selective epitaxy to master its manufacturing. In particular, the most attractive feature is the formation of the link between the intrinsic base and the extrinsic base. This link is formed during growth of the intrinsic base, thanks to the overhanging polybase lead. In addition, the pedestal oxide etched away from the base cavity helps in reducing the extrinsic collector-base capacitance (C_{BC}). This feature is now the main limitation of this architecture to reach f_{MAX} > 400 GHz since intrinsic-to-extrinsic base resistance cannot be optimized independently of the intrinsic base. All the trials done to reduce the base resistance led to a degradation of the base transit time and therefore f_T. Thus, the research on novel architectures was driven by the need to form a low resistive path between the intrinsic base and the extrinsic, independently of each other. In addition, these architectures targeted low C_{BC} to maximize f_{MAX}. Several architectures have been published in the literature but best results to date have been obtained by the IHP with f_T/f_{MAX} of 300/500 GHz [16] and 505/720 GHz [17] in a 0.13-µm BiCMOS technology and a bipolar-only process, respectively. Details about these research activities are presented in § IV.B.1. Finally, research done in the frame of the ITRS (International Technology Roadmap for Semiconductors) showed that f_T / f_{MAX} of 0.8/2.0 THz could be reached [18].

B. CMOS Node State-Of-The-Art

1) Overview of 'production-qualified' technologies and related Bipolar / CMOS process integration issues: BiCMOS technologies enjoy a long lifetime so that significant production is still observed on 'old' 0.5-µm and 0.35-µm nodes. Volume production today in high-speed BiCMOS is probably in the 0.18-µm and 0.13-µm nodes, that are sweet spots with respect to the performance / cost trade-off. Indeed, state-of-the-art performances are demonstrated in 0.13-µm today [16]. The need for denser CMOS led to the development of nanoscale BiCMOS technologies in the past years. Today, 90-nm BiCMOS technologies have been published by GF [15] and NXP [13] and is being developed by Infineon Technologies (cf. § IV.C.1). Most advanced CMOS node is proposed by STMicroelectronics with the B55 [11] technology presented previously. The HBT / CMOS co-integration raises several changes, whose complexity increases when moving to denser CMOS. Three main categories of process issues exist [19]:

- Thermal budget: Depending on the position of the bipolar integration in the CMOS process flow, thermal budget constraint is put either on the CMOS devices or on the bipolar devices. Often the priority is put on the compatibility of CMOS devices with the original platform in order to avoid developing again the MOS models and related libraries. This approach is however more and more questioned today since the process thermal budget of CMOS process flow (and mainly the LDD and S/D final anneal) limits the scaling down of the vertical profile (and mainly the base profile) of the bipolar devices [20].
- Structural integration: Again the objective is to avoid any degradation of the MOS performances (including yield) by the addition of the bipolar process operations. The number of patterning steps necessary to build a Si/SiGe HBT makes it a real challenge. Reciprocally, the CMOS patterning steps must not impact the bipolar transistors, whose total height is usually much higher than the CMOS gate one. In nanoscale CMOS nodes, specific process adaptations are mandatory. Among them, we can find the usage of planarizing tri-layer lithography stacks for the gate patterning or the thickening of the Pre-Metal Dielectric but it requires

additional developments on contacts patterning. In addition, slotted (bar) contacts, which are often used in bipolar transistors [21] are no longer compatible with the standard patterning of MOS contacts.

- Back-end of line: The need for a specific BEOL is discussed in § III.C below. The first challenge is the compatibility of a metallization optimized for the digital performance with the analog constraints. Especially, the decrease of the electromigration capability with the reduction of the metal layers thicknesses puts more and more constraints on the wiring of Si/SiGe HBTs, which drive lot of current (peak f_T of a 300GHz transistor is ~ 15 mA/µm²). The choice between an analog- and a digital- optimized BEOL is a dilemma since modifications in the thin metal stacks could impact the digital capability and libraries compatibility.

2) Perspectives for next BiCMOS nodes: The development of BiCMOS technologies in 45 nm and 28 nm CMOS nodes or even below faces two questions. The first one is the technical feasibility of the bipolar / CMOS co-integration since CMOS technologies are more and more complex with MOS devices more and more sensitive to any 'perturbation'. The second one is of course the cost, with on the one hand the development cost linked to the first question, and on the other hand the wafer cost of these technologies. These cost-related questions are difficult to answer since they must be handled in the frame of a product plan. Concerning the technical feasibility, preliminary studies [19][20] have shown that perspectives exist for planar technologies such as fully-depleted (FD) silicon-on-insulator (SOI) CMOS platforms until the 14/10-nm node. Main challenges lie in the high-K metal gate (HKMG) stack that drives the V_T of MOS devices, that cannot be tuned by playing on well or pocket implantations. The control of the SOI thickness, critical for the performance of the MOS devices, is also a major concern. As discussed in § IV.D, the advanced CMOS / mature BiCMOS heterogeneous integration is an alternative way to the usual monilithic integration.

C. Passive devices: Passive devices are the third pillar of the BiCMOS technologies and therefore must benefit from the same care in their definition and development than the bipolar devices. A part of the offer can be common to what can be found in RF CMOS platforms, i.e., a wide range of resistors, varactors, metal capacitors, etc. The bipolar process steps can be used to complement the FEOL offer with specific diodes (PIN & Schottky) benefiting from the bipolar collector module [15]. But, while a mmW BEOL is not a standard for RF CMOS, it is part of the BiCMOS offer for a while. As mentioned previously, the BEOL choice is driven by Digital / Analog trade-off. This can be illustrated by the comparison between the BiCMOS9MW and BiCMOS055 technologies of STMicroelectronics (cf. Fig. 3). In the first one the original 0.13-µm digital BEOL has been fully modified to offer a dual thick Cu module at the expense of the thin metal layers. In the second one, a thick Cu metal level has been added to the original 55-nm CMOS metallization i.e. without any modification of the thin metal layers. The addition of one or two thick Cu layers allows the increase of the Q-factor of the inductors and the reduction of the attenuation constant of the transmission lines (down to 0.5 dB/mm at 60 GHz in BiCMOS9MW). It also increases the current capability and reduces IR drop. However thick Cu increases the complexity and the cost of the technology.

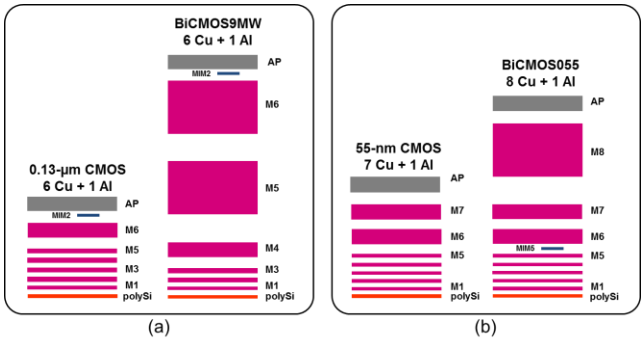


Fig. 3. Exemples of BEOL modifications between the digital CMOS and derived BiCMOS at STMicroelectronics in 0.13 µm (a) and 55 nm (b).

IV. Research Activities in Europe: TARANTO Project

TARANTO [1] is a 3-year R&D European funded project, started on April 2017. It aims at further strengthening the leading position of the European semiconductor industry in SiGe BiCMOS. Then, it targets to provide a solid industrial base for the development of new products in areas such as telecommunications, home electronics and car electronics which are of key importance for Europe's high-tech industries.

A. Project Description

1) Project filiation: TARANTO is built on the results of the successful European funded projects DOTFIVE [22], DOTSEVEN [23], and RF2THZ [24], which helped to establish Europe's leading position in SiGe BiCMOS technology within last decade. These projects have facilitated impressive innovations (cf. § IV.B.1) in HBT technology wich resulted, e.g., in an increase of record f_{MAX} from 350 GHz before the start of DOTFIVE in 2008 to 700 GHz achieved in DOTSEVEN.

2) Project objectives: The main technical objectives of TARANTO are, first, to make the new performance level of SiGe HBT demonstrated in previous projects available for mass production, and second to tailor technologies to the above-mentioned application domains. In DOTSEVEN, HBTs with f_{MAX} up to 700 GHz were realized for the first time by introducing non-conventional device architectures and elaborating processes sequences regardless of any CMOS compatibility. TARANTO addresses the challenging task to reach a similar performance level in fabrication processes that fulfill the industrial needs of simplicity, robustness and high yield. Then it aims to integrate these HBTs in advanced CMOS processes with tight constraints on thermal budget and device topology. Technically, the objective are:

- To develop 600 GHz f_{MAX} HBTs integrated with existing CMOS processes i.e. 1) SiGe on low-cost CMOS (130/90 nm) for Infineon Technologies as best solution for cost-effective mm-wave applications like automotive radar, medical sensing and wireless backhaul and 2) SiGe on advanced CMOS (55/28 nm) for ST as best solution for highly integrated RF

applications like 5G communications and ultra-high speed optical communication;

- To perform advanced studies at IHP on HBT with 700 GHz f_{MAX} compatible with the BiCMOS technologies of Infineon and ST.

The project not only addresses the development of new BiCMOS platforms, but also the characterization and modelling activities which are required to develop process design kits (PDKs) for the design of integrated circuits. Finally, the performance of the technologies will be demonstrated by means of three system demonstrators:

- High speed ADC and DAC for ultra-high speed optical communication;
- Advanced and scalable radio transceiver frontend for a 5G capable massive MIMO system;
- Multi-Gbit/s E-band transceiver with integrated beam stearing functionality for inter-vehicle communication.

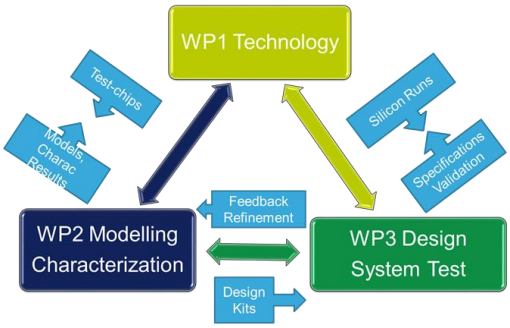


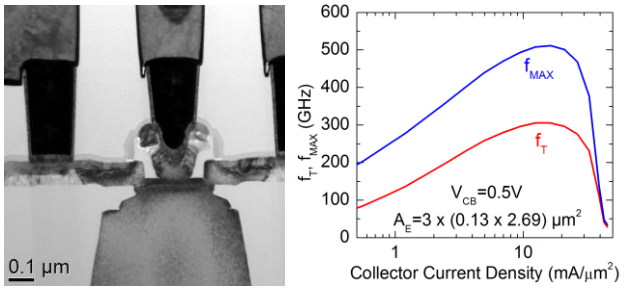
Fig. 4. Main work packages and interactions in TARANTO.

3) Project organization: TARANTO activities combine (1) the development of high-performance SiGe BiCMOS technologies, (2) the development of design infrastructure with advanced device models and PDKs, and (3) the design of fundamental building blocks and system demonstrators. Therefore, the project addresses the full value chain required for the introduction in the market of a new technology generation and for its exploitation into new product opportunities. The activities in these three areas are organized in three work packages. The schematic in Fig. 4 represents the interactions between them. In addition to those technical work packages, a management work package (WP4) is added for the management of the project, the dissemination of project results and project communication and for the exploitation of the results. Next paragraphs deal with the WP1 work for whose the partners are IHP, Infineon Technologies and STMicroelectronics. Information about the other work packages and related partners can be found in [1].

B. Device Development and Optimization

1) IHP & Infineon Technologies: IHP investigates two HBT concepts with respect to BiCMOS integration and their potential for highest RF performance. Both approaches utilize partially mono-crystalline extrinsic base regions to address the challenge of forming low-resistive connections to the internal base simultaneously with low C_{BC}. These extrinsic base regions are formed by additional epitaxial steps after formation of the emitters.

The first architecture uses SEG of the base combined with an epitaxial base link [25]. This EBL HBT architecture mitigates major limitations in the base link resistance and consequently in f_{MAX} of the classical DPSA-SEG architecture [26]. The process is characterized not only by a self-aligned emitter-base and emitter-collector design but also by a self-aligned arrangement of the emitter contact area to the emitter window helping to decrease R_B and C_{BE}. IHP and Infineon explore the performance potential of the EBL-HBT concepts in joint fabrication runs which start at Infineon by forming the buried layer, the deep trench and shallow trench isolation (STI), and the MOS gates. Next, the EBL-HBT module is fabricated at IHP. After HBT fabrication, the process is continued at Infineon with implantation of S/D regions and BEOL fabrication. A performance of 240 GHz f_T and 500 GHz f_{MAX} was achieved in such a joint BiCMOS fabrication run [8]. f_T values of 300 GHz together with f_{MAX} values of 500 GHz were demonstrated in a simplified process where some steps of the CMOS flow such as formation of gate spacers and S/D extensions were omitted [26]. The TARANTO project addresses further performance enhancement and improved manufacturability of this HBT module. The addressed process developments include structural modifications for improved scalability of the emitter window width, optimized base-emitter spacers, an improved fabrication process for the epitaxial base link, and optimization of the vertical doping profile.



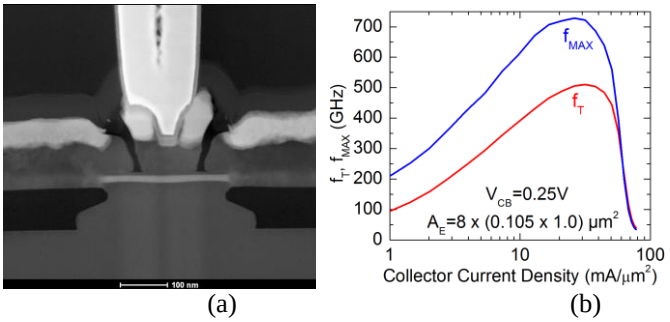
(a) (b)

Fig. 5. (a) TEM cross section of an HBT with elevated extrinsic base and 130 nm emitter width (from [26]), (b) Corresponding f_T and f_{MAX} vs. collector current density.

The second architecture utilizes NSEG of the base and elevated extrinsic base regions (EEB) grown after emitter formation. Such a device architecture is used in IHP's 130 nm BiCMOS processes SG13S [27] and SG13G2 [16]. The self-aligned arrangement of the elevated extrinsic base to the emitter window facilitates very low values of the extrinsic base resistance. However, the arrangement of the emitter windows to the internal collector regions and the selectively-implanted collector regions (SIC) is defined by lithographic alignment in this concept. An advanced version of this process has demonstrated so far the best high-frequency parameters. f_{MAX} values of 720 GHz, f_T values of 505 GHz, and CML ring-oscillator gate delays of 1.34 ps were achieved in an experimental process flow [17]. Process constraints due to the thermal budget of the CMOS were omitted in this bipolar flow. A series of process modifications was introduced to enhance the RF performance of the HBTs with respect to the previous technology generation SG13G2. These developments include an improved vertical doping profile with enhanced Ge

concentration, reduced depletion layer widths, an enhanced conductivity of emitter and base link regions, improved lateral control of the selectively implanted collector, and enhanced dopant activation due to millisecond annealing and a low temperature backend with nickel silicide [17].

The challenging task of integrating HBTs with such a performance level in a CMOS process is addressed in TARANTO. The BiCMOS integration of the NSEG HBT is being investigated in the 130 nm process of IHP. HBTs are integrated after gate structuring and re-oxidation of CMOS gates as described in [27]. In this concept, the major thermal budget of the CMOS process that acts on the HBT is the final RTP step for S/D activation. In the BiCMOS process, the temperature of this step will be reduced in order to minimize its impact on the HBT at a cost of re-engineering the CMOS devices. Moreover, additional process effort is needed to avoid the formation of spacers at the emitter due to the gate spacer process. The cobalt silicidation of the original CMOS process will be replaced by a NiSi process because of its beneficial effect on HBT performance. The HBTs of [17] took additional advantage of a millisecond flash annealing process. This process is not available for routine BiCMOS fabrication at IHP and its effect on RF performance has to be compensated by other measures.



(a) (b)

Fig. 6. (a) TEM cross section of an HBT with elevated extrinsic base and 105 nm emitter width (from [17]). (b) Corresponding f_T and f_{MAX} vs. collector current density.

As described above, a very encouraging HBT performance was achieved in DOTSEVEN with the joint fabrication runs of IHP and Infineon. In TARANTO, the goal for Infineon is to establish an HBT with epitaxial base link which is completely manufactured in Infineon fabrication lines and shall be integrated in a 90-nm BiCMOS process. The target device structure will be adapted from the IHP EBL concept [25] and will be optimized to meet the requirements of volume production. The development is divided in two phases. In the first phase, the necessary unit processes for the EBL HBT, which have been done up to now by IHP, will be developed in Infineon's wafer fab in Dresden. This process shall reach an f_{MAX} > 500 GHz and a level of maturity which is suited for processing of test structures and circuit runs for partners in WP2, which deal with characterization and modeling of the new devices, and in WP3, which use the new technology for circuit design. So far Infineon was able to achieve an f_T of 305 GHz and f_{MAX} of 537 GHz for an HBT with 0.11×2.7µm² emitter area integrated in Infineon's 130-nm CMOS process. Details of this work are described in [28]. In the second phase of the project, the performance of the HBT will be further optimized towards f_{MAX} of 600 GHz. Key topics in this task are the optimization of the doping profiles of the HBT, the improvement of the selective base link epitaxy and the scaling down of the emitter window to values below 100 nm. Furthermore, the impact of the thermal budget from BiCMOS integration on HBT and CMOS devices will be studied.

2) STMicroelectronics: The main objective of ST with respect to this task is to demonstrate a 400 GHz f_T / 600 GHz f_{MAX} HBT compatible with the 55-nm and 28-nm FD-SOI CMOS nodes. The three main topics under investigation are 1) the process thermal budget, 2) the emitter-base architecture and 3) the collector module. Developments in B55 technology were indeed constrained by both the reuse of the HBT architecture introduced in the BiCMOS9MW technology [14] and the CMOS process thermal budget which had not been modified versus the CMOS technology of reference. Hence, improved HBT transit frequencies can be achieved by reducing the process thermal budget of B55 technology to better control the dopants diffusion. It is the case when the transistor is integrated in 28-nm CMOS [20] and is possible by modifying the 55-nm CMOS process thermal budget. The study published in [29] exhibited that a too low process thermal budget degrades the MOSFET performances and cannot be recovered due to the sensitivity of MOSFETs to dopants diffusion and activation. However, a moderate reduction of the S/D spike annealing combined to Dynamic Surface Annealing (DSA) recovers the MOSFETs performances while improving significantly the performances of the HBT (355 GHz f_T / f_{MAX} HBT was demonstrated). The f_{MAX} challenge is addressed by the development of a new bipolar architecture overcoming the limitations of the DPSA-SEG architecture (cf. § III.A.2). A new proprietary architecture, called EXBIC (for Epitaxial eXtrinsic Base Isolated from the Collector), first investigated by TCAD [30] is being developed (cf. Fig. 7). This structure is based on two key processes. First, a boron in-situ doped epitaxial lateral base link is used to widely reduce the extrinsic base link resistance. Then, an isolation between the extrinsic base and the collector is implemented preventing boron diffusion and reducing C_{BC}. Another interesting feature of this architecture is the ability to master the collector profile with an intrinsic in-situ doped collector. Driven by the compatibility with FD-SOI CMOS, studies are also done on the collector module. The objective is to replace the buried layer used in B55 by an implanted collector while keeping a regular CBEBC transistor layout [19]. This kind of collector architecture shows some drawbacks like the significant amount of defects it generates when arsenic is used as implant species. The carbon-phosphorous co-implantation dramatically reduces this drawback thanks to a good silicon-interstitials passivation. Additionally, a good dopants profile control can be reached thanks to appropriate Carbon dose and energy. Similar maximum f_T values (~ 325 GHz) are obtained for both B55 reference and structures featuring a Carbon-Phosphorous co-implanted collector. However, a layout optimization aiming at reducing the collector resistance leads to impressive f_T of 450 GHz [31]. Nevertheless, f_{MAX} performances remain widely impacted by both an important base resistance and a high C_{BC} due to the layout constraints. The implementation of a Super Shallow Trench Isolation (SSTI) module is currently under

investigation to reduce the base-collector capacitance. Indeed, standard STI module cannot be used due to its 300-nm depth which cuts the dopants area in the case of an implanted collector. Finally, device adaptation studies in 28-nm FD-SOI will investigate the bipolar integration constraints and evaluate the best bipolar integration scheme with respect to the CMOS integrity.

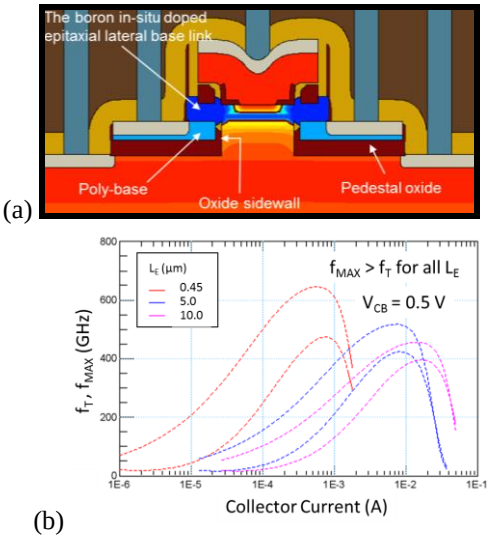


Fig. 7. a) TCAD cross-section of the EXBIC architecture. b) f_T & f_{MAX} from B55X (cf. IV.C.2) tentative HICUM model based on TCAD simulations.

C. Monolithic Platform Integration

1) Infineon Technologies: On Infineon side, the final goal is to develop the new BiCMOS platform B12HFC which integrates the new HBT into Infineon's 90-nm CMOS node. A major topic in this task is to find a suitable integration position of the new HBT module in the CMOS process flow. On the one hand, the thermal budget of the highly-doped drain (HDD) and lightly-doped drain (LDD) anneals in this CMOS process is considerable. In case the HBT module was integrated prior to S/D formation the thermal budget of the extension anneals would have to be significantly reduced. Otherwise, the performance of the HBT device would suffer from a large out-diffusion of the vertical profiles. The significant reduction in LDD anneals would in turn require reengineering the CMOS spacer construction as well as matching device implants to the new anneal regime. On the other hand, temperature profiles of key processes for modern HBT processing, e.g. 600°C – 800°C for selective epitaxy processes, can have significant impact on the doping profiles of MOSFET devices. Also, the layer stack which is necessary to build the bipolar devices can induce stress on the CMOS devices. This may lead to enhanced diffusion effects during annealing steps of the HBT. Based on Infineon's experience from previous SiGe BiCMOS processes compared to the base CMOS only process the substrate orientation needs to be changed from notch parallel to the {110} to a 45° off-standard orientation to improve performance and yield of the HBT devices. Hence, to reach the target of f_{MAX} = 600 GHz in a BiCMOS flow, the impact on the electrical parameters of the MOSFET devices has to be taken into account. As a consequence, re-centering of the device parameters by re-engineering of the CMOS base-process and, if necessary, re-modeling of CMOS devices has to be performed. Since this final 90-nm BiCMOS process will not be available before the end of the TARANTO project, Infineon will make B11HFC+ as an intermediate technology offering with an f_{MAX} > 500 GHz available. This way, the project partners of WP2 and WP3 will have early access to the newly developed HBT module. All the influences described above may impact the CMOS devices to such a degree, that CMOS circuit functionality using design parameters of the base-technology cannot be ensured. Therefore, B11HFC+ is intended to be used for bipolar-only designs without CMOS functionality.

2) STMicroelectronics: The main objective is to develop the platfom of the next BiCMOS generation based on the studies aforementioned. While it was clear from the start of this project that a new bipolar architecture was mandatory, different options were considered for the CMOS node. In order to mitigate the risks related to the development of new bipolar architecture, the current roadmap plans the release of a second 55-nm BiCMOS technology featuring an improved SiGe HBT. In parrallel, integration trials will evaluate the feasibility of 28-nm FD-SOI BiCMOS. Concerning this new 55-nm BiCMOS, BiCMOS055X (B55X), the decision taken in the first year of the TARANTO project was to go for a modified process thermal budget. Results reported in [29] demonstrated that thermal budget could be optimized to both improve the performances of the bipolar transistors and match those of MOS transistors with the initial technology. Therefore the B55X technology is aimed to deliver the same CMOS devices offer than the B55 together with a 400 GHz f_T / 600 GHz f_{MAX} EXBIC Si/SiGe HBT featuring an implanted collector (cf. Fig. 7). An update of the resistors model is however expected due to the better dopant activation brought by the DSA. Current B55 CMOS models will not be updated in the first release of the B55X platform but will likely be fine tuned in next PDK releases. This technology will be made available both for device characterization and modelling (WP2) and circuits designs (WP3).

D. Heterogeneous Integration Studies

The goal of this task is to perform a feasibility study for system-in-package integration of SiGe with advanced CMOS.

1) Infineon Technologies: Infineon will evaluate the possibility to integrate SiGe BiCMOS chips fabricated on mature CMOS nodes together with very advanced CMOS ICs side by side in an eWLB (embedded wafer level ball grid array) package. In Fig. 8 this proposal is shown. Both chips are connected by a copper redistribution layer. Infineon will work on providing a demonstrator for this SiP. A very important aspect for the usability of this solution for automotive radars is the mechanical reliability of the new package. Using thermomechanical simulations the layout of the SiP will be optimized. Finally, temperature cycling on board studies will be performed to investigate the interaction of the two chips in an eWLB package with the PCB.

2) STMicroelectronics: Different 2.5D/3D heterogeneous integration processes are considered in this task (passive and active interposers, hybrid bonding, 3D monolithic). Objective is to evaluate the pro's and con's of the different approaches based on a (or several) product test case(s) based on

simulations and on STMicroelectronics manufacturing experience. The three FoM that are considered are 1) the performance, 2) the yield and 3) the process cost. They design constraints that will be taken into account will be 1) the analog/digital partitioning, 2) the IOs density and 3) the MOS / HBT pitch.

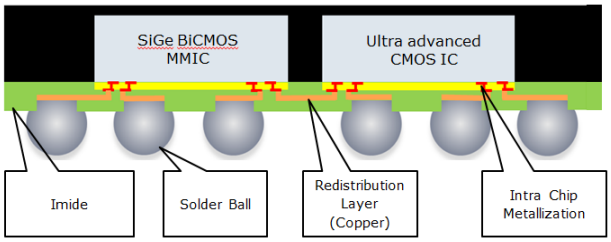


Fig. 8. Proposal for a System in Package (SiP) with a BiCMOS MMIC and an IC from a very advanced CMOS node.

V. Conclusions and Perspectives

Advantages of SiGe BiCMOS technologies and their applications in high speed and high data rate communication systems, and smart mobility systems have been reviewed. Current state-of-the art shows that ~300/400 GHz f_T/f_{MAX} Si/SiGe HBTs are available in advanced CMOS nodes (90 nm and 55 nm) and that +500 GHz f_{MAX} is demonstrated in 0.13-µm CMOS. Future perspectives, driven by the TARANTO European research program, have been presented. Main objective of this program is to support the development of 600 GHz f_{MAX} nanoscale SiGe BiCMOS platforms, which will maintain Europe at the forefront of the BiCMOS technologies.

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