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Device Architectures for High-speed SiGe HBTs

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***Abstract*—This paper reviews recent developments in process technology of high-speed SiGe HBTs at IHP. Two device concepts, one with selective epitaxial growth and one with non-selective epitaxial growth of the base, are analyzed with respect to their impact on radio frequency performance. Both device architectures take advantage of a low-resistive base link formed by selective epitaxial growth of extrinsic base regions after emitter structuring. As an intermediate result of the European project TARANTO, HBTs with f_T values of 470 GHz and f_{MAX} values of 610 GHz are demonstrated in a 130 nm BiCMOS process.**

Keywords—Si/SiGe HBT, BiCMOS, millimeter-wave.

I. Introduction

Advances in process technology of SiGe Heterojunction Bipolar Transistors (HBT) resulted in an impressive progress of their radio frequency (RF) performance. As a result, integration of high-speed SiGe HBTs in advanced CMOS technologies continues to be a very attractive option to expand their application fields into higher frequency bands. Despite of the pervasion of scaled CMOS technologies into an increasing number of RF and analog mixed signal applications, BiCMOS technologies remain a key enabler for highest application frequencies and demanding mm-wave systems that integrate radio front-end circuits with digital control circuits and signal processing on a single chip. SiGe HBTs offer in addition to high transit frequencies f_T and high maximum oscillation frequencies f_{MAX} larger breakdown voltages and consequently larger output power than deeply-scaled MOS transistors. The current status and trends of SiGe BiCMOS technology development were reviewed in [1]. HBTs of high-performance production technologies have reached now f_T values of about 300 GHz and f_{MAX} values of about 400 GHz and were integrated in CMOS nodes of 55 nm [2], 90 nm [3], [4], and 130 nm [5]. Future developments address further advancement of the performance of HBTs, CMOS, as well as passive components, whereby the selection of the base line CMOS note is driven by the amount of digital density required for the addressed market segment. Resent research has demonstrated a significant potential for further enhanced RF performance of SiGe HBTs. The current state-of-the-art is represented by peak f_T/f_{MAX} values of 505 GHz/720 GHz and current-mode-logic (CML) ring oscillator gate delay of 1.34 ps demonstrated in [6]. Developments of SiGe HBT technology and of their utilization for application towards THz frequencies were summarized in [7], [8].

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This paper addresses advancements and challenges in process technology of SiGe HBTs. Two device concepts are analyzed that address the challenge of forming a low-resistive connection to the intrinsic base by introducing an additional epitaxial step for the creation of extrinsic base regions. It is demonstrated that an HBT performance of 470 GHz f_T and 610 GHz f_{MAX} can be reached in a 130 nm BiCMOS process. These results were achieved in a process with non-selective epitaxial growth (NSEG) of the base. The paper is organized as follows. Sec. II reviews advantages and limitations of device architectures used in today's SiGe BiCMOS platforms. Sec. III deals with the HBT architecture with selective epitaxial growth (SEG) of the base and epitaxial base link (EBL) regions [9]. Sec. IV discusses the HBT process with NSEG of the base and elevated extrinsic base (EEB) regions that has demonstrated the highest RF performance of SiGe HBTs so far [6].

II. SiGe HBT Process Technology

The improvement of the RF performance of SiGe HBTs during the last decades was based on innovations of the device construction and of the fabrication steps accompanied by a significant reduction of lateral and vertical device dimensions. The target for the development of new device constructions has been the reduction of access resistances to the intrinsic emitter, base, and collector regions combined with minimum contributions of extrinsic device regions to the base-collector and base-emitter capacitances. The major challenge in this context is the simultaneous realization of low base resistance R_B and low base-collector capacitance C_{BC}.

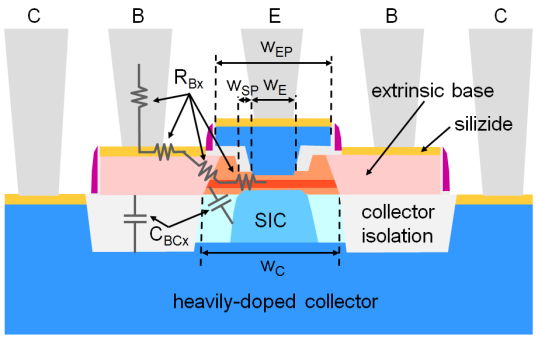

Fig. 1. Schematic cross section of a high-speed SiGe HBT. Critical device dimensions and contributions to the extrinsic base resistance R_{Bx} and extrinsic base-collector capacitance C_{BCx} are indicated.

Basic structural features of a typical high-speed SiGe HBT are depicted in the schematic cross section in Fig. 1. Critical device dimensions such as emitter window width w_E, collector window width w_C, emitter poly width w_{EP}, and the width of base-emitter spacers w_{SP} are indicated. Extrinsic device parasitics R_{Bx} and C_{BCx} are essentially determined by device

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regions adjacent to intrinsic transistor with width w_E. The extrinsic base resistance is build up by contributions from the base layer below the base–emitter spacer, the adjacent mono-crystalline or poly-crystalline p-doped region, the contact resistance between silicide and base poly-Si, the silicide resistance, the contact resistance between silicide and metal contact plug, and the resistance of subsequent metal regions. The extrinsic base-collector capacitance includes capacitances of the mono- and poly-crystalline extrinsic base regions to the selectively implanted collector (SIC) and the heavily-doped collector and contributions from the isolation region between extrinsic base and collector.

Today, most high-speed SiGe HBTs make use of the so-called double-poly-Si (DP) architecture which provides access from the contact regions to the intrinsic base and emitter regions by poly-crystalline (or single-crystalline) Si layers. These heavily doped layers support low emitter resistance R_E and low external base resistance R_{Bx}, respectively. Their dielectric isolation against the surrounding transistor regions keeps extrinsic capacitances C_{BCx} and C_{BEx} small. Despite of this common feature of state-of-the-art SiGe HBT technologies, there are quite different approaches for device manufacturing with different implications for optimization of their electrical performance. A key differentiator for SiGe HBT fabrication is the formation of the SiGe base by either selective or non-selective epitaxial growth. Other process options regard the lateral collector isolation by deep trenches or by the standard shallow trenches of the CMOS process, the formation of the highly conductive sub-collector, the formation of the base-emitter structure, and the degree of self-alignment.

The most straight forward approach to self-alignment of the critical dimensions of the intrinsic transistor is the Double-Polysilicon Self-Aligned (DPSA) devices architecture with SEG of the base [10]. This architecture is used in the latest high-performance BiCMOS production processes of ST Microelectronics [2], Infineon [5], and NXP [4]. In principle, only one lithographic step is needed to construct the internal transistor. The emitter and collector windows, the SIC region, and the isolation between emitter and base can be formed in a self-aligned manner. The only drawback of the DPSA-SEG architecture is that the extrinsic-to-intrinsic base link is formed simultaneously with the SEG of the intrinsic base. As a consequence, the doping of the base link cannot be decoupled from the intrinsic base profile. In particular, attempts to enhance the doping of the base link region by diffusion during subsequent annealing steps has to be traded off against enhanced transit times due to broadening of the intrinsic base profile. It has been demonstrated in [11] that this issue is becoming a showstopper for further enhancement of the RF performance in future BiCMOS generation which target f_{MAX} values of 500 GHz and beyond. This challenge has stimulated the investigation of new device architectures that will be addressed in the following sections.

III. SEG-HBT WITH EPITAXIAL BASE LINK

This section discusses an SEG HBT concept that forms the extrinsic base region by an additional epitaxial process after emitter structuring. This so-called epitaxial base link is crystalline and in-situ boron doped. A detailed description of the EBL fabrication process can be found in [9]. The EBL HBT was compared directly with the conventional DPSA-SEG approach based on identical collector designs, transistor layouts, and measurement conditions in a joint study of IHP and Infineon [12]. In [13], the EBL concept was adopted by Infineon as a candidate for a future 90 nm BiCMOS technology. An alternative approach for an SEG HBT process with improved formation of the base link was proposed by ST Microelectronics [1].

A. Formation of the Base Link

In the classical DPSA-SEG HBT process, the vertical gap between the substrate surface and the base poly-Si is bridged during the selective growth of the base layer (Fig. 2a). Obviously, the base layer and the p+ base poly are separated after base epitaxy by a low-doped region which has to be eliminated by B in-diffusion from the base poly-Si. This issue could be circumvented by the EBL concept. The key idea to form the EBL is illustrated in Fig. 2b. The base link is grown by SEG of B-doped silicon in a cavity that was formed after removing a sacrificial nitride layer below the emitter overhang.

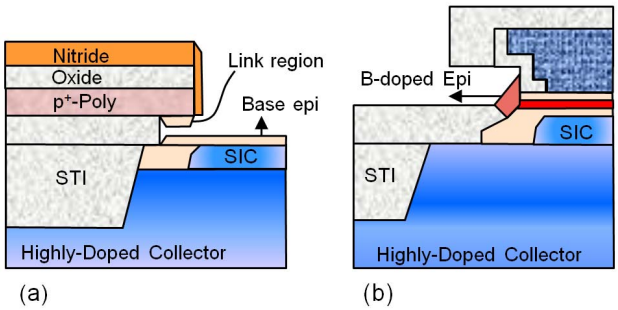

Fig. 2. Schematic flow of the selective epitaxial growth of the base link region in (a) the DPSA and (b) EBL processes.

The final structure of the EBL HBT is shown in the TEM cross section in Fig. 3. The process features self-alignment of the collector window and the extrinsic base regions to the emitter window as it is the case in the DPSA-SEG process. In addition, the overhang of the emitter poly-Si over the emitter window was created in a self-aligned manner helping to reduce C_{BE} and R_B.

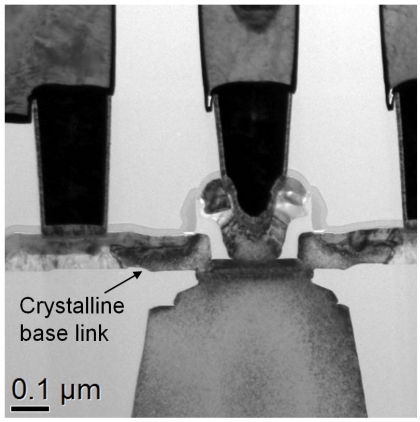

Fig. 3. TEM cross section of an HBT with epitaxial base link (from [12]).

B. Collector Module

The collector construction of typical high-speed Si bipolar transistors includes an epitaxially-buried, highly-doped sub-collector that is laterally isolated by deep trenches. The low-ohmic connection to the collector contact is realized by a so-called collector sinker. This approach was applied for the transistor shown in Fig. 3 which was fabricated in a joint fabrication run where IHP processed the EBL HBT module and Infineon the collector module, deep and shallow trench isolation, CMOS and metallization [12]. This EBL device with the classical collector module demonstrated f_T values of 300 GHz and f_{MAX} values of 500 GHz.

A collector module without deep-trenches and epitaxially-buried sub-collector regions was introduced in [14] in order to reduce fabrication complexity. This process is characterized by implantation of collector wells after shallow trench isolation (STI) and formation of the intrinsic transistor and the collector contact region in one active area. The STI below extrinsic base regions is replaced by a typically less than 100 nm thick oxide layer. This helps to reduce R_C but results in an enhanced extrinsic base-collector capacitance C_{BCx}. Moreover, the absence of deep trenches results in a lower thermal resistance R_{TH}. The original implementation of the EBL HBT used this collector module [9]. Under measurement conditions identical to those of [12], f_T values of 320 GHz and f_{MAX} values of 445 GHz were obtained for the EBL HBT on this collector module. The slightly higher f_T and lower f_{MAX} compared to the device with classical collector module could be related to the lower R_C and R_{TH} and to the higher C_{BC}, respectively.

C. Electrical Characteristics

Starting from the results of [12], further optimization of the emitter structuring and the emitter-base spacer process enabled lateral down-scaling of the effective emitter window width from 130 nm to 100 nm in joint BiCMOS fabrications of IHP and Infineon. The achieved DC- and AC-characteristics are shown in Fig. 4 and Fig. 5, respectively. Cutoff frequencies f_T of 280GHz, f_{MAX} of 575GHz, and CML ring oscillator gate delays of 1.75 ps were demonstrated for HBTs with emitter areas of 0.10x2.65 µm^2. A similar RF performance was achieved in an implementation of the EBL HBT module at Infineon demonstrating f_T values of 305 GHz and f_{MAX} values of 537 GHz [13].

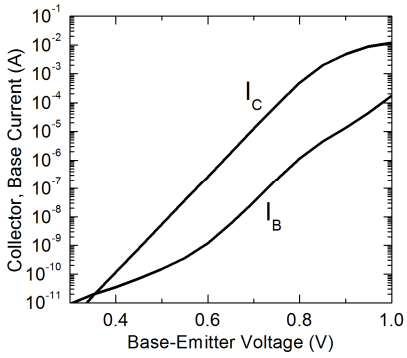

Fig. 4. Gummel characteristics of an HBT with epitaxial base link and an emitter area of 0.10x2.65 µm^2 fabricated in a joint process flow of IHP and Infineon.

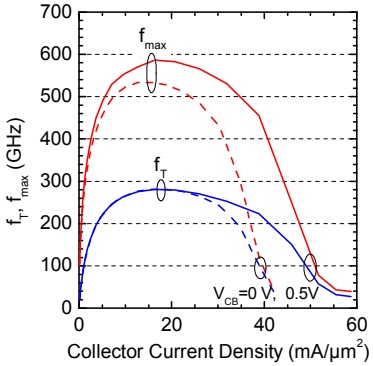

Fig. 5. f_T and f_{MAX} vs. collector curent density for an HBT with epitaxial base link and an emitter area of 0.10x2.65 µm^2 at different base-collector voltages. The HBTs were fabricated in a joint process flow of IHP and Infineon.

IV. NSEG-HBT with Elevated Extrinsic Base

The challenge of forming a low-resistive connection to the internal base simultaneously with low C_{BC} has stimulated the investigation of self-aligned architectures also for SiGe HBTs with non-selective growth of the base [15], [16], [17]. This section discusses results of an NSEG HBT process with elevated extrinsic base (EEB) regions that are formed by selective epitaxial growth of an in-situ B-doped layer after emitter structuring [16]. The EEB architecture was adopted for IHPs 130 nm BiCMOS technologies SG13S [18] and SG13G2 [19]. The recently qualified version of the SG13G2 process features f_T/f_{MAX} values of 350 GHz/450 GHz. Further development of this device concept facilitated the demonstration of f_T/f_{MAX} values of 505 GHz/720 GHz in [6].

A. Device Structure and Fabrication Process

The most advanced version of the EEB process flow was described in detail in [6]. Here, we summarize main features of this device architecture. The EEB-HBT process utilizes the implanted collector module without deep trenches and buried sub-collector regions of [14]. Collector regions are formed by high-dose ion implantation and are laterally confined by STI. Collector windows are defined by deposition and patterning an oxide layer and filling the opened windows by SEG of un-doped Si. Next, selectively implanted collector (SIC) regions are formed before the non-selective growth of the base is performed. The base layer stack grows mono-crystalline in active collector regions and poly-crystalline on top of the isolation oxide as indicated in Fig. 6. After epitaxy, an oxide/nitride/oxide layer stack is deposited and emitter windows are structured. Additional inside spacers are formed before depositing and structuring the As-doped emitter. The emitter is capped with a dielectric layer and structured via a patterned resist mask. Outside spacers are formed on the emitter resulting in the device structure shown in Fig. 6a. Next, the sacrificial nitride layer is removed by wet etching followed by the selective growth of the B-doped elevated extrinsic base regions. The fabrication of the HBT module is finalized with the patterning of the base poly-Si layer via a further resist mask.

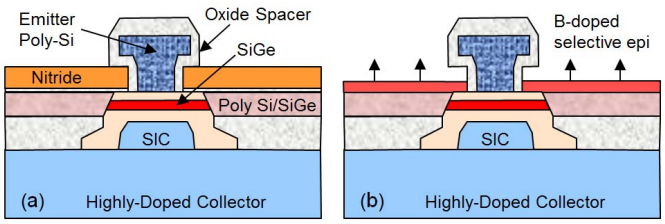

Fig. 6. Schematic flow of the selective epitaxial growth of elevated extrinsic base regions for HBTs with NSEG of the base: (a) before removal of the sacrificial nitride from extrinsic base regions, (b) elevation of the extrinsic base by selective epitaxial growth.

Fig. 7 shows TEM cross sections of the final device structure for an EEB-HBT of the SG13G2 technology and for a scaled device from a wafer of the current BiCMOS process development performed in the TARANTO project. This process targets the integration of HBTs with the performance level of [6] in the 130 nm BiCMOS process of IHP. The fabrication process of the HBT is based on that of the DOT7 device described in [6]. The progress of the RF performance of the DOT7 device compared to SG13G2 was based on a series of process developments which are summarized next. The vertical doping profile was optimized for short transit times by reduced thicknesses of the low-doped base-emitter and base-collector transitions and an increased peak Ge concentration of 32% after deposition and 28% after the full process [20]. Both technology generations take advantage of the suppressed diffusion of boron due to carbon doping. The SiGe layers are doped with about 10^{20} cm^{-3} carbon. Reduced emitter resistance was addressed by enhanced arsenic concentration and reduced thickness of the crystalline emitter. The doping level of the elevated extrinsic bases layer was enhanced and the width of salicide blocking spacers at the sidewalls of the emitters was reduced in order to reduce the extrinsic base resistance. Moreover, the SIC formation was changed from a resist mask in SG13G2 to a hard mask process in DOT7 allowing for an improved control of the width and the doping concentration of the SIC region. In addition, the DOT7 device took advantage of a millisecond flash-annealing step combined with a low-temperature back-end-of-line process with nickel silicide. An enhanced level of dopant activation without significant dopant diffusion is achieved by heating the wafer surface at a millisecond time scale close to the melting temperature. The subsequent thermal budget has to be minimized in order to prevent dopant deactivation. A modified contact formation and the replacement of the $CoSi_2$ process by NiSi helped to avoid temperatures above 500°C after the final activation step. In addition to these process modifications, lateral device dimensions were reduced as summarized in Table I.

The integration of the DOT7 device in the 130 nm BiCMOS process requires several modifications of the process steps for HBT and CMOS fabrication. The ms-flash annealing utilized for the DOT7 device was performed on an experimental tool that has not the maturity required for production-grade processing. That is why it had to be replaced by conventional spike rapid thermal processing (RTP) in the BiCMOS process. In order to limit the impact of the resulting reduction of the level of dopant activation on base resistance, we have carried forward the investigation of a new epitaxial growth process of the base layer that uses disilane instead of silane as precursor gas [21]. The disilane process is advantageous for the realization of low extrinsic base resistance and for further device scaling as discussed in the following subsection. Moreover, the hard mask process for SIC formation had to be modified for HBT yield improvement. In addition to the modifications of the HBT flow, the CMOS process was adjusted to accommodate the new process conditions introduced for best HBT performance. A new gate spacer process was introduced that helped to minimize the width of salicide blocking spaces at emitter sidewalls. The implant conditions for CMOS source/drain extensions and halos were adjusted to re-center CMOS parameters after reducing the final spike RTP temperature and introducing NiSi in order support highest HBT performance.

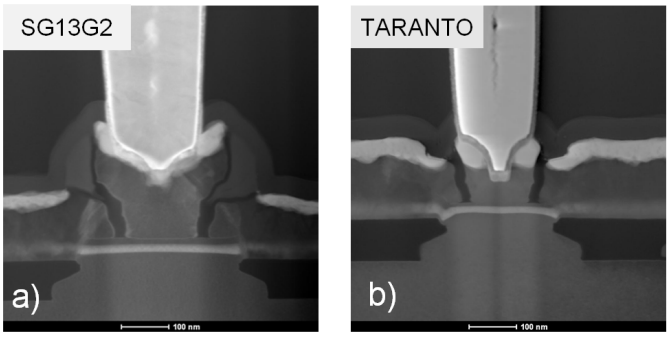

Fig. 7. TEM cross section of an HBT with elevated extrinsic base regions from (a) the SG13G2 process and (b) a current BiCMOS development lot of the TARANTO project.

TABLE I. DEVICE DIMENSIONS AND ELECTRICAL PARAMETERS FOR SEVERAL TECHNOLOGY GENERATIONS. MEASURING CONDITIONS ARE AS GIVEN IN [6].

	Unit	EBL [12]	SG13G2	DOT7 [6]	TARANTO
No. Emitters		3	8	8	8
l_E	µm	2.69	1.02	1	1
w_E	µm	0.13	0.135	0.105	0.11
w_C	µm	0.3	0.33	0.245	0.22
w_{EP}	µm	0.29	0.275	0.195	0.185
f_T	GHz	300	350	505	470
f_{max}	GHz	500	450	720	610
j_C @ peak f_T	mA/µm²	17	18	34	32
Gate delay	ps	1.83	1.90	1.34	1.50
C_{BC}/A_E	fF/µm²	11.2	13.4	18.0	17.4
C_{BE}/A_E	fF/µm²	16.2	15.7	24.3	22.3
$(R_B+R_E)*A_E$	Ωµm²	6.0	8.9	6.3	7.0
R_E*A_E	Ωµm²	n.a.	3.2	1.3	1.3
R_{SBi}	kΩ	3.0	2.8	2.9	4.0
BV_{EBo}	V	1.5	1.6	0.75	1.1
BV_{ECo}	V	1.5	1.6	1.6	1.5
BV_{CEs}	V	4.8	4.3	3.2	3.7

B. Optimization of the Epitaxial Growth of the Base

Optimization of the epitaxial process for the formation of the base layer stack turned out to be essential for further scaling of lateral device dimensions and performance optimization. This concerns in particular the deposition of flat and homogeneous SiGe layers in small collector windows and the formation of a smooth transition between the crystalline layer stack within the collector window and the polycrystalline layer on top of the neighboring oxide regions. Two process options for the base epitaxy which use silane and disilane as Si precursor gases were investigated in this context [21].

The replacement of silane by the higher order precursor disilane results in significantly higher growth rates. As a consequence, lower deposition temperatures are applicable for the disilane process. Silane epitaxy results in crystalline growth on Si areas and poly-crystalline growth on oxide areas. The grain structure of the poly-crystalline layer causes a rough transition line between the poly-crystalline and single-crystalline areas. Disilane epitaxy results in crystalline growth on Si areas and amorphous growth on oxide areas due to the reduced temperature ($T < 550°C$). This is illustrated in Fig. 8 by SEM cross sections of samples for which the epitaxy of the base layer stack was interrupted just before SiGe deposition. The disilane process results in smoother layers outside of the collector windows. In addition, a sharp transition line is formed between the poly and single-crystalline areas. For ideal transistor operation, the emitter window has to be securely positioned inside the unperturbed crystalline Si area within the collector window. The bumpy border line of the crystalline area in the case of silane epitaxy restricts the usable active transistor area in this case. A sharp straight border of the crystalline area is advantageous for minimum overlap of the collector window over the emitter window and thus supports the reduction of the contribution of the device edges to the base-collector capacitance.

A further challenge is the formation of a flat and homogeneous epitaxial layer within the whole collector window. In order to facilitate the use of minimum collector window sizes one has to minimize facet formation at the window edges and avoid twisting of the Si surface along the collector window as present in the images of Fig. 8. These issues are addressed in ongoing experiments by optimizing growth temperature, pre-bake conditions, and partial pressure of HCl and dichlorosilane (DCS) in the selective epitaxial process used for filling up the collector windows. A further important aspect for the formation of facets at the device edges is the orientation of the devices with respect to crystallographic axes. All images shown in Fig. 3, Fig. 7, and Fig. 8 originate from [001] wafers with devices aligned along [100] direction. This corresponds to a 45° rotation of the wafer with respect to traditional CMOS wafers. This wafer orientation results in minimum facet formation along the edges of the devices. However, one can identify facets at the corners of the collector windows which form 45° angles to the [100] and [001] aligned device edges (see Fig. 8).

The control of facet formation at the edges of the emitter window during epitaxy of the collector buffer layer is important for the HBT processes with NSEG of the base as well as for the EBL-SEG processes discussed in Sec. III. In the NSEG HBT process, the emitter window and the collector window are formed by two separate masks. In this case, it is possible to shorten the line edges of the emitter window in order to eliminate imperfect regions at the line edges of the collector window from the intrinsic transistor. This option does not exist for processes with self-aligned emitter and collector windows. There, the extension of the collector window over the emitter window is defined by the width of base-emitter spacers. Consequently, the extensions of the collector window over the emitter window along the emitter stripes and at the end caps of the emitter stripes cannot be varied independently. Therefore, the formation of a collector buffer layer without facets at the end caps of the collector window becomes more crucial for down-scaling the collector window size in the self-aligned processes such as the EBL-SEG process.

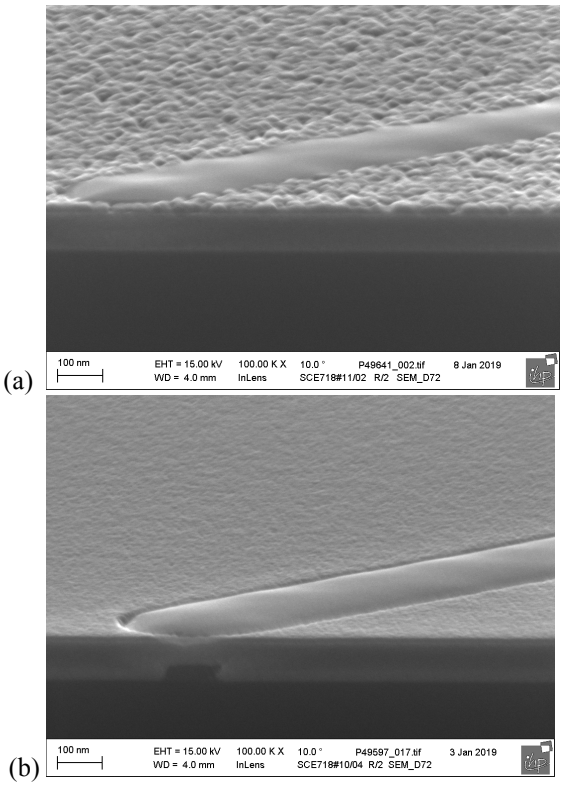

Fig. 8. SEM cross sections with 10° tilt angle of samples after selective epitaxy within the collector window followed by differential epitaxial growth of a Si seed layer on top of the surrounding oxide regions. (a) silane epitaxy, (b) disilane epitaxy.

C. Electrical Characteristics

Table I summarizes device dimensions and basic electrical parameters for the EBL-HBT with selective base epitaxy of [12] and for three variants of the EEB-HBT with non-selective base epitaxy. The DOT7 device demonstrates best values for f_T and f_{MAX} achieved with SiGe HBTs so far. The minimum gate delay of 1.34 ps for current-mode-logic (CML) ring oscillators with the DOT7 device represents the shortest gate delay demonstrated for a SiGe HBT technology so far. Shorter gate delays have not been reported for any other integrated circuit technology.

Fig. 9 depicts f_T and f_{MAX} values as a function of collector current density for a DOT7 device and for an HBT of a BiCMOS wafer that represents an intermediated step of the process development currently carried out in the TARANTO project. The peak f_T values obtained in the BiCMOS process are close to those of the record DOT7 device. However, peak f_{MAX} values are about 100 GHz lower in the present BiCMOS fabrication compared to the DOT7 HBT. This is an indication for a still somewhat higher base resistance in the BiCMOS process with conventional spike RTP and disilane epitaxy compared to the DOT7 process with ms-flash annealing and silane epitaxy.

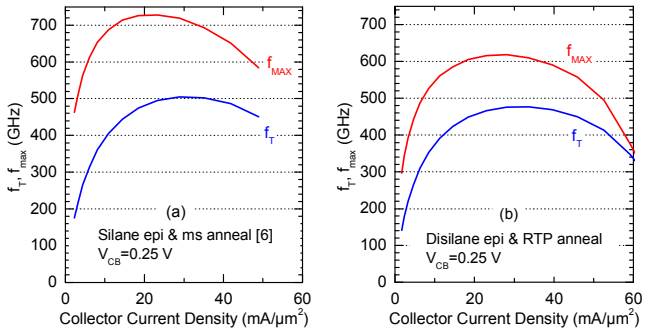

Fig. 9. f_T and f_{MAX} of HBTs with elevated extrinsic base regions: (a) with silane epitaxy of the base ms-flash annealing (from [6]) and (b) with disilane epitaxy of the base and conventional RTP.

The transition from the SG13G2 process to the new device generation resulted in an initial reduction of the yield of HBT arrays. This was caused by the interaction of a series of different factors including the doping level of the emitter, the Ge dose of the base, and the thickness of the Si cap layer above the SiGe. It turned out that the replacement of the $CoSi_2$ salicidation process by a NiSi process helped to recover the HBT yield without deteriorating other transistor properties. The two silicide processes were applied to otherwise identical wafer splits with HBTs of the new process generation. The sheet resistances of the silicide layers on n-type poly-Si are 4.7 Ω/sq. for the $CoSi_2$ process and 4.1 Ω/sq. for the NiSi process. Fig. 10 shows Gummel characteristics of HBT arrays with eight and with 4000 emitters in parallel for a wafer with NiSi and for a wafer with $CoSi_2$, respectively. The eight emitter array with NiSi shows ideal collector currents and nearly ideal base currents for all 55 devices on the 200 mm wafer (Fig. 10a). However, in case of $CoSi_2$, about 10% of the eight emitter devices show non-ideal base currents and one of the 55 devices shows a strongly degraded collector current (Fig. 10Fig. 10b). This is an indication for the generation of crystal defects. The consequences on yield of arrays of 4000 HBTs become clear from Figs. 10c and 10d. Only two of the 4k arrays with NiSi show non-ideal characteristics corresponding to a yield of 96%. In contrast, the wafer with $CoSi_2$ shows acceptable collector currents for only 8% of the 4k arrays.

The yield loss of the HBTs with $CoSi_2$ is largely caused by defect generation due to silicidation. The impact of these defects on HBT yield can be mitigated by thinner $CoSi_2$ and thicker emitter poly layers on cost of larger base and emitter resistances, respectively. Moreover, HBT yield can be impacted by the interplay of the mechanical stability of the HBT with strain generated due to silicidation and the higher thermal budget of the $CoSi_2$ process. The HBTs experience large internal strain due to the high Ge content of the SiGe base layer. In addition, heavily-doped emitter and collector regions can promote the generation of defects. Emitter fabrication and emitter doping concentration can largely impact HBT yield as shown in [22]. Nevertheless, it should be noted that high HBT yield is achievable even for the very aggressive emitter, base, and collector doping profiles used here as demonstrated by the 4k HBT arrays of the NiSi wafer (Fig. 10c).

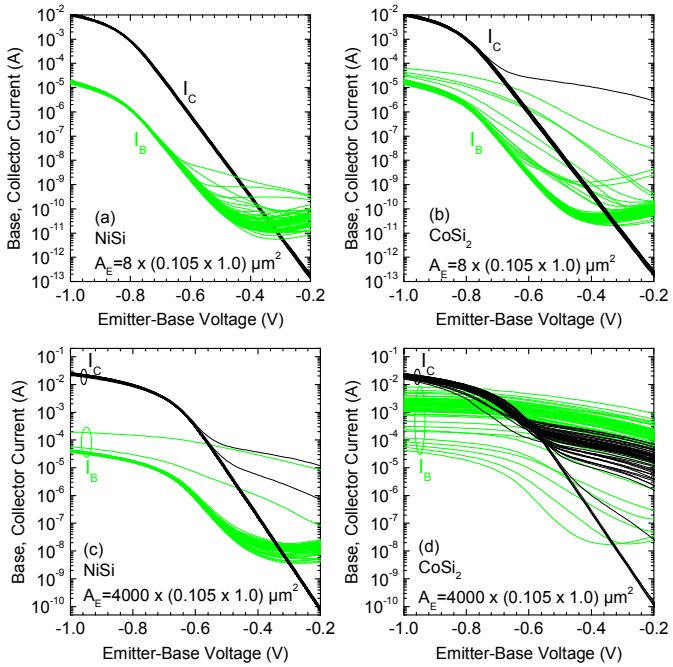

Fig. 10. Gummel characteristics of transistor arrays with 8 HBTs (a), (b) and 4000 HBTs (c), (d) in parallel, respectively. Data is plotted for all 55 chips from a 200 mm wafer for a wafer with NiSi (a), (c) and for a wafer with $CoSi_2$ (b), (d).

V. Conclusions

It was demonstrated that advancements of the device construction of SiGe HBTs and of critical process steps such as base epitaxy have opened up the opportunity for significantly enhanced RF performance in next generation SiGe BiCMOS processes. The formation of extrinsic base region by selective epitaxial growth after emitter structuring was shown to be a practical approach for the realization of a low-resistive connection of the intrinsic base region and thus for increased f_{MAX} values. HBTs with f_T values of 470 GHz and f_{MAX} values of 610 GHz were demonstrated in a 130 nm BiCMOS process with non-selective base epitaxy and elevated extrinsic base regions.

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