An Overview of the Modeling and Simulation of the Single Event Transients at the Circuit Level

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Abstract - The single event transients (SETs) are a common source of malfunction in nano-scale CMOS integrated circuits. For this reason, evaluation of the SET effects and application of appropriate measures for their mitigation are fundamental tasks in the design of advanced radiation hardened integrated circuits. In general, SET analysis is based on the multi-scale modeling and simulation approach comprising four main phases: modeling and simulation of radiation-matter interactions, device-level modeling and simulation, circuit-level modeling and simulation and logic-level modeling and simulation. In order to reduce the time and cost of the evaluation and design processes, a lot of effort is invested into the development of appropriate models which could provide accurate SET simulations at the circuit level. The circuit-level simulations provide a good trade-off between the complexity and speed of simulations, and at the same time ensure very good accuracy. This paper reviews the approaches for modeling and simulation of SET effects at the circuit level, emphasizing the major advantages and disadvantages of each approach.

I. Introduction

Performance of modern CMOS integrated circuits may be severely degraded under radiation exposure. With continuous downscaling of transistor sizes and supply voltage, the sensitivity to single event transients (SETs) has become a major reliability issue for nano-scale CMOS integrated circuits intended for operation under radiation exposure [1 – 4]. A SET is induced when a highly energetic particle, such as a proton, neutron, alpha particle or heavy ion, interacts with the sensitive volume within the target circuit. In general, SETs may occur as a result of cosmic radiation, but also due to radiation originating from sources used in nuclear reactors, scientific research facilities, medical therapy installations, chip packages, etc.

A SET is manifested as the pulsed current flowing through the target node. As a result of the induced pulsed current, a temporary disturbance of the voltage level, i.e. a SET voltage pulse, occurs across the target circuit node [5 – 9]. SET voltage pulses occur in combinational logic, and they pose a threat only if captured by a sequential element (e.g. flip-flop or SRAM). If a SET voltage pulse propagates through the combinational logic and is eventually lathed by a sequential unit, it will be transformed into Single Event Upset (SEU), resulting in data corruption and subsequent malfunction of the circuit or complete system. Thus, the characterization of the SET effects is a major requirement in the design of fault-tolerant circuits and systems.

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Generally, the evaluation of the circuit's sensitivity to SETs can be performed either by the computer-aided multi-scale modeling and simulations or through the controlled irradiation experiments. As the irradiation experiments are very expensive, modeling and simulation is employed as the primary approach, while final evaluation is conducted experimentally. The modeling and simulation methodologies for SET characterization typically comprise four main phases [10, 11]: (1) modeling and simulation of the charge deposition during the radiation-matter interactions (Monte Carlo simulations), (2) modeling and simulation of the SET response of a single transistor (TCAD simulations), (3) modeling and simulation of the SET-induced electrical response of a target logic gate or a circuit (SPICE simulations), and (4) modeling and simulation of the SET-induced logic response (HDL simulations).

Applying the multi-scale modeling and simulation approach for each design would be very time-consuming. In that regard, a lot of effort is devoted to the development of accurate and time-efficient modeling and simulation methodologies. One approach is based on the mixed-mode simulations which combine TCAD and SPICE simulations. However, although it provides good accuracy, the mixed-mode approach is still not sufficiently fast due to TCAD simulations which are computationally expensive. Thus, a lot of effort is devoted to the improvement of the circuit-level SET evaluation methodologies. Since they provide very good accuracy and high execution speed, the circuit-level SET modeling and simulation techniques are widely considered as the optimal methodology for efficient SET effects characterization.

The circuit-level modeling and simulation of SETs is usually based on implementing the pulsed current sources within the target circuit to model the SET-induced charge deposition and collection [10, 11]. By injecting the current pulse into the nodes of a target circuit, the generation and propagation of SET voltage pulse can be studied and the critical charge (minimum charge necessary to cause a SET) can be estimated. Besides a wide range of current injection models, alternative SET models with improved accuracy are investigated. However, while all existing approaches have certain advantages, they also suffer from inherent disadvantages. It is therefore necessary to evaluate thoroughly each SET modeling and simulation approach in order to

choose the most suitable one for characterizing the SET robustness of a particular design.

Although different circuit-level SET modeling and simulation approaches have been proposed in literature, there are no detailed reports on their comparative analysis. A review of the most popular circuit-level SET modeling and simulation methodologies has been published in [12]. However, the analysis in [12] does not cover all available SET modeling and simulation techniques. In that sense, the contribution of this paper will be to provide a detailed review of the existing circuit-level SET modeling and simulation methodologies, particularly addressing their key advantages and disadvantages.

The rest of the paper is organized as follows. Section II describes the fundamental mechanisms underlying the SET effects. Section III presents the classification of the circuit-level SET modeling and simulation approaches. In Sections IV – VIII are discussed the key features of the existing SET modeling and simulation approaches. The comparative analysis of the SET modeling and simulation approaches, emphasizing their most important advantages and disadvantages, is outlined in Section IX.

II. Fundamental Mechanisms of SETs

Understanding the physical mechanisms underlying the SET effects is crucial for accurate modeling and simulation of the SET-induced response of integrated circuits. In modern CMOS integrated circuits, the depletion layers across the reverse biased *p-n* junctions within the NMOS or PMOS transistors are mostly sensitive to ionizing particle strikes [5, 6]. The passage of a high energy particle through the target device results in the deposition of the charge along the particle's track. While some of the induced charge will recombine, the electric field across the reverse biased *p-n* junction will collect the rest of the deposited charge through three main charge collections mechanisms: drift (prompt) collection, funneling collection and diffusion collection [7], as depicted in Figure 1. Besides, the particle strike may trigger the parasitic bipolar structure in CMOS logic, resulting in enhanced charge collection [7].

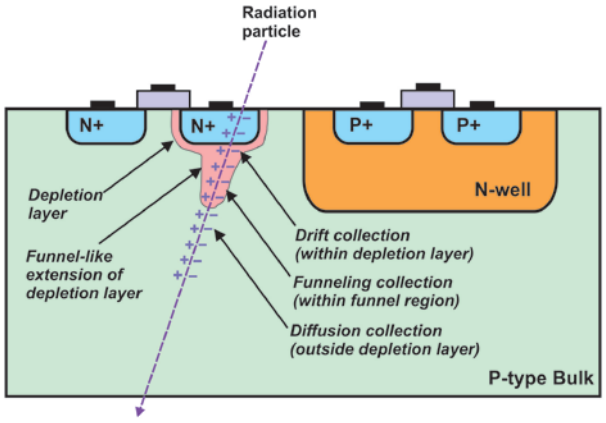

Figure 1. SET mechanisms in CMOS technology

In principle, for CMOS technology which is commonly used in the design of modern integrated circuits, the *off* transistors (NMOS or PMOS) are mostly sensitive to particle strikes. The state of the transistors is determined by the input logic level: low input level implies that NMOS is *off* and PMOS is *on*, while for high input level NMOS is *on* and PMOS is *off*. In Figure 2 is illustrated the SET effect in a CMOS inverter with low input level. When the particle strikes the *off* NMOS transistor, the induced charge is collected by the electric field and transformed into SET current pulse I_{SET}. As a result of the current flow, the output voltage level will be changed. Consequently, the PMOS transistor will act as a restoring element, providing the drive current I_{DRIVE} to dissipate the SET current I_{SET}. In addition, the load gate will provide additional current I_{LOAD} to counteract the SET-induced current.

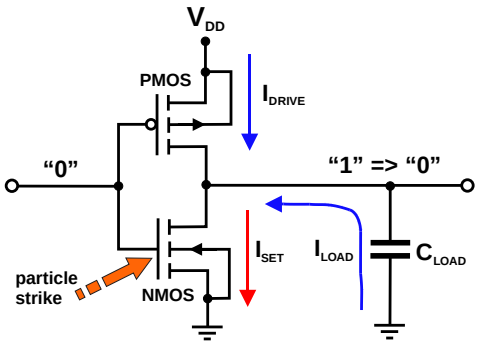

Figure 2. SET-induced response of an inverter

The SET-induced current is a pulsed current with typical duration ranging from dozens of *ps* up to a fraction of *ns*, and with amplitude from several *μA* up to several *mA*. The amplitude and duration of the SET current pulse depends on the charge collection process. When the charge is induced mainly within the depletion layer, the drift and funneling processes will be the dominant charge collection mechanisms, and the induced current pulse will be very short. This occurs when the particle passes directly through the drain of an *off* transistor. Otherwise, if the charge is induced outside the depletion layer, i.e. when the particle strike occurs outside the drain region, the charge collection will primarily be accomplished through the diffusion process. As a result of diffusion collection, the current pulse will be longer because the diffusion collection is slower process than the drift collection.

As a consequence of the current flow through the circuit, the voltage level across the struck node (at the output of target logic gate or circuit) will be deformed. The SET-induced deformation of the voltage level is manifested as a pulse. If the logic state at the output of target gate in normal operation is 0, the SET will induce a positive (0-to-1) pulse. On the other hand, for logic 1 in normal operation the SET will induce a negative (1-to-0) pulse, as illustrated in Figure 2. If the amplitude of the SET voltage pulse swings beyond the threshold level, i.e. beyond the half of supply voltage, the logic level at the output of the target

gate will be altered. Moreover, if the duration of the initial SET voltage pulse is sufficient (larger than the propagation delay of subsequent gates), it may be capable to propagate through the subsequent combinational gates.

As the SET voltage pulse propagates through a combinational chain, its shape may be altered due to electrical and/or logical masking of the subsequent gates [9]. In general, the SET voltage pulse can propagate with or without attenuation, or can be completely filtered. If the SET voltage pulse arrives at the input of a sequential element within the latching window, it will be latched into the sequential element, resulting in a soft error (SEU).

The shape of the SET-induced current pulse and the resulting SET voltage pulse is defined by numerous technological, design, operating and irradiation parameters. The most important factors influencing the SET-induced circuit response are [13 – 16]: irradiation factors (particle energy, direction and location of particle strike), technological factors (doping profiles, carrier lifetime), design factors (transistor size, load capacitance), operating factors (supply voltage, temperature).

With technology downscaling, new physical mechanisms associated with SETs occur, imposing the need for advanced simulation methodologies. An example is the charge sharing effect, which occurs in highly scaled (< 130 nm) technologies. The charge sharing occurs when the passage of a high energy particle results in the charge deposition within two or more transistors, consequently leading to the creation of two separate SET pulses, and possibly resulting in multiple SEUs [8].

Therefore, modeling and simulation of SET effects requires very careful consideration of the impact of all contributing factors in order to predict accurately the response of the target circuit, and accordingly improve the design to achieve sufficient radiation hardness.

III. Classification of SET Modeling And Simulation Approaches

A typical approach for simulating the SET effects on the circuit (transistor) level is by injecting a current pulse in the target node of the circuit. Such analysis is conducted with SPICE-based simulators. Basically, two concepts of modeling the SET-induced current are widely used:

(1) Macro-modeling: current source is implemented as a stand-alone module connected between the output of target gate and the ground, as illustrated in Figure 3.

(2) Micro-modeling: current source is implemented within the target transistor, as illustrated in Figure 4.

In general, the macro-modeling concept is more popular because it is easier for implementation in circuit simulators. On the other hand, the micro-model should be integrated in the target transistor, which requires the modification of the predefined transistor model. Thus, the micro-modeling concept may be applied for SET simulation only when the transistor models are available.

In principle, the same current model may be used for simulating the particle hits in both PMOS and NMOS transistors, and the only difference will be in the direction of the current flow.

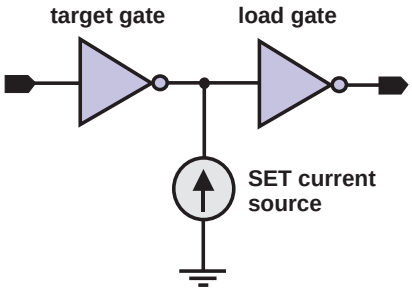

Figure 3. SET macro-model

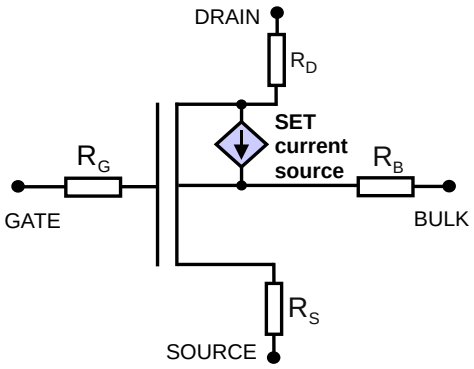

Figure 4. SET micro-model

Numerous models for the SET-induced current have been proposed, and they can be classified into six major groups:

(1) Models based on single voltage-independent current sources.
(2) Models based on voltage-dependent current sources.
(3) Models based on two voltage-independent current sources.
(4) Models based on piecewise interpolation.
(5) Models based on look-up table.
(6) An alternative approach to the current injection models (1) – (5) employs a switch and a series resistor to reproduce the SET response.

All existing modeling and simulation approaches have advantages but also certain drawbacks. It is therefore necessary to consider carefully the key features of each modeling and simulation approach and determine to what extent it could be applicable for evaluating a particular design. In that regard, the following discussion analyzes the benefits and shortcomings of the common SET modeling and simulation approaches, providing useful guidelines for the selection of a suitable approach for a particular design.

IV. Models Based on Single Voltage Independent Current Source

SET models based on voltage-independent current sources are implemented as macro-models, i.e. as stand-alone current sources connected between the target node and the ground terminal. The most common models are described in the following discussion.

A. Double-Exponential Current Model

The double-exponential current pulse, illustrated in Figure 5, is the most widely used model for simulating the SET-induced current. It was proposed by Messenger and can be expressed by the relation [17]:

$$I_{SET}(t) = \frac{Q_{COLL}}{\tau_f - \tau_r}\left(e^{-\frac{t}{\tau_f}} - e^{-\frac{t}{\tau_r}}\right) \quad (1)$$

In relation (1), Q_{COLL} denotes the collected charge, τ_f represents the collection time constant of the junction, and τ_r is the ion-track establishment time constant. Generally, τ_f defines the fall time of the current pulse, while τ_r defines the rise time.

The timing constants τ_f and τ_r are technology-related. According to [18], the time constant τ_f can be expressed by the relation,

$$\tau_f = \frac{k\varepsilon_0\varepsilon_r}{q\mu N_D} \quad (2)$$

where k is the Boltzmann constant, ε_0 is the permittivity of vacuum, ε_r is relative permittivity of silicon, q is the electron charge, μ is the electron mobility, and N_D is the donor density. There is no a straightforward equation to determine the value of τ_r, but it is generally expressed in terms of τ_f. Several different relations have been proposed in literature. For example, $\tau_f = 4\times\tau_r$ in [18], and $\tau_f = 4.6\times\tau_r$ in [19]. In general, the value of τ_r is in the range from several *ps* to tens of *ps*, while the value of τ_f is in the range from tens of *ps* to hundreds of *ps*.

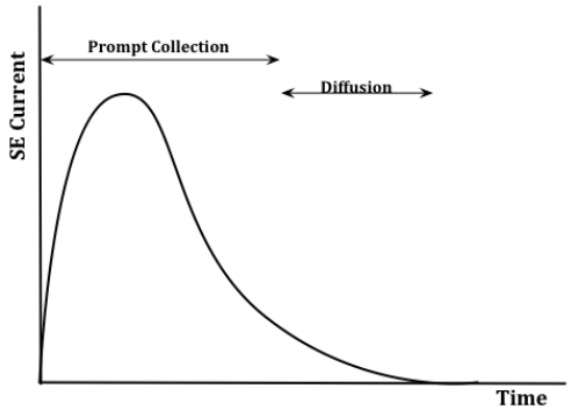

Figure 5. Typical double-exponential current waveform

B. Freeman's Current Model

An alternative exponential model was proposed by Freeman [20]. Freeman's model defines the SET current in terms of the total collected charge Q_{COLL} and a single technology-related timing parameter τ, and it can be expressed as [20],

$$I_{SET}(t) = \frac{2}{\sqrt{\pi}}\frac{Q_{COLL}}{\tau}\sqrt{\frac{t}{\tau}}exp\left(\frac{-t}{\tau}\right) \quad (3)$$

This model has been used for estimating the critical charge of a bipolar memory cell [20], but it can also be utilized for characterization of other logic blocks.

C. Hu's Current Model

Hu [21] derived a model considering the drift and funneling effects, the depletion layer width W and the angle of particle incidence θ, with instantaneous rise-time and fall-time governed by the $cosh^2$ function,

$$I_{SET}(t) = \frac{I_0}{cosh^2\left(\frac{I_0 t cos\theta}{2.5\times10^{-10}W}\right)} \quad (4)$$

In comparison to other voltage-independent current models, Hu's model is the only model which considers the impact of the angle of incidence. However, the potential drawback of this model is that it requires the knowledge of the depletion layer width, which is technology-related and usually not available to the circuit designer.

D. Diffusion Current Model

Diffusion model defines the SET current in terms of pulse amplitude I_{max} and time t_{max} required to reach the amplitude of the current pulse, and it can be expressed by the relation [22],

$$I_{SET}(t) = I_{max}\left(e^{t_{max}/t}\right)^{3/2}\left(e^{-3t_{max}/2t}\right) \quad (5)$$

Diffusion model is useful for simulating the long SET pulses which result from the diffusion collection process, i.e. when the ionizing particle does not cross directly through the drain. It is particularly suitable for modeling the neutron-induced strikes [12].

E. Roche's Current Model

Roche [23] has proposed an exponential current model consisting of two parameters, amplitude I_0 and decay time constant t,

$$I_{SET}(t) = I_0 \cdot e^{-t} \quad (6)$$

The amplitude I_0 is dependent on the electric field intensity within the target device and LET value of the incident particle [24]. This model has lower accuracy in

estimating the critical charge compared to the double exponential, Freeman and diffusion models [24].

F. Rectangular Current Model

The rectangular pulse current model is defined by two parameters: amplitude I_{AMP} and pulse duration T, with zero rising and fall time constants (in practice the rise and fall time constants of several *ps* are used) [25].

$$I_{SET}(t) = \begin{cases} I_{AMP}, & \tau_1 < t < \tau_2 \\ 0, & \tau_1 > t > \tau_2 \end{cases} \quad (7)$$

Although this model ignores the most important physical effects of SETs, it may be useful for estimating the circuit's response to SETs when the physical aspects are not a primary concern. With only two parameters, the rectangular current model is very easy for application in circuit simulations, and it is a suitable choice for initial evaluation of the SET sensitivity. Two common modifications of the rectangular model are: (1) trapezoidal current model which is essentially the rectangular pulse model with realistic values for rising and falling edges (at least 10 *ps*), and (2) triangular current model.

IV. Models Based on Voltage-Dependent Current Sources

The main drawback of the voltage-independent SET current models is that they consider the charge collection in a *p-n* junction with constant bias and without load [26]. In reality the voltage across the *p-n* junction is not constant during the particle strike, but it varies and is dependent on the induced current. If the impact of load and the relation between the injected current and the node voltage are not considered, the total collected charge and the shape of both the SET current pulse and the resulting SET voltage pulse will not be determined accurately. Namely, in the circuit-level SET simulations employing the independent current models, the voltage across the struck node will go beyond the power supply rails for high levels of injected current, which is physically impossible. This phenomenon is known as the voltage override effect.

Numerous reports have confirmed that the SET current waveforms obtained from TCAD simulations do not suffer from the voltage override effect. This is illustrated in Figure 6 which compares the SET voltage pulse obtained with double-exponential current model and with TCAD simulations [26]. The TCAD simulations employ complex models which take into account the effect of both voltage variation and loading. Thus, the current shapes from TCAD simulations are usually used for calibrating the circuit-level current models. The typical current shapes from TCAD simulations are shown in Figure 7 [26]. It can be seen that the shape of the SET-induced current pulse is double-exponential for low LET values, but deviates from the double-exponential shape at higher LET values (e.g. for LET > 10 MeV·cm^2/mg). The induced current pulse has a short high-amplitude current peak followed by a longer plateau region. The amplitude of the plateau region depends on the drive current of the restoring transistor [27], while the duration of the plateau is related to the LET of the incident particle.

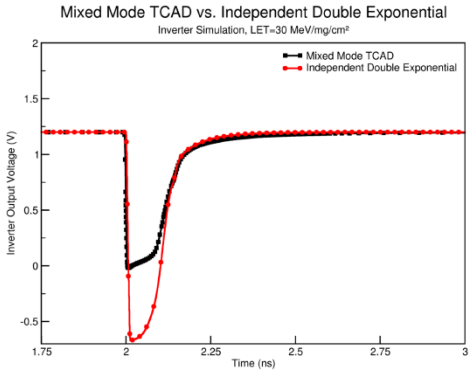

Figure 6. SET voltage pulses obtained with double-exponential current model and TCAD simulations [26]

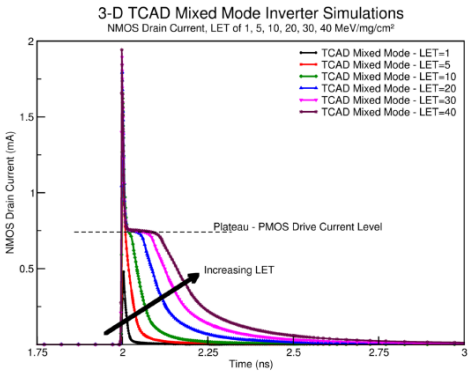

Figure 7. SET current pulses from TCAD simulations [26]

Various models taking into account the dependence of the node voltage on the SET-induced current have been reported in literature [26 – 40]. The following discussion presents the most common voltage-dependent SET current models. In general, the voltage-dependent models can be applied either as macro-models (stand-alone components connected between the target node and ground), or as micro-models integrated within the transistor.

Kauppila et al. [26] introduced a compact voltage-dependent SET current model, as illustrated in Figure 8. This model is described by a set of equations [26] and it is composed of a capacitor C_S, one independent current source I_{SRC} and two voltage-dependent current sources G_{REC} and G_{SEE}. The capacitor C_S stores the charge which is equivalent to the SET-induced charge, and its value can be chosen arbitrarily. The independent current source I_{SRC} is basically the standard double-exponential current source [26]. Two voltage-dependent current sources account for the recombination process and the variation of node voltage due to induced charge.

The model proposed in [26] has been initially developed as a micro-model that can be integrated in the standard transistor models. To validate the approach, the model has been integrated within the BSIM4 and Mextram transistor models for CMOS and HBT transistors in 90 nm CMOS technology. Additionally, the model has been constructed as a Verilog-A module which can be implemented in circuit simulators as a stand-alone current source like the standard voltage-independent models. The current pulse shapes reproduced with this model for 90 nm CMOS technology are in very good agreement with the 3D mixed-mode simulation results [26].

Using the current model proposed by Kauppila et al. enables to accurately characterize the SET-induced current, particularly the plateau observed for high LET values. In addition, the model can account for the parasitic bipolar effect, which is one of its key advantages. However, there are no any reports on the applicability of the model to more scaled technologies. In addition, it is not easy to apply this model as a micro-model since that requires the modification of the transistor models which are not always readily available. However, the possibility to apply the model as a stand-alone current source in standard SPICE simulations provides a very good opportunity to adopt the model to different technologies.

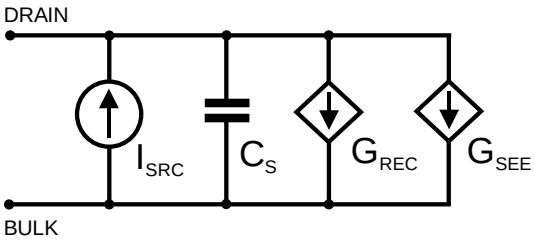

Figure 8. Model proposed by Kaupilla et al. [26]

Clark et al. [28] proposed a voltage-dependent current model based on conventional double-exponential current model. The model is applied in the target circuit as a stand-alone current source, and it is described with a modified double-exponential relation,

$$I_{SET}(t) = k(V_{NODE} - V_{SUB})\left(e^{-\frac{t}{\tau_2}} - e^{-\frac{t}{\tau_1}}\right) \qquad (8)$$

where V_{NODE} denotes the voltage across the target node which varies in accordance with the injected current, V_{SUB} is the substrate voltage which is defined by the supply voltage, and k is technology-related parameter. The value of k is defined by the relation $k = q\mu N/L_f$, where q is the electron charge, μ is the average mobility of carriers in silicon, N is the number of electron-hole pairs generated per unit length, and L_f is the funnel length.

Although the model proposed by Clark et al. takes into account the effect of voltage bias on the amplitude of the SET-induced current, it neglects the fact that the duration of the current pulse also depends on the node voltage [29]. As a consequence of this simplification, the duration of the SET voltage pulse at the output of a target circuit cannot be predicted accurately.

To resolve the drawbacks of the current model defined in [28], Hellebrand et al. proposed a refined current model implemented as a stand-alone current source in Verilog-A [29]. The model is defined by an integral equation,

$$I_{DRIFT}(t) = G \cdot \left(U(t) - \frac{1}{C(t)}\int_0^t I_{DRIFT}(t')dt'\right) \qquad (9)$$

In relation (9), $G = 1/(R_T + R_S)$, where R_T is the resistance of charge track and R_S is the substrate resistance. $C(t)$ and $U(t)$ denote the capacitance and voltage of the node, respectively. The model proposed in [29] considers only the drift collection during the particle strike, while neglecting the diffusion collection. Therefore, it cannot accurately predict the SETs occurring when the particle does not pass directly through the drain.

Alvarado et al. [30] proposed a physics-based voltage-dependent macro-model implemented in Verilog-A, as illustrated in Figure 9. The model has been derived for PD SOI technology, and is based on the use of an internal transistor's node called floating body contact P. The SET current is modelled with the drift-diffusion expression, and is implemented as a voltage-dependent source connected between the floating body contact and the substrate. The fact that the access to an internal node is required may be a limitation in practical uses. In addition, there is no evidence of the applicability to standard bulk CMOS technologies.

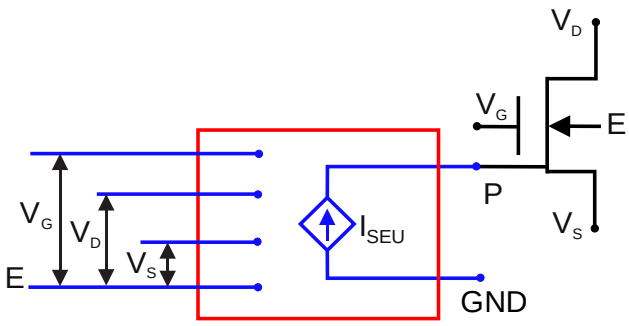

Figure 9. Model proposed by Alvarado et al. [30]

Privat et al. [31] reported a SET current macro-model implemented in Verilog-A, as illustrated in Figure 10. The model is based on multiple dependent current sources, and a capacitor which stores the total collected charge obtained from TCAD simulations. The current sources are described with the Weibull's function. The rationale for using the Weibull function was justified by the fact that the current model should have characteristics that allow simulator convergence, and that can be achieved with the Weibull function. The major advantages of this model are that it is fairly simple, can be used as a stand-alone device in circuit simulations, and provides the accuracy comparable to TCAD simulations. However, the model requires extensive calibration with TCAD simulations for different design and operating settings.

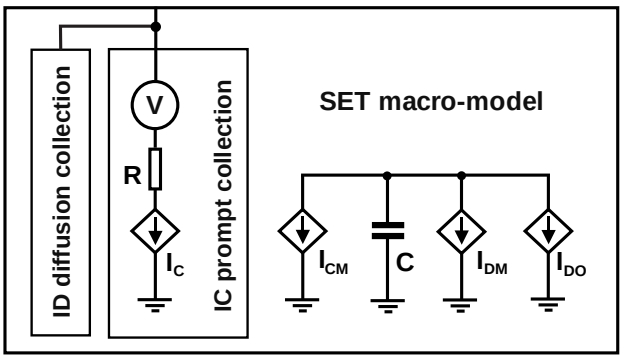

Figure 10. Model proposed by Privat et al. [31]

Mavis et al. proposed an equivalent circuit model (ECM) [32], capable of reproducing the realistic SET current pulse with the plateau effect. The model is based on a series of dependent current and voltage sources connected as stand-alone modules between the target node and ground or power supply rails. Application of the ECM model in circuit simulators is straightforward since it is constructed with the standard SPICE components. Evaluation on 180 nm technology has confirmed very good agreement with the results from 3D simulations [32]. However, one of the key drawbacks of this model is that extensive simulations are required to calibrate the current and voltage sources for every new technology.

Fulkerson et al. have developed a physics-based SET current model [33]. In this model, the ion-struck device is expressed spatially as a mathematical model in which the charge cloud generated by the SET strike is defined by a delta function with magnitude equal to the deposited charge. Using this mathematical representation, the carrier transport (drift and diffusion) equations are solved through Fourier analysis. The obtained solutions are valid for low injection n-type and p-type devices. High-injection solutions are then obtained by solving the same transport expressions numerically. This model can be incorporated in commercial circuit simulator along with the existing SPICE models of BJT which makes possible the inclusion of parasitic BJT effect in circuit simulations. Though physics-based, the model equations are not a function of the drain bias, which means it can be used only as an independent current source.

V. Models Based on Dual Voltage-Independent Current Sources

To resolve the inherent drawbacks of the models with single independent current sources, and provide simpler alternative to the voltage-dependent models, two different approaches using two double-exponential current sources have been proposed [34, 35].

A model utilizing two standard double exponential current sources connected in parallel between the output of target gate and ground, as illustrated in Figure 11, has been proposed by Black et al. [34]. One current source has high amplitude and short duration, while the other has lower amplitude and long duration. Thus, by connecting these two current sources in parallel, the resulting current will be the current pulse with the plateau region as observed in TCAD simulations. The two current sources are defined by one current parameter and three time parameters. The parameters of the current pulses are determined from TCAD simulations. It is important to note that this modeling approach is applicable only when the SET current pulse has a plateau region.

Kleinosowski et al. [35] also proposed the use of two current sources to model the SET effects, as illustrated in Figure 12. However, unlike the solution in [34], where the current sources are connected in parallel between the target node and ground, in [35] one current source is connected between drain and bulk and the other between bulk and source. The direction of the current flow is determined according to the type of target transistor. Both current sources are also described by the standard double exponential model. However, the amplitudes of the current are chosen to be proportional to the drain/source resistances. In that way the model takes into account the differences in the drain and source resistances. Usually, the current from the drain is larger than the current from the source, because of the positive drain voltage which creates a larger electric field that pulls electrons towards the drain terminal.

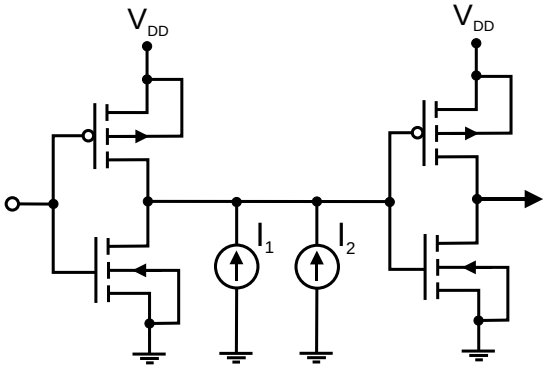

Figure 11. Model proposed by Black et al. [34]

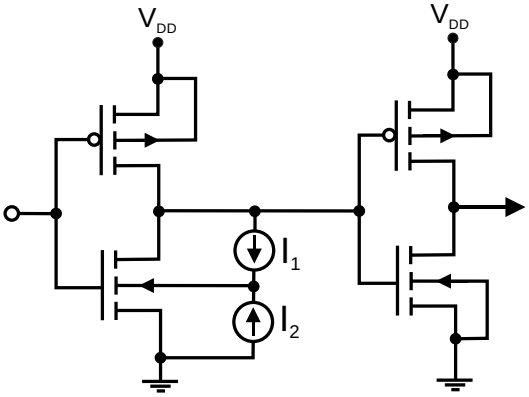

Figure 12. Model proposed by Kleinosowski et al. [35]

VI. Models Based on Piecewise Interpolation

The piecewise approximation method is used to represent a realistic SET current pulse with a number of segments which can be described by simple mathematical relations. Then, the current pulse expressed by the piecewise approximation relations is applied in SPICE simulations as a compact model connected between the target node and ground connection.

Basically, the most common approach is based on the piecewise linear (PWL) approximation, where the SET current pulse obtained from TCAD simulations or irradiation experiments is represented by a number of linear segments. The PWL models are very suitable not only for application in SPICE simulations but also for logic simulation with high level hardware description languages such as VHDL and Verilog. The fundamental PWL models utilize at least 3 linear segments to approximate the SET current [36]. A 3-segment PWL model applied to a double-exponential current pulse is shown in Figure 13.

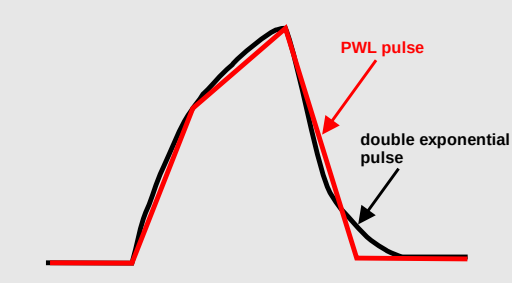

Figure 13. PWL current model

An alternative approach, based on the piecewise quadratic approximation (PWQ) has been proposed by Dharchoudhury et al. [37]. In this case, the SET current waveform obtained from TCAD simulations is represented by a number of segments defined by a second order polynomial. The main advantage of PWQ method over PWL method is that it requires smaller number of segments to represent realistically the SET current pulse.

While both PWL and PWQ models can accurately represent the characteristics of real SET current pulse, they are inherently not scalable to bias conditions, LET values, or device sizes [26]. This implies that TCAD simulations or experimental calibrations should be performed for each new device under test or new technology in order to define the parameters of the interpolation functions.

VII. Models Based on Look-up Table

The concept of modeling the SET-induced current with a look-up table (LUT) has been proposed as a very promising approach encompassing the accuracy of TCAD simulations and the speed of circuit simulations [38, 39]. Basically, the idea of the LUT-based SET modeling is to extract the SET current waveforms for different design and operating set-tings from TCAD simulations or irradiation experiments, and store the obtained data in the LUT. Then, the circuit simulators can construct the SET pulses by reading the data stored in the LUT.

In [38], a two-dimensional LUT is constructed by expressing the SET current values in terms of the node voltage and collected charge. The LUT readout is performed with a custom-developed SPICE model. The solution proposed in [39] employs Verilog-A to construct a LUT containing the SET current values in terms of the supply voltage and time. The LUT is then coupled to the SPICE simulator as depicted in Figure 14. While the LUT-based models provide benefits in accuracy and speed, their limitations are that a large LUT is required to cover a wide range of design and operating conditions, and TCAD or experimental calibration is required for each device.

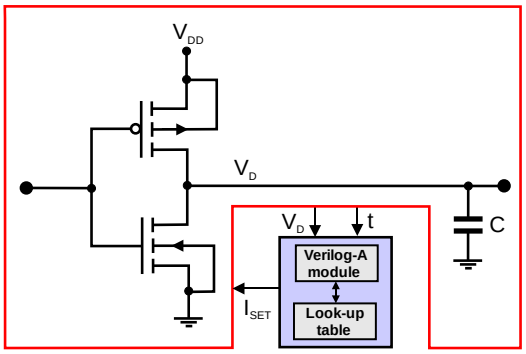

Figure 14. LUT model implemented in Verilog-A [39]

VIII. Models Based on Switch and Resistor

Makihara et al. [40] have proposed a new SET simulation technique based a switch and a series resistor instead of the current source. This concept does not reproduce directly the SET current pulse, but rather the SET voltage pulse. The on-time of the switch defines the duration of the SET voltage pulse, while the resistance defines the pulse amplitude. A typical implementation of this SET modeling concept is depicted in Figure 15.

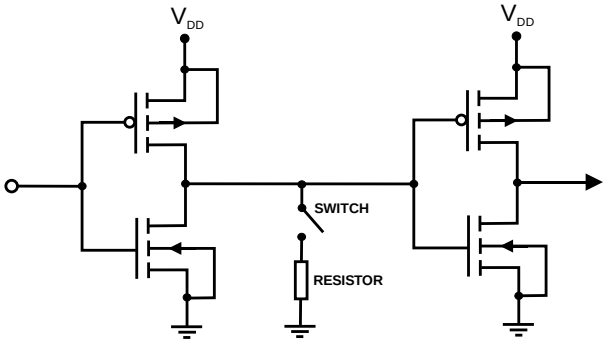

Figure 15: Model proposed by Makihara et al. [40]

The setup in Figure 15 is used to simulate the 1-to-0 SET voltage pulse. For simulation of 0-to-1 SET voltage pulse, the switch and resistor should be connected between the target node and the supply rail. This approach can reproduce the SET response for both lower and higher LETs, and the results are in good agreement with TCAD simulations [40]. To apply the model in SPICE simulations, it is necessary to calibrate the resistance and the on-time of the switch using the reference data obtained from TCAD simulations. Ref. [12] has proposed a modified approach based on a variable resistance instead of a fixed one, thus allowing more accurate reproduction of the SET response.

IX. Comparative Analysis of SET Modeling and Simulation Approaches

Each of the analyzed SET modeling and simulation approaches has both advantages and disadvantages, which should be considered in practical applications. The major advantages and disadvantages of analyzed methodologies are outlined in Table I.

TABLE I
COMPARISON OF SET CURRENT MODELS

Model type	Advantages	Disadvantages
Models based on single voltage-independent current sources	Represented by simple relations Can be easily implemented in SPICE simulations	Not very accurate because the dependence between induced current and node voltage is not considered
Models based on voltage-dependent current sources	Reproduce realistic SET effects Accuracy close to TCAD simulations	Not easy for implementation Extensive calibrations are required
Models based on multiple independent current sources	Can be easily implemented in SPICE simulations Accuracy close to TCAD simulations	Circuit or device simulation are required for calibrating the model
Models based on piecewise interpolation	Can be easily implemented in SPICE simulations More accurate than independent models	Device simulations are required for calibrating the model
Models based on look-up table	Can be easily implemented in SPICE simulations More accurate than independent and PWL models	Device simulations or experiments are required for calibrating the model
Models based on switch and resistor	Can be easily implemented in SPICE simulations Accuracy close to TCAD simulations	Device simulations are required for calibrating the model

From previous discussion it can be seen that the most accurate representation of the SET effects can be obtained with the models which can reproduce the dependence between the SET current pulse and the resulting SET voltage pulse. However, implementation of the voltage-dependent models in SPICE simulations is still not optimal because extensive calibrations are required. Therefore, the SET current models based on independent current source are still widely used, while a lot of effort is put into the development of accurate voltage-dependent SET models which can be easily applied in simulations.

X. Conclusion

The circuit-level modeling and simulation of SET effects is essential for understanding the operation of the circuits under radiation exposure, and accordingly for the design of appropriate techniques for mitigating the SET effects. This paper reviews the common methodologies for modeling and simulation of SET effects on the circuit level. For each approach, the most important implementation details and the key advantages and disadvantages have been outlined. The presented comparative analysis provides useful guidelines for the selection of appropriate modeling and simulation methodology for a particular application.

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References

[1] E. Normand, “Single Event Upset at Ground Level,” *IEEE Trans. on Nuclear Science*, vol. NS-43, 1996, pp. 2742 – 2750.

[2] L. Rockett, “Designing CMOS Data Cells for Space Systems,” *Microel. Journal*, vol. 35, 2004, pp. 953 – 967.

[3] R. Baumann, “Soft Errors in Advanced Computer Systems,” *IEEE Design and Test of Computers*, vol. 22, 2005, pp. 258 – 266.

[4] J. M. Benedetto, P. H. Eaton, D. G. Mavis, M. Gadlage, T. Turflinger, “Digital Single Event Transient Trends with Technology Node Scaling,” *IEEE Transactions on Nuclear Science*, vol. 53, 2006, pp. 3462 – 3465.

[5] P. V. Dressendorfer, “Basic Mechanisms for the New Millennium,” *IEEE NSREC Short Course*, 1998.

[6] T. Weatherford, “From Carriers to Contacts, a Review of SEE Charge Collection Processes in Devices,” *IEEE NSREC Short Course*, 2002.

[7] P. Dodd, L. Massengill, “Basic Mechanisms and Modeling of Single Event Upset in Digital Microelectronics,” *IEEE Trans. on Nuclear Science*, vol. 50, 2003, pp. 583 – 602.

[8] V. Ferlet-Carvois, L. W. Massengill, P. Gouker, “Single Event Transients in Digital CMOS - A Review,” *IEEE Trans. on Nuclear Science*, vol. 60, 2013, pp. 1767 – 1790.

[9] T. Karnik, P. Hazucha, J. Patel, “Characterization of Soft Errors Caused by Single Event Upsets in CMOS Processes,” *IEEE Trans. on Dependable and Secure Computing*, vol. 1, 2004, pp. 128 – 143.

[10] D. Munteanu, J. L. Autran, "Modeling and Simulation of Single Event Effects in Digital Devices and ICs," *IEEE Trans. on Nuclear Science*, vol. 55, 2008, pp. 1854 – 1878.

[11] Y. Suge et al. "Modeling and Simulation of Single-Event Effect in CMOS Circuit," *Journal of Semiconductors*, vol. 36, 2015, pp. 1 – 10.

[12] K. R. Pasupathy, B. Bindu, "A Review on Circuit Simulation Techniques of Single Event Transients and Their Propagation in Delay Locked Loop," *IETE Technical Review*, vol. 34, 2016, pp. 276 – 285.

[13] T. Heijmen, D. Giot, P. Roche, "Factors That Impact the Critical Charge of Memory Elements," *Proc. 12th IEEE International Online Testing Symposium*, Lake Como, Italy, 2006, pp. 1 – 6.

[14] S. Bota, G. Torrens, B. Alorda, J. Segura, "Critical Charge Characterization in 6-T SRAMs During Read Mode," *Proc. 15th IEEE International Online Testing Symposium*, Lisbon, Portugal, 2009, pp. 120 – 125.

[15] Q. Zhou, K. Mohanram, "Gate Sizing to Radiation Harden Combinational Logic," *IEEE Trans. on Computer-aided Design of Integrated Circuits and Systems*, vol. 25, 2006, pp. 155 – 166.

[16] M. Bagatin et al., "Temperature Dependence on Neutron-induced Soft Errors in SRAMs," *Microelectronics Reliability*, vol. 52, 2012, pp. 289 – 293.

[17] G. C. Messenger, "Collection of Charge on Junction Nodes from Ion Tracks," *IEEE Trans. on Nuclear Science*, vol. Ns-29, 1982, pp. 2024 – 2031.

[18] D. Limbrick, W. Robinson, "Characterizing Single Event Transient Pulse Widths in an Open-Source Cell Library Using SPICE," *Proc. 8th Workshop on Silicon Errors in Logic – System Effects*, Illinois, USA, 2012, pp. 1 – 4.

[19] F. Wrobel, L. Dilillo, A. D. Touboul, V. Pouget, and F. Saigne, "Determining Realistic Parameters for the Double Exponential Law that Models Transient Current Pulses," *IEEE Trans. on Nuclear Science*, vol. 61, 2014, pp. 1813 – 1818.

[20] L. B. Freeman, "Critical Charge Calculations for a Bipolar SRAM Array," *IBM Journal of Research and Development*, vol. 40, 1996, pp. 119 – 129.

[21] C. Hu, "Alpha Particle Induced Field and Enhanced Collection of Carriers," *IEEE Electron Device Letters*, vol. 3, 1982, pp. 31 – 34.

[22] T. Merelle et al., "Criterion for SEU Occurrence in SRAM Deduced from Circuit and Device Simulations in Case of Neutron-Induced SER," *IEEE Trans. on Nuclear Science*, vol. 52, 2005, pp. 1148 – 1155.

[23] P. Roche, L. M. Palau, G. Bruguier, C. Tavernier, R. Ecoffet, J. Gasiot, "Determination of Key Parameters for SEU Occurrence Using 3D Full Cell SRAM Simulators," *IEEE Trans. on Nuclear Science*, vol. 46, 1999, pp. 1354 – 1362.

[24] R. Naseer, Y. Boulghassoul, J. Draper, S. DasGupta, A. Witulski, "Critical Charge Characterization for Soft Error Rate Modeling in 90 nm SRAM," *Proc. IEEE International Symposium on Circuits and System*, New Orleans, USA, 2007, pp. 1879 – 1882.

[25] B. Zhang, A. Araposthatis, S. Nassif, M. Orshansky, "Analytical Modeling of SRAM Dynamic Stability," *Proc. IEEE International Conference on Computer-Aided Design*, San Jose, USA, 2006, pp. 315 – 322.

[26] J. S. Kauppila et al., "A Bias-Dependent Single-Event Compact Model Implemented into BSIM4 and a 90 nm CMOS Process Design Kit," *IEEE Trans. on Nuclear Science*, Vol. 56, 2009, pp. 3152 – 3157.

[27] D. Kobayashi, T. Makino, K. Hirose, "Analytical Expression for Temporal Width Characterization of Radiation-induced Pulse Noises in SOI CMOS Logic Gates," *Proc. IEEE Intern. Physics Reliability Symposium*, 2009, pp. 165 – 169.

[28] K. A. Clark et al., "Modeling Single Event Effects in a Complex Digital Device," *IEEE Trans. on Nuclear Science*, vol. 50, 2003, pp. 2069 – 2080.

[29] S. Hellebrand et al., "A Refined Electrical Model for Particle Strikes and its Impact on SEU Prediction," *Proc. 22nd IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Rome, Italy, 2007, pp. 50 – 58.

[30] J. Alvarado, V. Kilchytska, G. Berger, D. Flandre, "Efficient Single Event Upset Simulations of a Tolerant PD SOI CMOS D flip-flop," *Proc. Conference on Radiation and its Effects on Components and Circuits*, Bruges, Belgium, 2009, pp. 225 – 229.

[31] A. Privat, L. T. Clark, "Simple and Accurate Single Event Charge Collection Macro Modeling for Circuit Simulations," *Proc. IEEE International Symposium on Circuits and Systems*, Lisbon, Portugal, 2015, pp. 1858 – 1861.

[32] D. G. Mavis, P. H. Eaton, "SEU and SET Modeling and Mitigation in Deep Submicron Technologies," *Proc. IEEE Inter. Reliability Physics Symposium*, Phoenix, USA, 2007, pp. 293 – 305.

[33] D. E. Fulkerson, E. E. Vogt, "Prediction of SOI Single Event Effects Using a Simple Physics Based SPICE Model," *IEEE Trans. on Nuclear Science*, vol. 51, 2005, pp. 2168 – 2174.

[34] D. A. Black et al., "Modeling of Single Event Transients with Dual Double-Exponential Current Sources," *IEEE Trans. on Nuclear Science*, vol. 62, 2015, pp. 1540 – 1549.

[35] A. Kleinosowski, P. Oldiges, P. Solomon, R. Williams, "Method for Soft Error Modeling with Double Current Pulse," Patent, Dec. 2009, US Patent 7 627 840.

[36] A. M. Francis, M. Turowski, J. A. Holmes, H. A. Mantooth, "Efficient Modeling of Single Event Transients Directly in Compact Device Models," *Proc. IEEE International Behavioral Modeling and Simulation Workshop*, San Jose, USA, 2007, pp. 73 – 77.

[37] A. Dharchoudhury, S. M. Kang, H. Cha, J. H. Patel, "Fast Timing Simulation of Transient Faults in Digital Circuits," *Proc. IEEE/ACM International Conference on Computer-Aided Design*, San Jose, USA, 1994, pp. 719 – 726.

[38] Z. Xueqian, Z. Zhenyu, Z. Minxuan, L. Shaoqinq, "Verilog-A Based Implementation for Coupled Model of Single Event Transients in Look-up Table Technique," *Proc. 8th IEEE International Conference on ASIC*, Changsha, China, 2009, pp. 666 – 669.

[39] C. Shuming, L. Biwei, L. Bin, "Coupled SET Pulses Modeling Based on LUT in Ultra-deep Submicron Technology," *Proc. IEEE Region 10 TENCON Conference*, Hyderabad, India, 2008, pp. 1 – 5.

[40] A. Makihara et al., "New SET Characterization Technique Using SPICE for Fully Depleted CMOS/SOI Digital Circuitry," *IEEE Trans. on Nuclear Science*, vol. 55, 2008, pp. 2921 – 2927.