Impact of inter-cell and intra-cell variability on forming and switching parameters in RRAM arrays

Alessandro Grossi, Damian Walczyk, *Member, IEEE,* Cristian Zambelli, *Member, IEEE,* Enrique Miranda, *Senior Member, IEEE,* Piero Olivo, Valeriy Stikanov, Alessandro Feriani, Jordi Suñé, *Fellow, IEEE,* Gunter Schoof, Rolf Kraemer, Bernd Tillack, Alexander Fox, Thomas Schroeder, Christian Wenger, and Christian Walczyk

***Abstract*—The inter-cell variability of the initial state and the impact of d.c. and pulse forming on inter-cell variability as well as on intra-cell variability in TiN/HfO_2/Ti/TiN 1T-1R devices in 4 kbit memory arrays were investigated. Nearly 78% of devices on particular arrays were d.c. formed with a wordline voltage V_{WL} = 1.4 V and a bitline voltage V_{BL} = 2.3 V, whereas 22% devices were not formed due to the combined effect of the extrinsic process-induced inter-cell variability of the initial state and intrinsic inter-cell variability after d.c. forming. Furthermore, pulse-induced forming with pulse widths on the order of 10 μs (V_{WL} = 1.4 V, V_{BL} = 3.5 V) caused for 86% of devices a low resistance state. Using a retry algorithm, we achieve 100 % of formed devices. To assess and confirm the nature of the variability during forming operation and during cycling the quantum point-contact (QPC) model was considered. The modeling results demonstrate a relationship between the forming and the device performance. The cells requiring large energy for forming operation, due to impurities in the HfO_2 deposition during array processing, are those subject to poor switching performance, larger variability, and faster wear-out. Devices formed by pulse-retry algorithm show (i) shorter endurance and (ii) higher variability during cycling.**

***Index Terms*—4 kbit RRAM array, Inter-cell variability, Intra-cell variability, Hafnium dioxide (HfO_2), Pulse-induced forming, Quantum point-contact (QPC) model.**

I. Introduction

RECENT advances in the performance of resistive random access memory (RRAM) have led to significant interest in system-on-chip applications in Si-based CMOS technologies, in particular for microcontrollers in wireless sensor nodes and in automotive electronics [1], [2]. For sensor nodes, the integration of energy-efficient microcontrollers with RRAM could provide the prospect of completely autonomous systems. In electric cars, energy-efficient microcontrollers for internal states storage in complex control units are inevitable due to the relatively low energy supply resources. Hence, recent hardware-based approaches focus on the integration of HfO_2-based RRAM in a microcontroller unit [3]. HfO_2 is one of the most promising transition metal oxides for RRAM with an ideal CMOS back-end-of-line compatibility. Thus considerable progress has been made in 1T-1R device integration as well as in understanding the physical/chemical properties of the resistance change behavior. Although memory arrays in the 1T-1R architecture demonstrated excellent performance parameters [4]–[7], the inter-cell variability (variations between cells) and intra-cell variability (cycle-to-cycle variations of any given cell) still prevents RRAM manufacturing from fast commercialization. While the intra-cell variability can be optimized for the particular memory cells, the inter-cell variability in memory arrays must be minimized [8]. Hence, several investigations on the extrinsic process-induced and intrinsic microscopic origin of the inter-cell and intra-cell variability after forming have been carried out in the recent past [9]–[14]. In this work, however, we first investigate the inter-cell variability of the initial state in memory arrays and then study the impact of d.c. and pulse forming on inter-cell variability as well as on intra-cell variability. To assess and confirm the nature of the variability during forming operation and during cycling the quantum point-contact (QPC) model was considered.

D. Walczyk, G. Schoof, R. Kraemer, B. Tillack, A. Fox, T. Schroeder, Ch. Wenger, and Ch. Walczyk are with IHP, 15236 Frankfurt (Oder), Germany (e-mail: walczykd@ihp-microelectronics.com).

C. Zambelli, A. Grossi, and P. Olivo are with the Department Ingegneria ENDIF, Universitá degli Studi di Ferrara, Via G. Saragat, 44122 Ferrara, Italy.

E. Miranda and J. Suñé are with the Departament d'Enginyeria Electrónica, Universitat Autónoma de Barcelona, Campus UAB, Cerdanyola del Valles, 08193 Barcelona, Spain.

V. Stikanov is with IASA, 37 Prospect Peremogy, 03056 Kiev, Ukraine.

A. Feriani is with NplusT Semiconductor Application Center, Via Umbria 112, 06132 San Martino in Colle (PG), Italy.

B. Tillack is also with the Department of Computer Engineering and Microelectronics, Technische Universität Berlin, 10587 Berlin, Germany.

R. Kraemer and T. Schroeder are also with the Brandenburgische Technische Universität, Konrad-Zuse-Strasse 1, 03046 Cottbus, Germany.

II. Devices and Experiments

The bottom metal electrode of 150 nm TiN with a sheet resistance of 10-50 Ω/sq was prepared by physical vapor deposition (PVD) sputtering. 9 nm HfO_2 was deposited at 320 °C by the reaction of O_2 and tetrakis(ethylmethylamido)hafnium ($Hf(NMeEt)_4$) onto TiN in an atomic vapor deposition (AVD) chamber. Finally, HfO_2 was capped by 7 nm ionized metal plasma (IMP) Ti and 150 nm PVD TiN [15]. To investigate the impact of inter-cell and intra-cell variability, 4 kbit RRAM arrays with 600×600 nm^2 MIM area and with 890×965 nm^2 1T-1R area were processed [16]–[18]. Memory array characterization was performed for 20 packaged memory arrays on a dedicated automated Active Technologies RIFLE system [16].

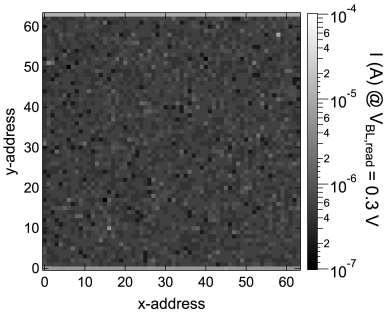
III. Results and Discussion

A. Inter-cell variability in initial state and after d.c. forming

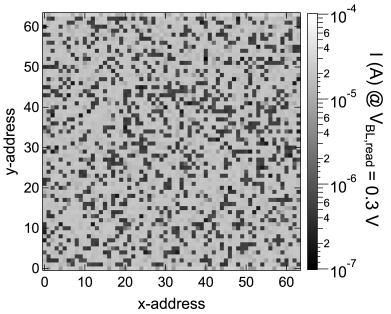
In this section, we present the influence of the d.c. forming process on the inter-cell variability. Forming was a prerequisite to induce stable resistance changes in our devices. This process

TABLE I
SUMMARY OF DC FORMING, PULSE-INDUCED FORMING, PULSE-RETRY FORMING, DC-RETRY FORMING, SET/RESET AND READ VOLTAGES.

	Bitline (BL) voltage V_{BL}	Sourceline (SL) voltage V_{SL}	Wordline (WL) voltage V_{WL}	Bitline (BL) pulse width $t_{BL,\,pulse}$/ Bitline (BL) sweep time
d.c. forming	0 V - 2.3 V	0 V	1.4 V	23 s
d.c. Set	0 V - 2.3 V	0 V	1.4 V	23 s
d.c. Reset	0 V	0 V - 2.3 V	2.2 V	23 s
Pulse-induced forming	3.5 V	0 V	1.4 V	10 μs
Pulse-retry forming	3.5 V	0 V	1.4 V	10 μs
d.c. retry forming	0 V - 3.5 V	0 V	1.4 V	-
Pulse set cycling	3 V	0 V	1.4 V	10 μs
Pulse reset cycling	0 V	3 V	2.2 V	10 μs
Reading	0.3 V	0 V	1.4 V	-



(a)



(b)

Fig. 1. Current distributions for a 64 × 64 bit (4 kbit) RRAM array with 1T-1R devices with 600 × 600 nm^2 MIM area. (a) Initial state. (b) After forming in d.c. step sweep. The gate-source voltage was set to V_{WL} = 1.4 V with a bitline voltage sweep to V_{BL} = 2.3 V with ramp rate dV/dt = 0.1 Vs^{-1}. Current reading was performed at V_{WL} = 1.4 V and $V_{BL,\,read}$ = 0.3 V.

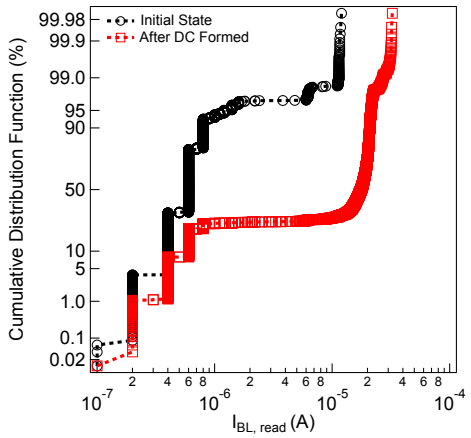
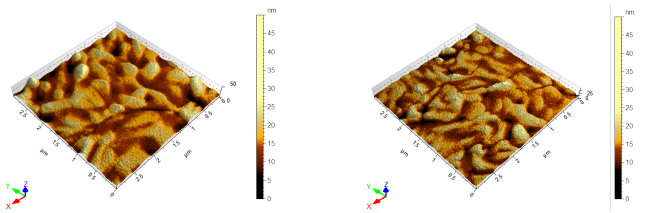


Fig. 2. Statistical current distributions of the initial state and after forming in d.c. step sweep. Current reading was performed at V_{WL} = 1.4 V and $V_{BL,\,read}$ = 0.3 V.

consists in the application of a d.c. step sweep on the bitline (BL) to V_{BL} = 2.3 V as well as grounding the sourceline (SL) V_{SL} = 0 V. In contrast to d.c. voltage sweeps, current-driven d.c. step sweeps result in more reliable transitions into the bipolar switching mode in 1R devices by avoiding overshoot issues [19]. To prevent hard breakdown, the saturation current of the select transistor is controlled by the wordline (WL) voltage at V_{WL} = 1.4 V. Table I summarizes the forming, set/reset and reading parameters in this work. In general, the forming process produces a non-destructive soft breakdown and progressive breakdown regime of the dielectric and requires a sufficiently high electric field across the HfO_2 film thickness [20], [22], [23]. Due to the stochastic nature of the forming process or due to process-induced variations, the inter-cell variability of memory elements in a 4 kbit memory array cannot be neglected. To address this point, we first show in Fig. 1 the current distribution in the initial state which is defined by the combination of the Ti and HfO_2 film thicknesses [18] and the current distribution after d.c. forming.

Statistical analysis in a cumulative distribution function plot in Fig. 2 reveals that only 78 % of the devices (red curve) were successfully formed by the d.c. step sweep, whereas 22% devices were not formed due to the high inter-cell variability of the initial state current. The thickness inhomogeneity of the PVD Ti layer with $\sigma < 5\%$ standard deviation over the whole wafer diameter is believed not to play a central role in the inter-cell variability of the initial currents in Fig. 2 since the memory array with circuitry area is 365 × 752 μm^2. When compared with Ti, the thickness inhomogeneity of the HfO_2 film with $\sigma < 2\%$ standard deviation should also be insignificant for the initial current inter-cell variability [24]. One reason could be the root mean square surface roughness of HfO_2 films due to the columnar structure of the TiN bottom metal electrode [25], although a post-metallization annealing (PMA) step was applied which was reported to reduce the surface roughness [26]. To support this hypothesis it is shown in Fig. 3 the different root mean square values of the roughness profiles extracted from TiN and HfO_2 films used in RRAM arrays processing. The randomly distributed inter-cell variability after



(a) (b)

Fig. 3. Roughness profile of the TiN (a) and HfO_2 (b) films used in the array processing.

forming in d.c. step sweep is often related to intrinsic processes which involve microscopic transport of oxygen vacancies and permutations of filamentary clusters [9], [27], [28].

B. Inter-cell variability in initial state and after pulse-induced forming

Recently, the pulse-induced forming has attracted wide attention as an alternative to d.c. forming. This pulse forming mode may reduce the operation current and the energy per unit volume imparted to the dielectric [29], [30]. Moreover, the forming time for the whole memory array can be reduced. To understand the pulse-induced forming process in more detail, we varied the forming parameters, namely V_{WL}, V_{BL}, and the voltage pulse width $t_{BL,\ pulse}$ on an adjacent memory array. For V_{WL} = 1.4 V, V_{BL} = 3.5 V, and $t_{BL,\ pulse}$ = 10 μs, devices were formed, which is comparable to d.c. forming (see Fig. 2). V_{WL}, V_{BL} in conjunction with $t_{BL,\ pulse}$ are critical parameters to initiate the pulse-induced forming process. Simplified analytical models reproduce the statistical distribution of the forming voltage V_{BL} for each device in the memory array [31], [32]. The pulse-induced forming energy density (voltage $\times$ current $\times$ time/area) imparted to the dielectric for each cell reaches an average value of 1.9×10^{-9} J/μm^2 in comparison to 3.7×10^{-3} J/μm^2 after d.c. forming.

From a physical point of view, the pulse-induced forming may be appreciated with the shape of the created conductive filament: while pulses with low V_{WL} and V_{BL} voltages or short pulse width $t_{BL,\ pulse}$ create narrow filaments showing low currents, higher V_{WL} and V_{BL} voltages or long pulse width $t_{BL,\ pulse}$ create stable and wider filaments [33]. The filament diameter and areal density may be correlated with the concentration of oxygen vacancies that are supposed to participate in the filament formation process. The oxygen vacancies are predominantly produced at the Ti metal electrode as the result of redox processes of the oxide by the Ti metal electrode [34]–[36].

We applied thereafter these parameters to a fresh memory array. Figures 4(a) and 4(b) show the current distributions of the initial state and after pulse-induced forming. Statistical analysis in a cumulative distribution function plot in Fig. 5 reveals that 86 % of the devices were formed by the pulse process. A retry-algorithm was then implemented to form the remaining devices. The retry operations have been mostly required on cells with low initial currents. One reason could be that devices with a lower initial current need a higher energy density imparted to the dielectric to be formed. Forming with

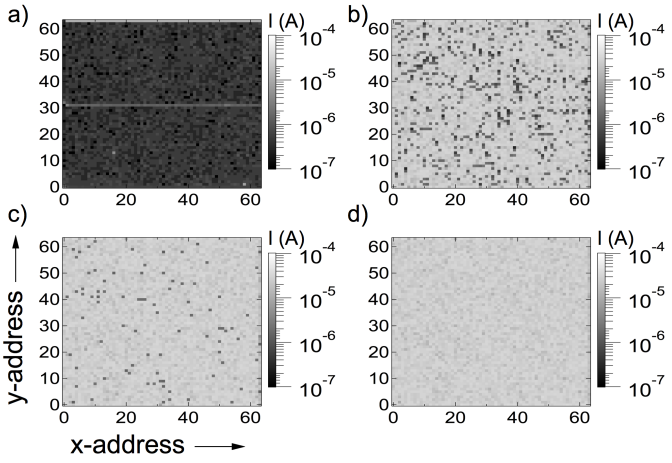


Fig. 4. Current distributions for a 64 $\times$ 64 bit (4 kbit) RRAM array with 1T-1R devices with 600 $\times$ 600 nm^2 MIM area. (a) Initial state. (b) After pulse-induced forming. V_{WL} was set to 1.4 V with V_{BL} = 3.5 V and $t_{BL,\ pulse}$ = 10 μs: total 86 % formed. (c) After applying a retry-algorithm to unformed devices: total 97.6 % formed. (d) After d.c. forming of the devices not formed by the retry step: total 100 % formed. Current reading was performed at V_{WL} = 1.4 V and $V_{BL,\ read}$ = 0.3 V.

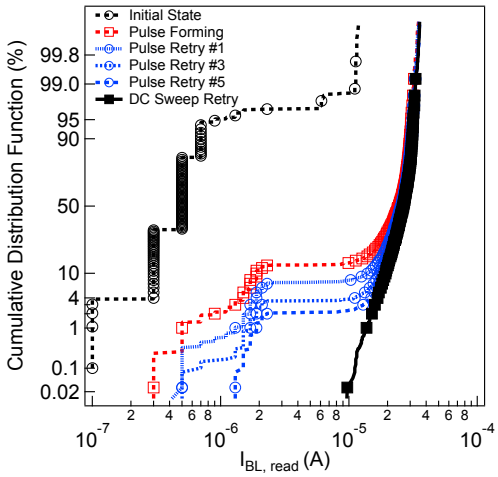


Fig. 5. Statistical current distributions of the initial state, after pulse-induced forming and after application of retry-algorithms. Current reading was performed at V_{WL} = 1.4 V and $V_{BL,\ read}$ = 0.3 V.

the same parameters as before was applied 5 times on BLs with unformed devices. This increased the fraction of formed devices in the array to 97.6 % (Figs. 4(c) and 5). The remaining 2.4 % devices could be formed by a d.c. forming step (Figs. 4(d) and 5). After forming, positive V_{SL} step sweeps with V_{WL} = 2.2 V and V_{BL} = 0 V reset the devices to the high resistance OFF state. Positive V_{BL} step sweeps with V_{WL} = 1.4 V and V_{SL} = 0 V set the devices to the low resistance ON state (Table I). The OFF/ON resistance contrast on repeated switching cycles remains typically between 1.4 to 10.

C. Intra-cell variability in set/reset endurance and after bake

We performed set/reset pulse operations after pulse forming and after pulse-retry forming to evaluate the cycling endurance (Fig. 6). 70 % of the devices formed with the first forming

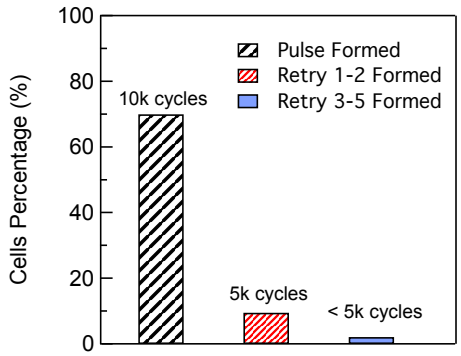


Fig. 6. Set/reset cycling endurance after pulse-induced forming and after pulse-retry forming.

pulse show the highest endurance, whereas almost 16 % of them evidenced resistance switching issues after a possible over-forming process [40].

As the number of forming-retry pulses increases, the resistance switching capability of the conductive filament is strongly impacted: retry-formed cells show lower cycling endurance compared to single-pulse formed cells. The retrieved endurance of 10^4 cycles is significantly lower than what retrieved for similar arrays [33], [41] and this could be attributed to the impact of impurities in the metal-organic AVD precursor, in particular to carbon [36]. To support such a consideration, Fig. 7 shows a XPS depth profile measurement of a 50 nm thick HfO_2 deposited on a silicon substrate. Since the cells embedded into the array are too small for the analysis, XPS profile has been measured on cells with a higher HfO_2 stack, but processed with the same deposition parameters used for the MIM cells in the array. A high presence of carbon and nitrogen atoms can be observed: these impurities are caused by the liquid metal-organic precursor, used for the AVD deposition process. Their presence severely limits the oxide performance and wears the cells in the array faster than any other degradation mechanism.

To evaluate the relationship between forming conditions and endurance, formed cells with a single pulse, after 1, 3, 5 forming-retry pulses and after d.c. step sweep were considered (Tab. I). Figures 8 (a) and 8 (b) show the average and minimum (i.e. considering the worst-case condition) read window calculated during cycling for each cell subset [16]. For all cell subsets both average and minimum read window decrease with increasing number of cycles.

Figure 9 (a) shows the ON state (LRS) intra-cell variability during cycling, which indicates decrease for each cell subset. The highest variability is observed on cells formed after 5 pulse-retry algorithms and after d.c. step sweeps. Similar behavior is observed for the OFF state (HRS) intra-cell variability during cycling in Fig. 9 (b). The reduction of the intra-cell variability during cycling is given by the fact that a consecutive set/reset operation brings all cells toward a uniform wear-out condition of the conducting filament, therefore reducing the fluctuations due to structural modifications of the conduction path in the memory cells [11].

In order to investigate the reason underlying different

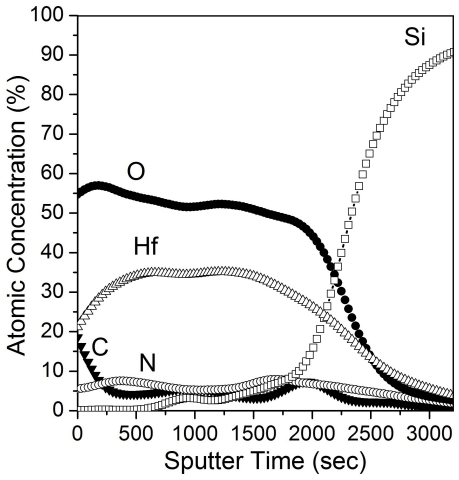


Fig. 7. XPS depth profile measurement of a 50 nm thick HfO_2 RRAM cell.

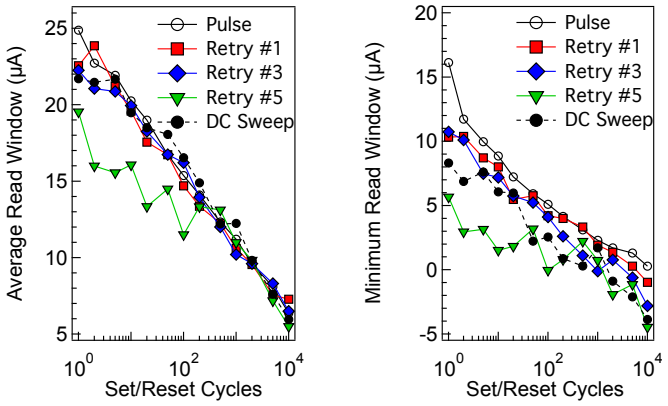


Fig. 8. (a) Average and (b) minimum read window after a single pulse, after 1, 3, 5 forming-retry pulses and after d.c. step sweep.

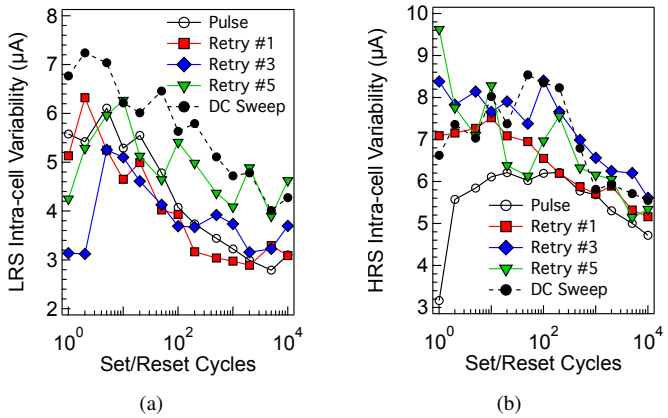
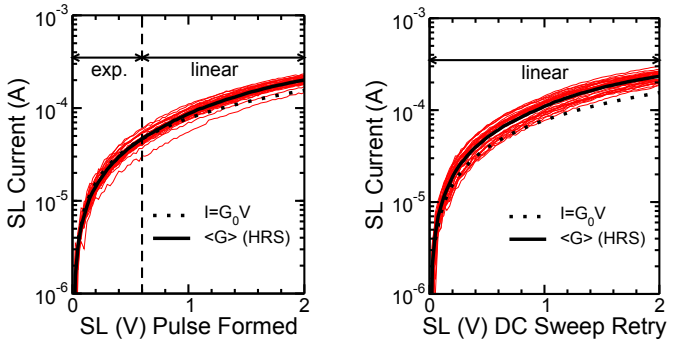


Fig. 9. Intra-cell variability during 10^4 pulse set/reset cycling for (a) LRS and (b) HRS.



(a) (b)

Fig. 10. HRS I-V curves measured on cycled devices after Reset on cells formed with a single pulse (a) and with DC retry operation (b).

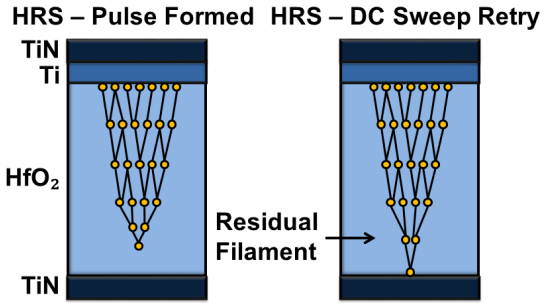


Fig. 11. Schematic showing the conductive filament shape after reset (HRS) for Pulse and DC Retry formed cells.

degradation speed for different forming retry times, I-V measurements of the Reset operation have been performed at endurance cycle 10^4. Fig. 10 shows HRS I-V curves of the cells formed with a single pulse (a) or with DC sweep retry operations (b). The black dashed line shows the limit $I = G_0V$ with $G_0 = 2e^2/h$ equal to the quantum conductance unit corresponding to the creation of a single mode nanowire according to Quantum Contact Point (QPC) model [20], where e is the electron charge and h the Planck's constant. The average $< G >$ curves measured after Reset is shown for sake of comparison. Within this framework, in case of $I > G_0V$ the presence of a residual conductive filament has to be taken into account. Cells formed with a single pulse show lower average conductance values after Reset, even after cycling. Moreover, on single pulse formed cells an exponential ($V_{SL} < 0.6V$) plus linear ($V_{SL} > 0.6V$) current behavior can be observed since $< G >$ is very close to $I = G_0V$ limit, whereas only linear behavior is observed on $< G >$ of DC sweep retry formed cells. This indicates that for single pulse formed cells, the filament geometry after cycling in reset condition still evidences a potential barrier giving rise to direct tunneling transport through a material barrier or through a residual confinement barrier (QPC) [30] (i.e., the exponential part of the curve), whereas for DC sweep retry formed cells only the ohmic component is present due to worn-out filament (see Fig. 11). Fig. 12 shows the cumulative distribution of conductance values measured after Reset operation of cells formed at different retry steps: cells formed with a higher number of retry operations show higher conductance values and intra-

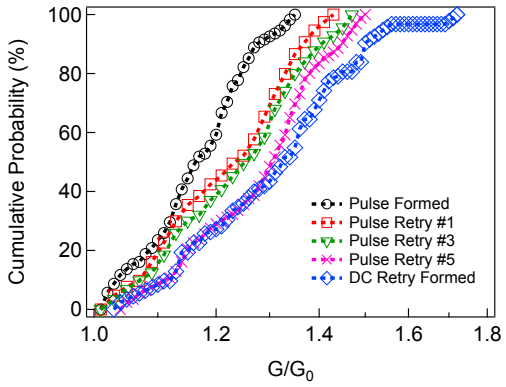
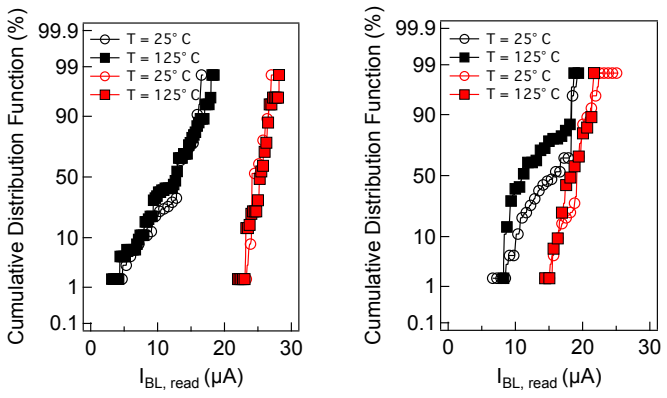


Fig. 12. Cumulative distribution of conductance values measured after Reset on cycled cells.

cell variability. More retry steps allow the cells to reach a more stable state resulting in higher conductance values yet displaying lower switching capabilities. More energy is indeed required in these cells in order to create the conductive filament compared to single pulse formed cells, hence it can be expected that even during cycling a higher set/reset energy was required to create/disrupt the filament on such cells. Due to such lack of energy, a higher intra-cell variability is observed since set/reset operations were not correctly performed on all retry-formed cells.

Figure 13 shows the cumulative distribution function plots for the first (a) and for the 10^4 (b) cycle for pulsed set/reset operations. A 24-hour temperature bake at 125 °C has been applied before and after set/reset cycling on different arrays. The LRS and HRS average currents do not show any relevant variation after bake for both fresh and cycled devices (Tab. II).



(a) (b)

Fig. 13. Statistical current distributions of the temperature bake at cycle (a) 1 and after (b) 10^4 set/reset cycles for the LRS state (red curves) and for the HRS state (black curves) obtained with the following set/reset pulse conditions: $V_{BL/SL}$ = 3 V and $t_{BL,\,pulse}$ = 10 μs (Tab. I).

IV. Conclusion

This paper has presented results on the inter-cell variability of the initial state and the impact of d.c. and pulse forming on inter-cell as well as on intra-cell variability in 4 kbit memory arrays. 100 % of devices in a memory array must be formed

TABLE II
HRS/LRS STATISTICS BEFORE AND AFTER A 24 HOURS TEMPERATURE BAKE AT 125 °C.

	Cycle 1		Cycle 10^4	
	μ (μA)	σ (μA)	μ (μA)	σ (μA)
HRS (25 °C)	11.9	3.7	13.1	3.0
HRS (125 °C)	11.8	3.7	12.1	4.1
LRS (25 °C)	25.2	1.1	18.5	2.7
LRS (125 °C)	25.3	1.3	18.5	1.8

to guarantee a product maturity level for RRAM, however, we observe that on particular arrays only 78 % are d.c. formed. The insights suggest a combination of the extrinsic process-induced variability of the initial state and intrinsic variability after forming as origin. Pulse-induced forming was achieved by choosing 10 μs pulses as well as by V_{BL} = 3.5 V and V_{WL} = 1.4 V. These parameters were applied to the memory array. Using a retry algorithm, we achieve 100 % of pulse-formed devices. However, the endurance of retry-formed devices decreased faster compared to pulse-formed devices with a single pulse. One possible physical explanation for the endurance degradation could be impurities in the metal-organic AVD precursor. The fitting of the I-V curves after different pulse forming steps by using the QPC model offers a route to the understanding of the degradation process within a physical framework.

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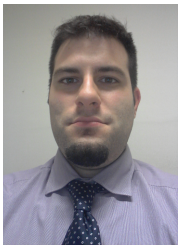
Alessandro Grossi received the M.Sc. degree in electronic and telecommunications engineering from the University of Ferrara, Ferrara, Italy, in 2013. He is currently pursuing the Ph.D. degree in Engineering Science within the Department of Engineering, University of Ferrara. He is currently working on the electrical characterization and modeling of emerging non-volatile memories.

Damian Walczyk (S'06–M'10) received a Dipl.-Ing. (FH) degree in microsystems engineering from the University of Applied Sciences in Münster, Münster, Germany, in 2009, and the M.Sc. degree in electrical and computer engineering from the University of Hagen, Hagen, Germany, in 2015. He joined IHP, Frankfurt (Oder), Germany, in 2010, and since then, he has been working on the electrical characterization of HfO_2-based RRAM devices.

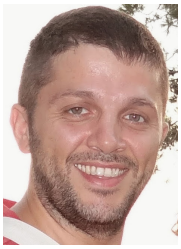


Cristian Zambelli (S'08–M'13) received the M.Sc. and Ph.D. (Hons.) degrees in electronic engineering from the University of Ferrara, Ferrara, Italy, in 2008 and 2012, respectively. He has held an Assistant Professor position with the Department of Engineering, University of Ferrara, since 2015. His current research interests include the characterization, physics, and modeling of nonvolatile memories reliability.

Enrique Miranda (SM'10) received the Ph.D. degree in electronics enginnering with the Universitat Autónoma de Barcelona (UAB), Spain, in 1999 and the Ph.D. degree in physics with the Universidad de Buenos Aires, Argentina, in 2001. Since 2006, he has been Professor with the Escola d'Enginyeria, UAB. His research interests are conduction mechanisms in dielectric films, oxide reliability, memristive and resistive switching devices.

Piero Olivo received the Ph.D. degree in electronic engineering from the University of Bologna, Bologna, Italy, in 1987. He has been a Full Professor of Electronics with the University of Ferrara, Ferrara, Italy, since 1994. His current research interests include the theoretical and experimental aspects of microelectronics, with an emphasis on physics, reliability, and characterization of electron devices and nonvolatile memories.

Valeriy Stikanov graduated from Kiev Polytechnic Institute, Faculty of Electronics, Department of Microelectronics, Kiev, Ukraine, in 1971. In 1987 he received the Ph.D. degree in microelectronic engineering. Since 1996 he is Professor of the System Analysis Department at the Kiev Polytechnic Institute. His scientific activity concerns the writing, erasing, degradation and storage of charge in non-volatile memory devices.



Alessandro Feriani graduated in Electronic Engineering from Perugia University, Perugia, Italy, in 2002. Since 2005, he is working for NplusT Semiconductor Application Center, Perugia, Italy, and he is responsible for application, memory tester and software engineer duties.

Jordi Suñé graduated in Physics in 1986 and received a Ph.D. degree in Electronics in 1989 both at the Universitat Autònoma de Barcelona (UAB), Bellaterra, Spain. He is Fellow of the IEEE for contributions to the understanding of gate oxide failure and reliability methodology. He has (co-)authored more than 150 papers in international journals and relevant conferences. His main fields of interest are gate oxide physics and reliability, resistive switching devices and oxide-based electronics.

Gunter Schoof received his Diploma degree in information technology from the Technische Universität Chemnitz, Germany, in 1983. Since 2003, he is working in the System Design Department at IHP, Frankfurt (Oder), Germany. He is responsible for the implementation and test of new IP components in a digital design library and investigates new methods and concepts of digital ASIC designs using fault-tolerant design techniques.

Rolf Kraemer received his Diploma degree and a Ph.D. degree from RWTH Aachen in Electrical Engineering and Computer Science in 1979 and 1985. He joined the Philips Research Laboratories in 1985 where he worked on distributed operating systems and wireless high speed communication in Hamburg and Aachen until 1998. In 1998, he became Professor at the Technical University of Cottbus with the joined appointment of the Department Head in System Design at IHP, Frankfurt (Oder), Germany.

Bernd Tillack received a Ph.D. degree from Halle-Merseburg University, Merseburg, Germany, in 1980. His research interests include SiGe BiCMOS technology development following the "More than Moore" strategy for embedded system applications. He is also currently with the Berlin Institute of Technology (TU Berlin), Berlin, Germany, as a Professor for Si-based high-frequency technologies.

Alexander Fox received a Diploma degree in electrical engineering from the RWTH Technical University Aachen, Germany, in 1999, and a Ph.D. degree from the Christian-Albrechts-Universität Kiel, Germany, in 2006. In 2000, he joined IHP in Frankfurt (Oder), Germany, where he has been working on integration issues of a 0.25μm BiCMOS technology, Embedded Flash memory module into a SiGe:C BiCMOS baseline technology, and on SiGe bipolar transistors.

Thomas Schroeder received a diploma in Chemistry in 1996 and a diploma in Physics in 1998 from the University of Tübingen. He passed his Ph.D. research at the Fritz-Haber Institute in Berlin and joined IHP in 2004. Prof. Schroeder is the Department Head of IHP's Materials Research Department and he is Professor in Physics at the TU Brandenburg-Senftenberg in Cottbus, Germany. He has authored and co-authored about 160 papers in peer-reviewed journals and he holds about 15 patents in Si microelectronics.

Christian Wenger received a Diploma degree in physics from the University of Konstanz, in 1995 and a Ph.D. degree from the Technical University of Dresden, in 2000. Since 2002, he has been with IHP where he is working in the field of BEOL functional devices. In 2009, he received a post-doctoral degree at TU Dresden. He has authored and co-authored more than 100 papers and holds 6 patents.

Christian Walczyk received a M.Sc. degree in Electrical Engineering from the University of Siegen, Germany, in 2007. Since 2007, he is with with the Materials Research Department at IHP, Frankfurt (Oder), Germany. He finished his Dr.-Ing. degree in Electrical Engineering at Technische Universität Berlin, Germany, in 2011. He has (co)authored 30 publications in peer-reviewed journals.