An Automated Test Equipment for Characterization of emerging MRAM and RRAM arrays

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An Automated Test Equipment for Characterization of emerging MRAM and RRAM arrays

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Abstract—In this paper it is presented a test equipment for the characterization of two different emerging memory technologies like the Thermally Assisted Switching-Magnetic Random Access Memory (TAS-MRAM) and the Resistive Random Access Memory (RRAM). The instrument is developed to allow a fast characterization of test array structures. The hardware architecture is based on a PCI local bus interface of a x86-PC that communicates with the units of the system like arbitrary waveform generators and programmable measurement units. A user-friendly software interface has been implemented to allow large flexibility in changing the test parameters and a fast analysis of the test results. The instrument performance has been evaluated performing the typical non-volatile memory tests such as endurance and disturbs characterizations.

Index Terms—Automated test equipment, non-volatile memory, reliability, thermally assisted switching, MRAM, RRAM

I. INTRODUCTION

The development and the testing of non-volatile memories (NVM) requires extensive characterizations that only a dedicated Automated Test Equipment (ATE) is able to handle. Different features might be required depending on the maturity level of the technology being characterized. Indeed, for a well-established NVM like the Flash technology, where the integration density is the highest, the most desired capability of a test environment is to run standard test algorithms in a highly parallel yet efficient way [1]. On the contrary, for an emerging technology where the physical mechanisms ruling the storage have to be explored, and the investigations are carried on test array structures that are commonly integrated without any internal circuitry (e.g., I/O interfaces, charge pumps, sense amplifiers, etc.) except what is used for cell addressing, a maximum flexibility is sought in terms of signals and timings features applied on the NVM [2], [3].

Among the emerging technologies that are under consideration for a possible replacement of the standard Flash [4] memories in embedded environments, the Thermally Assisted Switching - Magnetic Random Access Memory (TAS-MRAM)

[5]–[7] and Resistive Random Access Memory (RRAM) [8]–[10] represent two good candidates. In the former technology the information storage mechanism is based on the magnetization switch of a magnetic material controlled by applying a current, that generates a magnetic field either parallel or antiparallel to a fixed reference layer thus showing a defined resistance [11], [12]. In the latter technology the conductance of a Metal-Insulator-Metal (MIM) stack can be electrically modified creating or disrupting a conductive filament within the stack through Set and Reset operations, respectively. The presence or absence of such filament translates into a resistance variation of the MIM cell that defines the memory cell state. Both technologies are already in a phase that calls for their evaluation at an integrated array level.

In this paper we present an ATE dedicated to the characterization of TAS-MRAM and RRAM arrays which takes into account the specific requirements of both technologies, while aiming at achieving the performance of a production-line tester. The proposed ATE allows performing the typical tests that are demonstrated by commercial platforms specifically tailored for MRAM and RRAM technologies characterization such as the one in [13]–[16]: endurance testing, hysteresis (R-V curves in TAS-MRAM), I-V curves in RRAM, read disturb, breakdown voltage, switching voltages with respect to pulse widths, switching probability distribution with respect to applied voltage, low/high state resistance distribution and error rate testing. These characterizations are achieved by the proposed ATE without sacrificing the accuracy and ease of operation of the system. The instrument architecture has been developed with a twofold purpose: *i)* provide an environment for highly parallel testing in order to speed-up the long-term reliability characterization; *ii)* provide all the flexibility required in terms of operation modes that are requested by the exploration of an emerging technology. A software interface has been implemented using a high-level description language tightly coupled with a low-level driver. This solution allows implementing specific features to statistically identify failures and abnormal technology behaviors.

The advantages of the proposed ATE with respect to the state-of-the-art testers [13], [17]–[19] are modularity, flexibility and portability. The ATE can be easily modified adding/replacing waveform generators to satisfy specific requests for the memory technology without requiring any successive calibrations. No support of external instruments is required, limiting the sources of measurement errors. Moreover, the ATE features a higher portability compared to actual state-of-the-art testers (dimensions equivalent to a PC). The
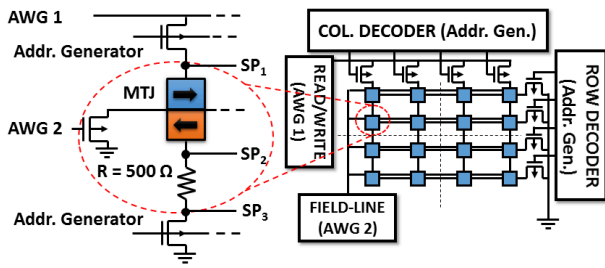
Fig. 1. TAS-MRAM memory cell (left) and array architecture (right) exploited in this paper.
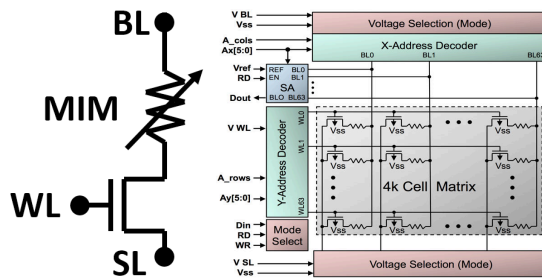

Fig. 2. RRAM memory cell (left) and array architecture (right) exploited in this paper.

tester can accommodate both packaged devices and wafers by using a specific test-head or probe card. The ATE software is fully accessible and reconfigurable considering the memory specifications. Finally, the Labview control software easily allows the development of complex test-flows with feedback loops (i.e., decide run-time which operation to perform as a function of the previous test results) in a user-friendly graphical interface. The performance and effectiveness of the proposed ATE has been preliminary demonstrated in [20], [21] and here is fully validated on different MRAM and RRAM test arrays.

II. ATE REQUIREMENTS

The paved capabilities of the TAS-MRAM in terms of performance and reliability pose however several challenges in the development of an ATE suitable for their characterization. The first issue is related to the current supply required by the cells in order to reliably switch between different logical states [22]. Each memory cell needs two current sources: one driving the heating phase (i.e., thermal assistance), and one driving the effective magnetic field switch. Their current value strictly depend on the parallelism to be achieved. Therefore, waveform generators with a high current output stage and a high slew rate are required to meet the fast operation feature of the TAS-MRAM technology, that is in the range of 200 ns $\div$ 20 μs.

The second issue is due to the extreme long-term reliability offered by the technology [23]–[25]. TAS-MRAM cells exhibit an endurance capability up to several millions switching cycles (i.e., orders of magnitude higher than a traditional flash technology), therefore to monitor potential reliability threats coming either from the manufacturing process or from the chosen write algorithm it is required to repeatedly apply

sequences of read/write operations with a perfect synchronization of the tasks to perform during the test. Moreover, it must be guaranteed a non-blocking time of the operations that extract the characterization data from the memory (i.e., read operation) both to avoid testing limitations and to allow the user to interact with the ATE during test (e.g., to extract statistical data).

The capabilities of RRAM memory cells in terms of current supply and fast operation features are not as strict as TAS-MRAM, therefore an ATE with flexibility and performance able to characterize MRAM technology is also suitable for testing RRAM arrays.

III. TEST CHIP SPECIFICATIONS

A. MRAM

The MRAM test chips tested by the designed ATE are 1 kbits TAS-MRAM arrays where only cells and decoders are present, organized in 4 banks with 8 wordlines and 32 bitlines each. The cells' architecture is a 1T-1J, integrated into a CMOS process from Crocus Technology, that is selected via a 10-bit multiplexer (see Fig. 1) [26]. To prove the capabilities of the proposed ATE to handle different TAS-MRAM technologies two different generations of the arrays have been characterized, hereafter indicated as Sample A and Sample B. The main difference in the two technologies is the stack of materials integrated in the cell structure, leading to different hysteresis characteristics in the magnetic materials and read/write speed of the array. The specifications of both test array architectures are the following:

- each memory cell in the array requires two signals during a write operation applied on dedicated pads. The first signal (AWG 1 in Fig. 1) drives the heating phase of the write procedure and ranges from 0 V up to 2 V, whereas the second signal (AWG 2 in Fig. 1) drives the effective magnetization switch by applying either a positive or a negative voltage ranging from 0 V up to ± 5 V.
- During the read operation, after applying a fixed voltage ranging from 0 V up to 0.5 V on AWG 1, three different voltages must be sensed on dedicated measurement pads that represent three sensing positions on the memory cell: the voltage on top of the magnetic element (SP_1), the voltage below it (SP_2), and voltage between the select transistor and a fixed 500 Ω resistor (SP_3). The combination of the voltages allows extracting the resistance value of the memory cell and hence its logical state.

The timings are usually 200 ns $\div$ 20 μs for the writing operations and 20 μs for the read operation. For the former it is important to guarantee that the signal driving the switching is synchronized with the heating voltage and that it ends 100 ns $\div$ 10 μs after the end of the heating signal.

B. RRAM

The RRAM test chips are 4 kbits arrays composed by a memory cells matrix, a bitline/sourceline (BL/SL) and wordline (WL) decoder and an operation control circuitry (see Fig. 2) [14]. The 1T-1R memory cells are constituted

by a select NMOS transistor manufactured with a 0.25 μm BiCMOS technology whose drain is in series to the MIM stack. The variable MIM resistor is composed by 150 nm TiN top and bottom electrode layers, a 7 nm Ti layer, and a 8 nm HfO_2 layer. To activate such a switching behavior, some technologies require a preliminary Forming operation in order to create the conductive path for the first time [27], [28]. The specifications of such architecture are the following:

- Forming, Set and Reset operations require the application of two signals on dedicated pads. The first signal (AWG 1) is applied on the WL of the selected 1T-1R cell to turn on the NMOS transistor and to define the current compliance, whereas the second signal (AWG 2) is applied either on BL (during Forming and Set) or SL (during Reset) of the selected cell in order to create or break the conductive filament, respectively. The WL signal ranges from 1.5 V up to 2.8 V, whereas BL and SL signals range from 0.2 V up to 3.5 V.
- In read operation, while applying a fixed voltage pulse of 1.5 V on WL (AWG 1) and 0.2 V on BL (AWG 2), the current flowing through the BL must be sensed in order to extract the resistance value of the memory cell and hence its logical state.

The operations can be performed by single pulses or sequence of pulses with lengths between 1 μs $\div$ 100 μs for Forming, Set and Reset and 10 μs for the read operation [29]. It is important to guarantee the synchronization between WL and BL/SL signals in all operations in order to correctly switch the devices. Moreover, during Read operation the voltage sensing must be correctly synchronized with WL and BL pulses.

IV. ATE HARDWARE ARCHITECTURE

The instrument architecture is depicted in Fig. 3. The ATE is composed by: a PCI controller, a RISC μP with a sequencer, pin drivers for the power supply and the address/vector generator unit, two Arbitrary Waveform Generators (AWGs), and a multi-channel Programmable Measurement Unit (PMU).

A. PCI Controller

The ATE is controlled by a standard x86-PC through the PCI local bus installed on the motherboard. The S5933 PCI controller and the control logic of the digital instrument section
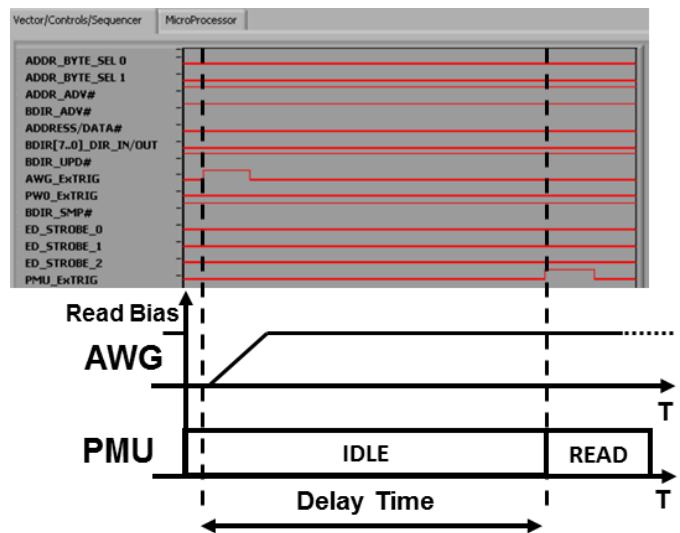

Fig. 4. Control panel of the RISC μP and of the digital sequencer. In this plot the AWG and PMU triggers are set for a read operation by the sequencer.

are mounted on a board to be plugged into the computer. The choice of the PCI local bus as an interface for the ATE allows considering the Memory Under Test (MUT) as an extension of the x86-PC memory, thus allowing direct addressing and reading.

B. Pin drivers

To correctly provide the power supply to the MUT connected to the ATE, and to provide the voltage to the address and the vector generator units (i.e., the units responsible for creating the signals that select the cells in the arrays) a pin drivers unit has been implemented. This component provides the matching between the PCI controller and the MUT bias requirements.

C. RISC μP and sequencer

The RISC processor mounted inside the ATE allows sharing the tasks with the x86-PC in order to optimize the system resources without loosing programming flexibility. The ATE core is implemented on a high performance FPGA. The digital sequencer unit coupled with the processor drives the digital
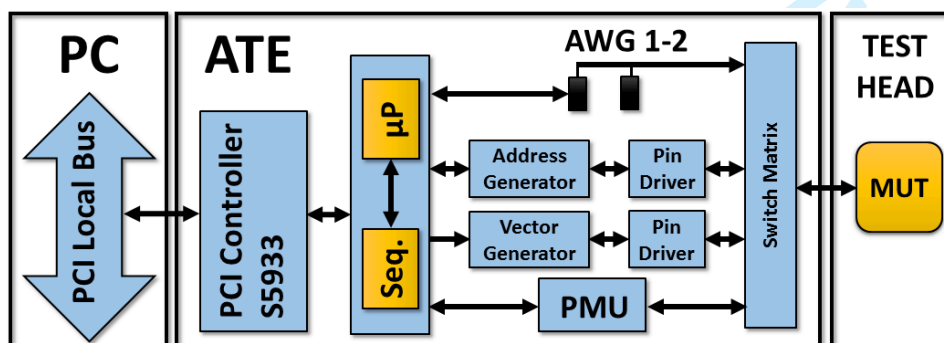

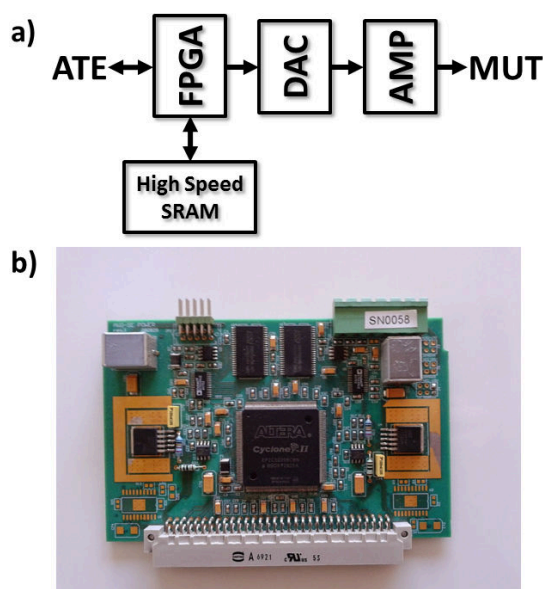Fig. 3. ATE architecture block diagram.

Fig. 5. Arbitrary waveform generator block diagram (a) and picture (b).
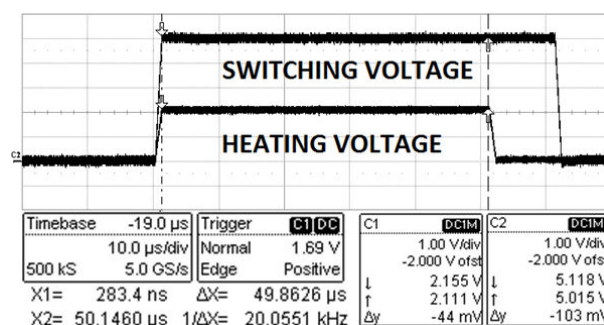

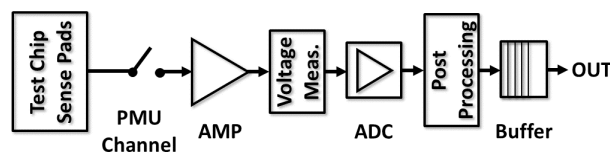Fig. 6. Measured voltage waveforms generated by the AWG units during a write operation.


Fig. 7. Block diagram of a single PMU channel.

Fig. 8. Resistance reading: test setup (left) and sensing pad resistance reading (right).

control signals of the peripherals connected to the ATE (i.e., it provides the trigger for the AWGs and the PMU). The entire unit works at 400 MHz allowing a 2.5 ns time resolution. Fig. 4 shows μP and sequencer control panel, showing the control signals applied during a read operation to trigger the voltage waveform generation by the AWGs with the timings required by the test chip specifications immediately followed by the PMU measurement.

D. AWG

The AWG units are the hardware components that drive the signals used during both write and read operations. Their design must fulfill all the tight requirements of the two technologies considered in this work, namely the high current output and the precision in generating short voltage pulses.

The block diagram of an AWG unit and its realization is shown in Fig. 5. The 14-bits digital samples of the voltage waveform to be generated, that can be graphically edited by the user with the ATE software interface, are stored in a high-speed static RAM. During measurement, on a trigger signal edge generated by the digital sequencer, the memory content is read in sequence and waveform samples are converted by a high-speed digital-to-analog converter (DAC) that operates at 100 MHz. A high-speed current feedback output buffer featuring a 1000V/μs slew rate converts the DAC output current to voltage. The maximum current that can be drawn by an AWG unit is up to 500 mA. The AWG clock speed defines the ATE limitations in waveform generation, consisting of a minimum pulse voltage length of 10 ns featuring a minimum rise/fall time of 9 ns. Its overall resolution is down to 1 mV. An example of voltage waveforms generated during the write operation on a TAS-MRAM array is shown in Fig. 6.

E. Multi-channel PMU

The PMU unit is used to sense the voltage on the TAS-MRAM sense pads and RRAM BL pin. The architecture of
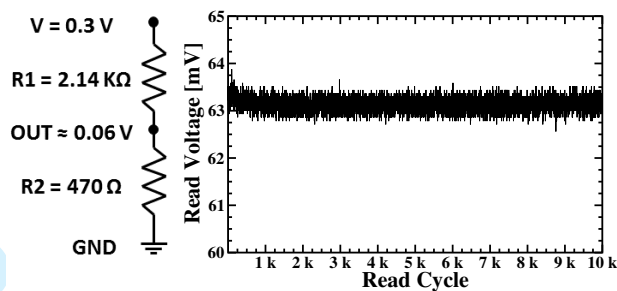
a single PMU channel is depicted in Fig. 7. Eight parallel independent channels are integrated in the ATE, each one featuring a signal conditioning amplifier with a high signal-to-noise ratio (AMP), a fast voltage measurement unit, a 12-bits ADC triggered directly by the digital sequencer, and a post-processing buffer unit to temporary store the measurement data to be evaluated by the ATE software. The operating frequency of the PMU is 70 MHz (14.3 ns resolution time) featuring a current measurement error less than 1 %. The ATE features a minimum read time of 40 ns, limited by both AWG triggering and PMU clock speed. The gain and the offset adjustments of the PMU are stored in an EEPROM memory that is read at system start-up.

10000 consecutive read operations on three out of eight PMU channels have been performed using a test setup that mimic the resistance configuration of a TAS-MRAM memory cell. A voltage divider constituted by the resistances R1 = 2.14 $k\Omega$ and R2 = 470 Ω (see Fig. 8a) is connected to the sense pads. The results obtained show an average displacement from the theoretical value equal to 3 mV, and a measurement uncertainty of 137 μV) as shown in Fig. 8 (b).
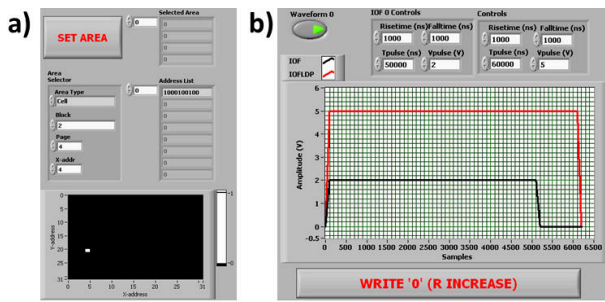
Fig. 9. GUI panel of the ATE for test population selection (a) and AWG setup for the write operations (b).

V. ATE SOFTWARE INTERFACE

The software interface is hierarchically organized in two different interacting layers: the low-level routines that directly communicate with the ATE hardware components, and the high-level libraries that interacts with the user through a Graphical User Interface (GUI). The low-level routines are written in C language to ensure efficiency both in terms of speed and memory requirements, whereas the high-level libraries have been implemented by using the National Instruments LabVIEW tool. The user can control any instrument operation and modify the ATE hardware parameters accordingly. It is possible to vary the write operation waveforms, the speed of the read operation, and many other parameters by simply acting on the GUI panels provided within the software interface (see an example in Fig. 9).

The GUI also allows selecting the test population within the memory array by implementing an address scrambler that may choose from single cells, array wordlines, banks and full chip. By interacting with the low-level routines the ATE software identifies the degree of parallelization requested by the user and sets the hardware resources accordingly. Moreover, an environment for graphically visualizing the test sequence is provided through LabVIEW, and a post-analysis tool for immediate data characterization after test. An example is given in Fig. 10 where the tool is used to locate the cells of an entire TAS-MRAM array that failed to switch due to a breakdown condition under very high voltage stress. The data are also available after the test execution in different formats readable by the most common data processing tools.

VI. EXPERIMENTAL RESULTS AND ATE PERFORMANCE

The ATE functionality and performance have been characterized through a set of tests applied on different TAS-MRAM and RRAM arrays. In order to show the ATE flexibility, the results obtained both on single cell subsets and full chip characterizations are reported. Typical NVM tests suitable for evaluating memory cells intrinsic reliability were performed on both technologies, such as:

- Hystheresis analysis (TAS-MRAM) and I-V curves (RRAM): they are obtained by measuring the read resistance while varying the voltage applied on the AWG connected to the field line drivers in TAS-MRAM and to the BL/SL in RRAM. These tests are useful to understand
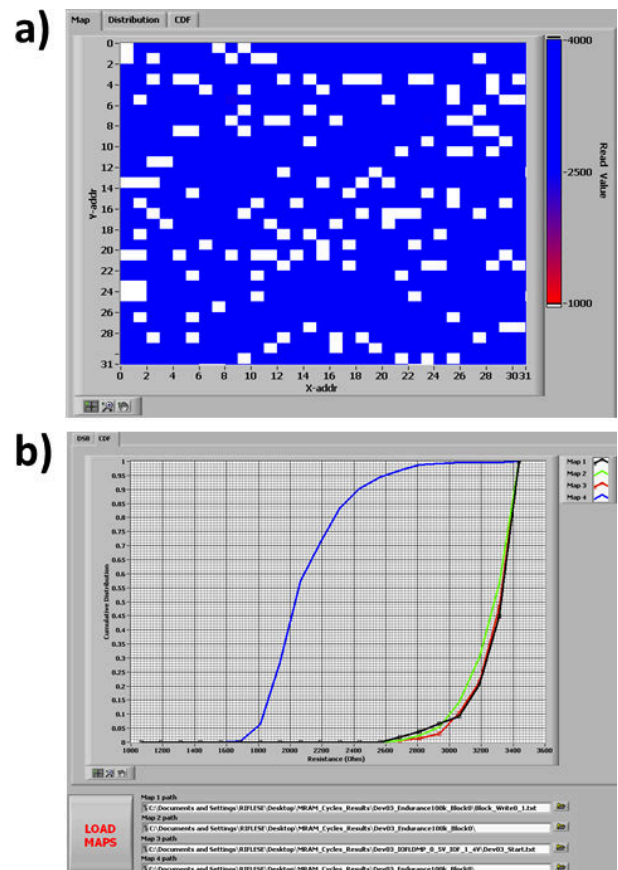

Fig. 10. Resistance map measured in a full TAS-MRAM chip reading operation on the user interface (a) and post-analysis tool used for statistical analysis (b).

possible asymmetries in the writing process in TAS-MRAM and the Set/Reset switching dynamics in RRAM, while providing an estimate of the technology write speed.

- Read disturb test: it consists in consecutive read operations applied on the same set of cells in the array. This test is also useful in understanding whether or not the read operation could be a blocking factor for the ATE performance since the read operation cannot be parallelized.

- Endurance test: it consists in repeated write operations interleaved by a readout operation at fixed cycles. This test combines the evaluation of the ATE resources parallelization capabilities and the read operation constraints.

A. MRAM

Fig. 11 shows the hysteresis characteristic of a single TAS-MRAM cell in both array technologies. A complete analysis performed on one cell in the array by increasing the voltage from 0 V up to 5 V in 0.2 V steps for both write operations can be performed in less than 5 seconds per cell for both TAS-MRAM technologies.

A test of 1M disturb cycles applied on full arrays requires up to 440 hours for Sample A arrays and 77 hours for Sample B arrays which are a reasonable time considering that similar
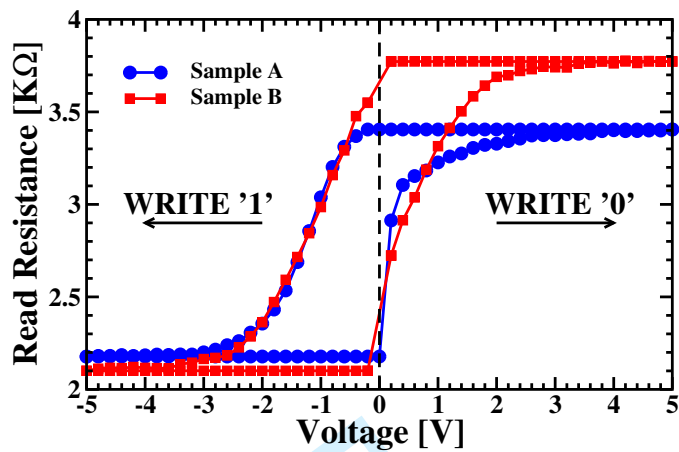
Fig. 11. Hysteresis characteristics of a single cell in Sample A and Sample B TAS-MRAM array.
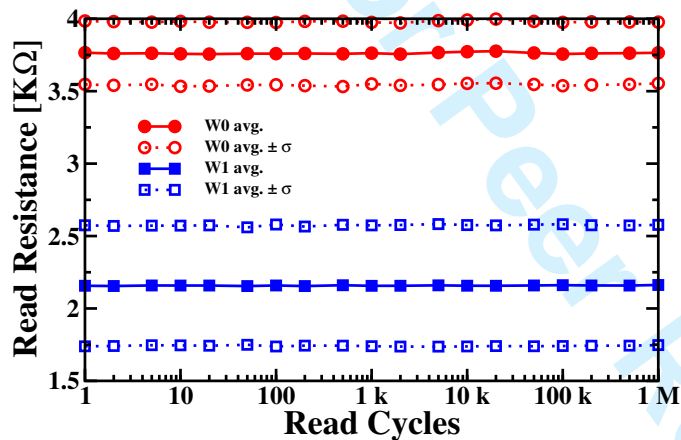

Fig. 12. Average read resistance and standard deviations for both logical states measured during a 1M cycles read disturb test on a full Sample A TAS-MRAM array. Similar results are obtained for Sample B arrays.

tests performed on single cell structures take almost the same time [25]. The results of the test are shown in Fig. 12.

Finally, to further test the efficiency of the tester, a 1M endurance switching cycling has been performed on a full chip. The test lasted 320 hours for Sample A technology and 56 hours for Sample B technology proving once again the goodness of the proposed measurement system. The results of the endurance characterization are shown in Fig. 13, where the average read resistance and standard deviation for both logical states are shown. The cumulative resistance distributions of Sample A (left) and sample B (right) TAS-MRAM array blocks in the different logical states at fixed switching cycles measured during an endurance test are reported in Fig. 14. It is worth to point out that the tester accuracy is not impacted by the TAS-MRAM read/write speed, since there are no measurement artifacts introduced by the ATE in the statistical analysis of the arrays. A resume of the performance feature of the proposed ATE is presented in Table I.

B. RRAM

In order to observe the RRAM cells switching dynamics, Set and Reset I/V characteristics have been measured with a
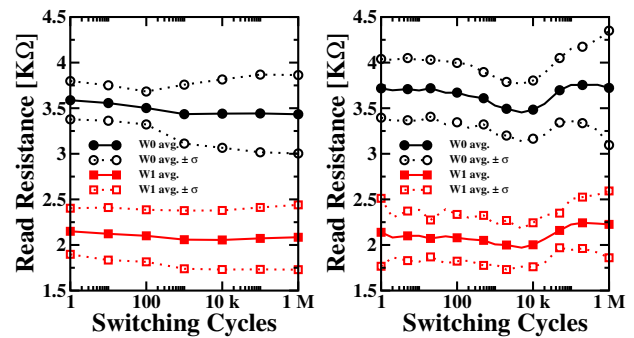

Fig. 13. Average read resistance and standard deviations of Sample A (left) and sample B (right) TAS-MRAM array blocks at fixed switching cycles measured during an endurance test constituted by 1M switching write cycles.
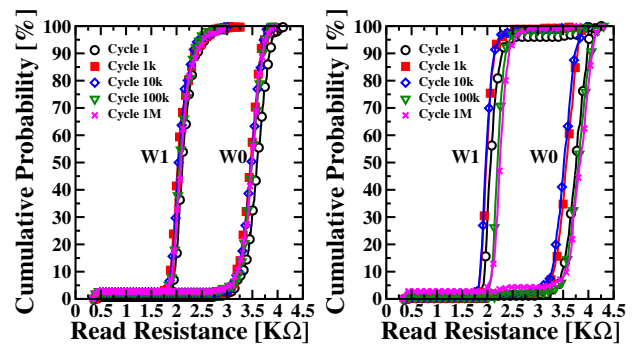

Fig. 14. Cumulative resistance distributions of Sample A (left) and sample B (right) TAS-MRAM array blocks in the different logical states at fixed switching cycles measured during an endurance test constituted by 1M switching write cycles.

DC sweep on 30 memory cells in the array, increasing the BL/SL voltage from 0 to 3.5 V with step voltage of 0.1 V, and a WL voltage of 1.5 V in Set 2.5 V in Reset, respectively (see Fig. 15).

In the considered RRAM cells the read signals has the same polarization of the Set operation (both pulses are applied on the BL), hence the read disturb could only be a problem on cells in HRS state because a very long sequence of read pulses could slowly re-create the conductive filament and change the state of the cells [30]. Thus, read disturb has been evaluated only on cells in HRS state: Fig. 15 shows the average HRS read current and its relative standard deviation measured during 100k read operations.

To evaluate the endurance properties of the cells, 10k Set/Reset cycles have been performed through an incremental program with verify procedure: such method leverages on the application of a sequence of pulses with increasing voltages, each step being followed by a current read operation that monitors the cell resistance [31]. When a cell reaches a predefined read current value after the pulse application, defined as verify target, the procedure is interrupted so that all cells are brought into a comparable electrical condition. In Set operation the BL pulse voltage was increased from 0.2 V to 3.5 V with steps of 0.1 V, $T_{pulse} = 10\mu s$, a WL voltage of 1.5 V and a read-verify target $I_{read} = 20\mu A$. In Reset operation the SL pulse voltage was increased from 0.2 V to 3.5 V with steps of 0.1 V, $T_{pulse} = 10\mu s$, a WL voltage of 2.5 V and a read-verify target

TABLE I
MEASURED ATE PERFORMANCE EVALUATED ON TAS-MRAM FULL CHIP TESTS

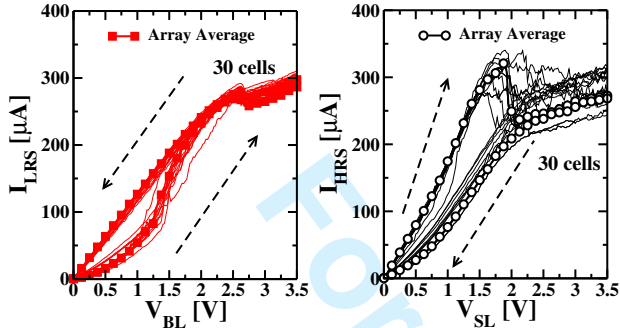| Test	Time [h] Sample A	Time [h] Sample B
Hysteresis analysis	1.27	1.20
Read disturb (1e6 cycles)	440	77
Endurance (1e6 cycles)	320	56

Fig. 15. SET (left) and RESET (right) switching kinetics performed on 30 cells in the RRAM array test structure [29].
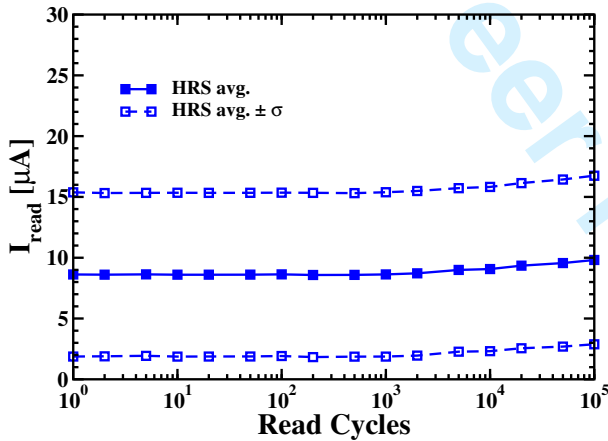

Fig. 16. Average read resistance and standard deviations for HRS state measured during a 100k cycles read disturb test on a full RRAM array.

$I_{read} = 10\mu A$. The average values and standard deviations of the currents read after Reset (HRS) and Set (LRS) operations during the endurance test are shown in Fig. 17. A resume of the performance features of the proposed ATE with RRAM arrays is presented in Table II.

TABLE II
MEASURED ATE PERFORMANCE EVALUATED ON RRAM FULL CHIP TESTS

Test	Time [h]
I-V Curves	0.58
Read disturb (1e5 cycles)	1225
Endurance (1e4 cycles)	6137

VII. ATE BENCHMARKING

Few commercial platforms [13], [17]–[19] have been presented for testing RRAM and MRAM devices, although those solutions are more suitable to test either single cell structures
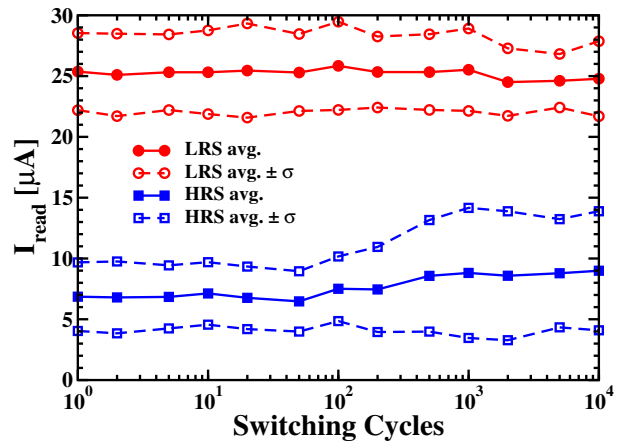

Fig. 17. Average read resistance and standard deviations measured on RRAM array at fixed switching cycles measured during an endurance test constituted by 10k switching cycles.
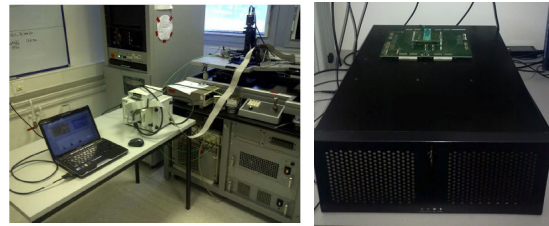

Fig. 18. Test platforms at a glance: the modular setup (left) and the proposed ATE (right).

or small test element groups. Moreover, the provided flexibility is often traded with the efficiency of test time. These test solutions require the interfacing with additional instrumentation and the usage of custom programming language that make difficult the fast evaluation of test patterns. In particular, the proposed ATE is proven to reach the performance of high-end measurement systems such as the one demonstrated in [17] in terms of measurement resolution (i.e., hundreds of μV using a 1.2V full scale), number of parallel measurement channels (i.e., eight parallel measurement channels), and synchronization/triggering capabilities (i.e., delayed measurement triggered by external events). In this section, the developed ATE is benchmarked against a common modular setup that is used in characterization and qualification of TAS-MRAM arrays. Fig. 18 shows the two platforms at a glance.

The benchmark setup is composed by a PXI-based bench controlled by a PC via an ExpressCard plug. The control routines are written in MATLAB language. The PC controls all the cards inside the PXI chassis: the analog output card (NI-PXI 6723) [32] for the heating and switching voltages generation, the analog acquisition card for the sensing (NI-PXI 6220) [33], and the GPIB card for data dispatching. The performance of this system are significantly lower than those offered by the proposed ATE: the analog output card has a sampling rate that limits the pulses generation for the heating and the switching voltages in the μs-range, whereas the analog acquisition card has a timing resolution of 50ns that is four times higher than the performance achieved by the

proposed ATE. Moreover, two points favor the developed ATE against this setup: the compactness of the system and the ease of programming. The former, because no external cables are foreseen in the proposed tester minimizing the risk of disturbs and measurement errors. The latter, because the intuitive GUI and the built-in post-analysis tools allow developing complex test flows in shorter time and with additional features like the run-time modification of the testing conditions during the test execution.

VIII. CONCLUSIONS

In this paper we have presented a dedicated automated test equipment to be used for the characterization of TAS-MRAM and RRAM array structures. Its internal hardware architecture has been developed using a modular approach that favors the integration between state-of-the-art PCI bus technology and cutting edge technology used for the development of high speed/high power arbitrary waveform generators. The instrument software is organized hierarchically so that low-level high-speed routines cohabit with graphical user interfaces that easily allows controlling all the hardware parameters. The performance of the tester has been proven in running both single cell tests and more complex routines, where a high parallelization degree was needed, with a relatively low execution time.

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