Nickel and Nickel-Platinum Silicide for BiCMOS Devices

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The world's fastest SiGe HBT was presented by Heinemann et al. at IEDM 2016, which was achieved among other measures by NiSi application. The BiCMOS integration of such HBTs requires a careful NiSi adjustment with respect to MOSFET leakage currents. The goal of this paper is to find out a NiSi or NiPtSi process, which results in low R_S to increase f_{max} without degradation of MOSFET leakage currents. An f_{max} rise is demonstrated by a reduction of NiSi or NiPtSi R_S to 4 Ω. A further R_S lowering to 1.6 Ω with a corresponding f_{max} increase was achieved by NiSi layers formed by two-step 300/450°C anneals, which generate elevated MOSFET leakage currents. They can be inhibited for NiSi formed by 200/450°C anneals at the expense of elevated R_S. NiPtSi significantly suppresses silicide pipes to the MOSFET channel even for 300/450°C anneals and is a promising choice for upcoming BiCMOS technologies.

Introduction

Recently, the world's fastest SiGe-HBT (hetero bipolar transistor) featuring $f_T/f_{max}/BV_{CE0}$=505 GHz/ 720GHz/ 1.6V and a minimum CML ring oscillator gate delay of 1.34 ps was presented by IHP researchers (1). The speed improvement in comparison with our previous HBT technologies originates from an optimized vertical profile, from lateral device scaling, and a decrease of emitter and base resistance by application of low temperature nickel silicide (NiSi) formation and low temperature back end of line processing.

The low temperature NiSi formation on the one hand reduces the base resistance by a suppressed boron deactivation of the base polysilicon (2), and on the other hand it prevents the degradation of the internal HBT base Ge and B profiles. Additionally, low-ohmic NiSi layers can rise the cutoff frequencies of specific HBT layouts, which will be shown in this paper.

The integration of such HBTs with MOSFETs into BiCMOS technologies comes along with challenges for a simultaneous Ni silicide formation. The silicide contact areas of MOSFETs are placed into the shallow and steep source drain (SD) areas. Therefore, the Ni silicide layers have to be carefully adjusted, to suppress silicide based defects shortening the SD-well pn junctions perpendicularly, towards the conducting channel, or along the SD-STI interface.

The goal of this contribution is to find out from several two-step silicidations of Ni or NiPt layers a suitable process for a BiCMOS technology which results in low silicide

sheet resistance for high cutoff frequencies of bipolar and MOS transistors without degradation of leakage currents.

In this paper, the silicide phase transitions of NiSi and NiPtSi are compared. The first of two Ni and NiPt silicide formation phases is investigated to control the silicide properties with respect to defect formation which can degrade MOSFETs by enhanced leakage currents. After a presentation of the silicide R_S process window of the considered silicide splits, the impact of silicide sheet resistance on f_{max} of two HBT generations with an asymmetric base contact is studied. Finally, the diode leakage currents of NiSi and NiPtSi splits are investigated to identify the best NiSi or NiPtSi scheme for the bipolar and MOSFET devices.

In result, an f_{max} increase is demonstrated by a reduction of NiSi or NiPtSi R_S to 4 Ω. A further R_S lowering with a corresponding f_{max} increase was achieved by NiSi layers formed by a two-step 300/450° anneals, which generates elevated MOSFET leakage currents. They can be suppressed for NiSi formed by 200/450°C or 230/450° anneals at the expense of elevated R_S. However, NiPtSi layers significantly prevent silicide pipes to the MOSFET channel even at 300/450°C anneals.

Nickel and Nickel-Platinum Silicide Phase Transitions

For a comparison of the Ni and NiPt silicide phase formations and for evaluation of the aimed NiSi and NiPtSi phases, a temperature dependent in situ XRD measurement is suitable. A description of the applied in situ XRD specular measurement in Bragg-Brentano geometry is given in (3).

In Fig.1, a transition from Ni to Ni_2Si, and NiSi is clearly visible, only the $NiSi_2$ intensity is not noticeable. The (111)-oriented Ni layer exists in a range from 100°C to 250°C. The Ni to Ni_2Si transformation starts at about 200°C and Ni_2Si remains until 320°C. The aimed NiSi phase forms at 300°C and extends over a large temperature range up to 750°C.

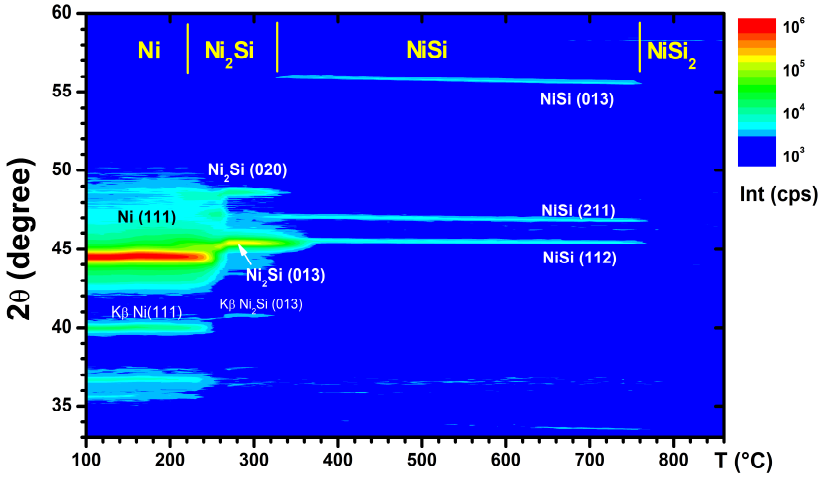

Fig.1: 2Θ–temperature plot of a 40nm Ni layer on Si created by in situ ω-2Θ scans measured in 10K intervalls.

The NiPt sample in Fig. 2 shows a similar silicide phase tranistion from Ni to N_2Si, and NiSi as the Ni sample.

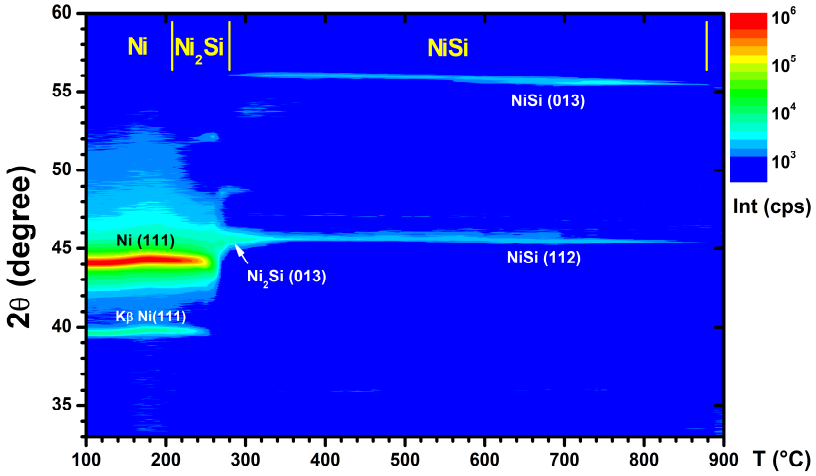

Fig.2: 2Θ–temperature plot of a 40nm NiPt(Pt:5%) layer on Si(100) created by in situ ω-2Θ scans measured in 10K intervalls.

However, the NiSi phase has a larger temperature process window (280°C to 880°C) compared to Fig.1, at the expence of the adjacent Ni_2Si and $NiSi_2$ phases. This increased NiSi stability is explained by Christensen et al. (4) by the fact, that NiSi has the best Pt solubility compared to all other Ni silicde phases. In result, Pt segregates at the interfaces and blocks for instance the $NiSi_2$ formation.

Nickel and Nickel-Platinum Silicide Formations

Two-step NiSi and NiPtSi Formations

In a two-step silicidation nickel is transformed by a low temperature anneal into the metal rich Ni_2Si phase. After a wet etch of residual Ni and TiN, the Ni_2Si is transformed into the desired NiSi phase by a sinter anneal at an elevated temperature. This scheme allows a good control of the NiSi layer properties, such as texture and the suppression of defects.

In this paper, temperature variations of the first anneal as well as Ni(Pt) depositions at elevated temperature are performed to investigate their influence on the formation of silicide defects such as pipes and spikes of pn junctions, which can enhance MOSFET leakage currents.

Fig. 3 gives an overview of the investigated Ni and NiPt silicidation schemes, which are applied on patterned BiCMOS wafers or on bare Si wafers. After the native oxide removal by HF dip and an in situ Ar sputter clean, the Ni is sputtered and covered by a TiN layer within a conventional metallization cluster tool by Applied Materials. The NiPt layers with a Pt content of 5% were deposited in a similar cluster tool in ann Applied Materials laboratory.

The silicidation starts with the Ni rich Ni_2Si phase formation by the first anneal or during the Ni(Pt) deposition at temperatures between 300°C and 400°C. A description of the Ni sputtering at elevated temperatures and its effect on the Ni silicide and Ni germanide texture is given in (5).The first anneal is executed at temperatures of 200°C or 230°C in a furnace under N_2 atmosphere, and at 250°C or 300°C in a low pressure chamber at 2 Torr. After a piranha wet etch of the Ni layers or an aqua regia etch for NiPt layers the wafers are sinter annealed in a conventional RTP system at 450°C for 30s in N_2 atmosphere.

Step	Description																			
Oxide Etch	HF dip + insitu Ar-Preclean																			
Ni(Pt)-Deposit	thickness (nm)	Ni:40									Ni:20		Ni:40	NiPt: 40 and 20						
	T	RT:27°C											300°	RT:27°C			300°	350°	400°	
1.Anneal	T, t	200°1hour	200°2hours	200°5hours	230°36m	230°70m	300°30s	300°90s	300°600s	300°900s	300°15s	300°90s	300°300s	Ni.Hot dep. NO 1.Ann	200°5hours	230°36min	300°90s	NiPt.Hot dep. NO 1.Anneal		
	process	furnace anneal					low pressure								furn.		lp			
	Ni consumption	PC					PC	FC			PC	FC			PC		FC			
Wet etch		Piranha													Aqua Regia					
2.Anneal	T, t	RTP: 450°C, 30s																		

Fig.3: Overview of investigated NiSi & NiPtSi formations including variations of the Ni(Pt) deposition temperature, the temperature and time of the first anneal with an indication of partial or full Ni consumption (PC, FC).

First Stage of Ni and NiPt silicidation

TEM images of Ni and NiPt silicides after the first anneals at 200°C for 5 hours and at 300°C for 90 seconds are presented in Fig. 4 to compare the first silicidation stages. The Ni_2Si-Ni-TiN layer stack in Fig. 4a indicates a partial Ni transformation into the Ni rich Ni_2Si phase after the 200°C anneal, which is in accordance with phase transition plot in Fig.1, where the NiSi formation starts at about 300°C. This is the case in Fig. 4b, where the Ni is fully consumed to build Ni_2Si and NiSi at the silicon substrate. In addition, $NiSi_2$ pyramids were formed at the silicide Si substrate interface, which could degrade pn junctions.

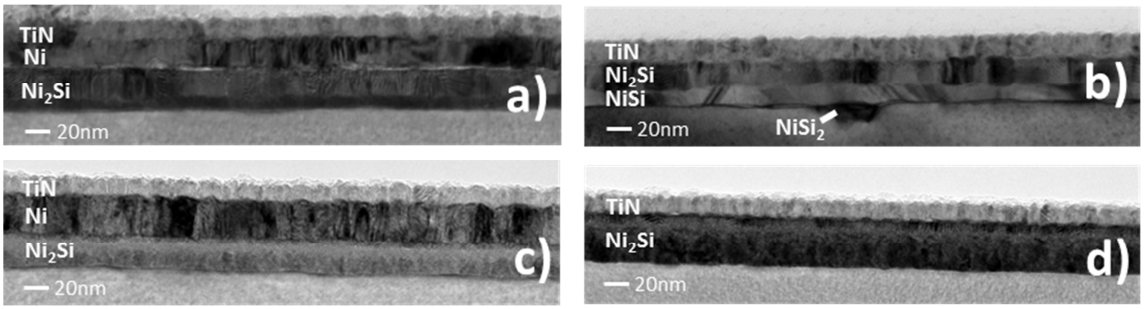

Fig.4: TEM cross section images after the silicidations: 40nm Ni annealed at 200°C for 5hours (a), 20nm Ni annealed at 300°C for 90s (b), 40nm NiPt annealed at 200°C 5hours (c), and 20nm NiPt after 300°C anneal for 90s (d).

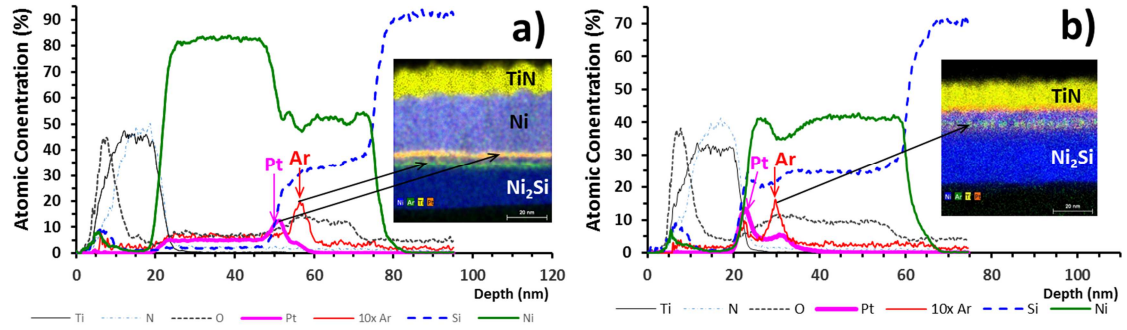

Fig.5: EDX Element depth profiles of 40nm NiPt annealed at 200°C 5hours (a), and 20nm NiPt after a 300°C anneal for 90s (b). The profiles were made on the TEM lamellas of Fig. 4c) and 4d).

The 200° annealed NiPtSi sample in Fig. 4c has a similar layer stack as the corresponding Ni sample (Fig. 4a). Surprisingly, no NiSi phase was found for the 300°C NiPtSi sample in Fig. 4d, although the NiSi formation in Fig. 2 sets in at about 300°C.

The element depth profiles of the NiPt silicide after a 200°C anneal for 5 hours is presented in Fig. 5a. The Pt concentration of 5% in the Ni layer equals the sputter target content. At the Ni to Ni_2Si interface the platinum significantly agglomerates and further diffuses into the Ni_2Si until the Ar defect band. This Ar defect band is formed by the in situ Ar preclean of the silicon substrate. It looks like, that the Ar hinders the Pt diffusion into the Ni_2Si towards the silicide silicon interface, where the Pt should segregate and suppress silicide defect formation such as $NiSi_2$ pyramids.

In the 300°C annealed NiPt sample (Fig. 5b) a Pt agglomeration occurs at the TiN Ni_2Si interface. At this elevated anneal temperature the Pt almost penetrates the Ar defect band. For a more homogenous Pt deviation across the silicide towards the silicon, the Ar defect band should be suppressed. Several options exist. First, the Ni or NiPt deposition is done without Ar pre clean after the HF dip, but this requires short delay times between HF dip and Ni(Pt) sputtering. Second, after HF dip an Ar free in situ clean in the metallization tool is implemented. This could be a sputter clean with an Ar free forming gas such as He/H_2 (4%), or the application of a remote plasma clean with NF_3 and NH_4 chemistry-called Siconi clean - and is described by Yang et al. (6).

Nickel and Nickel-Platinum Silicide Sheet Resistance

The silicide sheet resistance R_S can be applied to compare different silicidations, to evaluate silicide patterning effects such as linewidth effect, or to study its impact on device parameters such as maximum oscillation frequency f_{max} of HBTs.

The NiSi and NiPtSi sheet resistances ($R_{S\ Ni(Pt)Si:1.+2.Ann}$) are plotted versus the first anneal time for three temperatures of the first anneal (200°C, 230°C, and 300°C) in Fig. 6. At 300°C, the R_S saturates at 3.3 Ω for 20 nm Ni and 1.6 Ω for 40 nm Ni, respectively. This indicates full Ni consumption. The furnace anneals at 200°C and 230°C do not show any R_S saturation in the observed anneal-time range, since Ni is consumed only partially. The lowest Rs differences of NiSi and NiPtSi are found for the 300°C anneal, which is favored for the adjustment of low-ohmic NiSi in the next section.

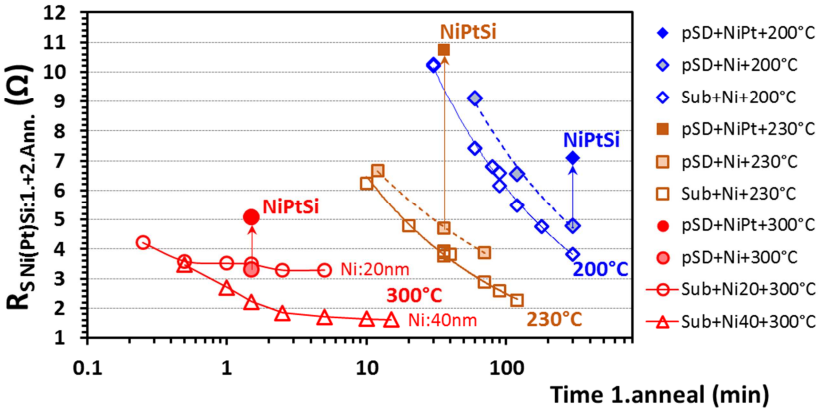

Fig.6: Plot of NiSi, NiPtSi sheet resistances ($R_{S\ Ni(Pt)Si:\ 1.+2.Anneal}$) vs. the first anneal time for the first anneal temperatures of 200°C, 230°C, and 300°C.

Fig. 7 presents the base poly silicide sheet resistance $R_{S\text{-}BasePoly\text{-}Silicide}$ for the silicide schemes, which are applied in the next sections. For 40nm Ni, the silicide schemes allow a NiSi R_S tuning range from 1.6 Ω to 9 Ω. The 200°C and 230°C anneals show low R_S deviations across the wafer because of the good temperature control of a furnace and furthermore negligible R_S differences of wide and narrow lines.

For the 200°C, 230°C, and 300°C NiPtSi schemes R_S increases of 1.5 Ω, 6 Ω, and 2 Ω compared to the corresponding NiSi formations are observed.

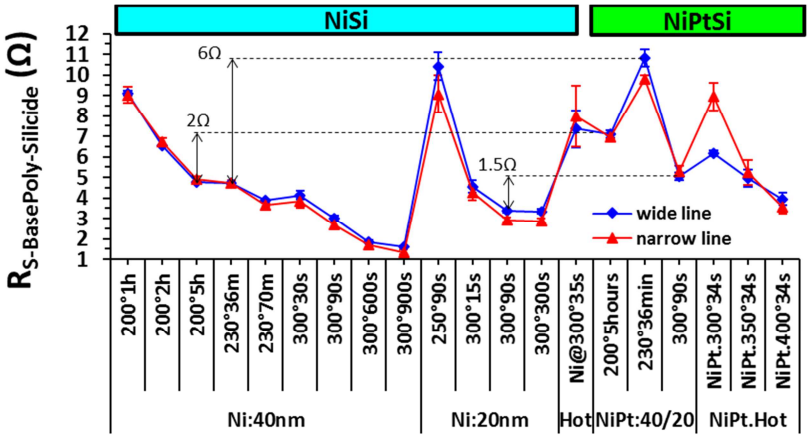

Fig.7: $R_{S\ BasePoly\text{-}Silicide}$ of wide (1,3µm) and narrow (130nm) base poly lines for NiSi and NiPtSi samples.

Impact of NiSi and NiPtSi Rs on HBT fmax

One figure of merit of SiGe-HBTs is the maximum oscillation frequency f_{max}, which depends by the following equation

$$f_{max} = \sqrt{\frac{f_T}{8\pi r_B C_{BC}}} \qquad [1]$$

on the transit frequency f_T, the base resistance r_B, and the collector-base capacitance c_{BC}. A silicide resistance variation could influence f_{max} by r_B.

HBTs with a single, asymmetric base contact of IHP's SG13S and SG13G2 BiCMOS technologies are chosen to demonstrate the impact of the base polysilicon NiSi Rs ($R_{S\ BasePoly\text{-}Ni(Pt)Si}$) on f_{max}. The asymmetric base-contacted HBTs allow a more flexible interconnection of the base, emitter, and collector areas compared to symmetric layouts, especially in the case of further downscaling, which is described in detail for the G2-HBT improvement by Heinemann et al. (1). The IHP SG13S- and SG13G2-HBTs are offered with f_{max} values of 340 GHz and 450 GHz using cobalt silicide with an Rs of 7 Ω. A detailed description of IHP's HBT generations is given by Rücker and Heinemann (7).

Fig. 8 shows the f_{max} dependence on $R_{S\ BasePoly\text{-}Ni(Pt)Si}$ of a SG13S-HBT (HBT1). The open circles present f_{max} vs. R_S for different Ni silicidations (Ni: 20nm, 40nm, with 1.anneals: 200/230/250/300°C and sintering according to Fig. 3). In that case, f_{max} could be increased from 342 GHz to 377 GHz by an R_S reduction from 10.4 Ω down to 3.3 Ω, respectively. Similar results deliver NiPtSi splits (the 3 low temperature and the 400°C NiPt deposition scheme according to Fig. 3). Here, a continues f_{max} increase from 333 GHz up to 373 GHz by lowering R_S from 10.8 Ω to 4.0 Ω is clearly visible.

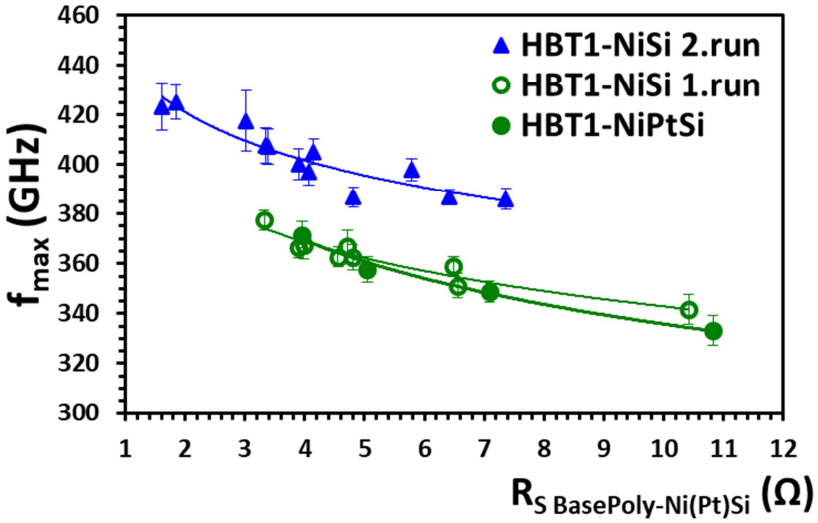

Fig.8: F_{max}-$R_{S\ BasePolySilicide}$ plot of an asymmetric base-contacted HBT of IHP's SG13S-BiCMOS (HBT1) technology using NiPtSi formations (solid circles), NiSi with a first run (open circles), and a NiSi with a second run (triangles).

In order to extend the Rs range down to 1.6 Ω a set of Ni silicidations was repeated in by a second run, which additionally includes anneals at 300°C for 600 s and 900 s. The f_{max} values (triangles) of this lot show an overall 30 GHz increase compared to the first NiSi run, which is due to fluctuations during HBT preparation. Nevertheless, a continous f_{max} increase from 386 GHz to 425 GHz by R_S lowering from 7.4 Ω to 1.6 Ω was achieved.

The f_{max}-R_S plot for the SG13G2-HBT2 for all the given NiPtSi silicide schemes of Fig. 3 is presented in Fig. 9. An f_{max} to R_S correlation clearly exists. A NiPt silicide resistance decrease from 10.9 Ω to 4.2 Ω results in an f_{max} increase from 427 GHz up to 531 GHz. This 104 GHz f_{max} rise of HBT2 is much higher than the corresponding 40 GHz increase of HBT1 for nearly the same silicide resistance range.

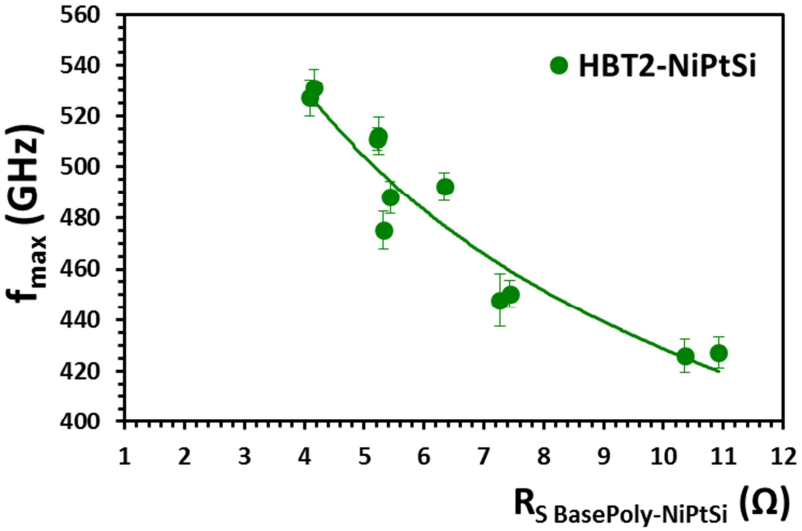

Fig.9: F_{max}-$R_{S\ BasePolySilicide}$ plot of an asymmetric base-contacted HBT2 of IHP's SG13G2-BiCMOS technology using NiPtSi formations.

The f_{max}-R_S data points in Fig. 8 and Fig. 9 could be described by power functions with exponents of HBT1 and HBT2 of about -0.1 and -0.23, respectively. Fig. 9 shows furthermore the f_{max} improvement potential for reduced R_S values below 4 Ω down to 1.6 Ω. Corresponding HBT preparations are still running.

In general, the results of Fig. 8 and Fig. 9 clearly demonstrate the f_{max} improvement potential by the reduction of the base polysilicon NiSi sheet resistance for HBTs with asymmetric base contacts.

Impact of NiSi and NiPtSi on Leakage Current of Diodes

In the previous section it was demonstrated that low-ohmic Ni(Pt)Si layers can significantly improve the maximum oscillation frequency for certain HBT constructions. In this section the questions should be answered: how do the Ni(Pt)Si layers interact with the MOSFET devices with respect to leakage currents and which Ni or NiPt silicidation scheme provides both larger HBT f_{max} and acceptable low leakage currents of the MOSFETs?

Ni silicide related MOSFET leakage issues are well-known, especially for large scaled CMOS technologies with ultra-shallow junctions and small gate length (8). Short channel control measures such as extension and halo implants can enhance these NiSi based effects (6). Three NiSi defect types which can degrade the source drain (SD) to well pn junction should be investigated: 1) silicide spikes such as $NiSi_2$ pyramids shortening in a perpendicular direction SD and well, 2) defects along the SD-STI (shallow trench isolation) interface, and 3) lateral silicide pipes towards the conducting channel.

Three types of pSD/n-well and nSD/p-well diodes are suitable to determine and distinguish these silicide based yield killers: area diodes to detect spikes, STI separated island diodes to recognize SD-STI defects, and diodes with long poly-gates on SD-well areas to determine pipes towards the MOSFET channel.

Fig. 10 presents the breakdown voltage (BV) versus the investigated NiSi and NiPtSi schemes of single area nSD/p-well and pSD/n-well diodes. The pSD/n-well diodes show for all silicide schemes BV of about -12V, which indicates no electrical active silicide defects in the perpendicular direction of the SD well junction. A similar behavior show the nSD/p-well diodes except for the NiSi layers annealed at 300°C for 600 s and 900 s. They have rather low diode BVs of 2 V, a clear indication of a silicide based degradation of the np junction. These low-ohmic NiSi layers (below 2 Ω) are rather thick - about 80nm. This enhances the probability of electrical active silicide defect formation. However, the NiPtSi layer deposited at 400°C is an example, that a 80nm thick silicide layer does not degrade the SD-well junction because it has a high diode BV of about 11V.

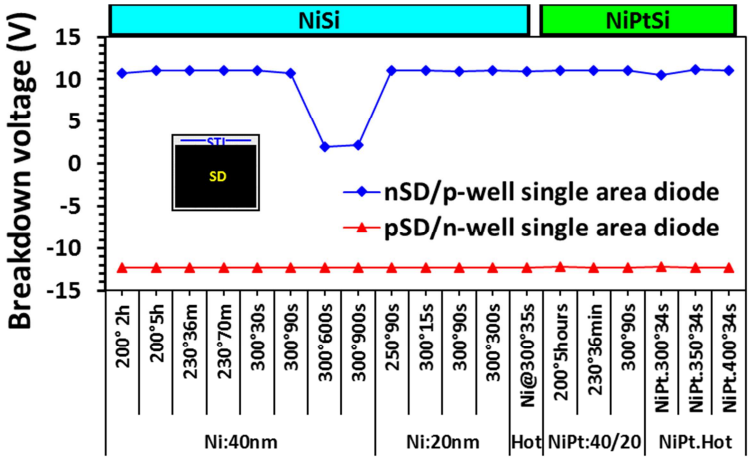

Fig.10: Breakdown voltage of nSD/n-well and pSD/p-well diodes for NiSi and NiPtSi first anneal splits followed by a 450° C sinter anneal.The diodes consist of single SD area (perimeter, area, and perimeter/area ratio of 850 µm, $3x10^4$µm^2 and 0.02 µm^{-1}) surrounded by STI.

The breakdown voltages versus the silicide splits of island shaped diodes (Fig.11) are significantly reduced for 300°C NiSi samples with long annealing times. In case of the pSD/n-well diode these reduced BV are due to silicide related defects at the SD-STI edge, because the corresponding values of area diodes (Fig. 10) do not show any BV impact. All the NiPtSi samples have no effect on the breakdown voltage, not even the one annealed at 300°C for 90s.

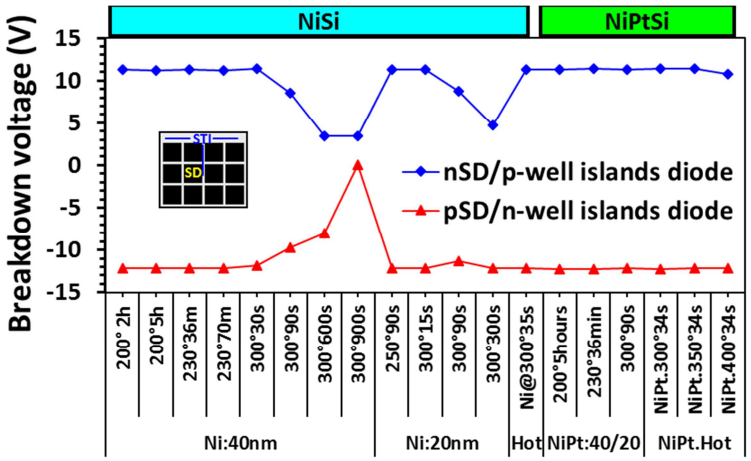

Fig.11: Breakdown voltage of nSD/n-well and pSD/p-well diodes for NiSi and NiPtSi first anneal splits followed by a 450° C sinter anneal. The diodes consist of 11400 SD islands (with SD perimeter, area, and perimeter/area ratio of $7x10^4$ µm, $3x10^4$ µm^2 and 2 µm^{-1}) separated by STI.

The leakage currents of MOS-like gate diodes on pSD/n-well and nSD/p-well are presented in Fig.12 together with inserted SEM images. For the pSD gate diodes, acceptable low leakage current values are observed only for the low temperature annealed NiSi layers at 200°C, 230°C, and 250°C as well as for all NiPtSi samples. The 300°C annealed Ni layers always cause elevated leakage currents. It is interesting to note, that between the "230°C, 70 minutes" and the "300°C, 30 s" NiSi samples the leakage current rises from $2x10^{-11}$ A to $1x10^{-7}$ A, although both samples have a similar thickness indicated by an R_S of about 4 Ω. As defect cause for the "300°C, 30 s" sample silicide

pipes towards the channel are most likely, because the corresponding pSD/n-well area and islands diodes did not display any pn junction degradation.

All NiPtSi samples show no impact on I_{Leak} of pSD gate diodes, although the silicide shape of the 300°C for 90s NiSi and NiPtSi layers (SEM inserts) resemble each other. The most impressive result in Fig. 12 is the shape of the thick NiPtSi layer in the lowest right SEM image of the 400°C-NiPtSi sample and the fact of low $I_{Leak\ pSD/n\text{-}well}$ of about $2x10^{-11}$A, although a significant silicide diffusion under the gate spacer occurs. This is a proof, how 5% platinum in the Ni layer can suppress - most probably by Pt agglomeration at the silicide towards the channel - the electrical active silicide defects. The corresponding nSD/p-well diode of the 400° NiPt sample demonstrates the limit of the Pt addition by an elevated I_{Leak} of $1x10^{-9}$ A. The reason is an enhanced lateral silicidation towards the channel for nMOSFETs which is described by Yamaguchi et al. (9). A closer look at the upper SEM image row of all nSD gate diodes indicates a larger silicide diffusion underneath the gate spacers compared to the corresponding pSD gate diodes in the lower row. The largest silicide under diffusion is induced at the 400° NiPt silicidation scheme resulting in an elevated I_{Leak}.

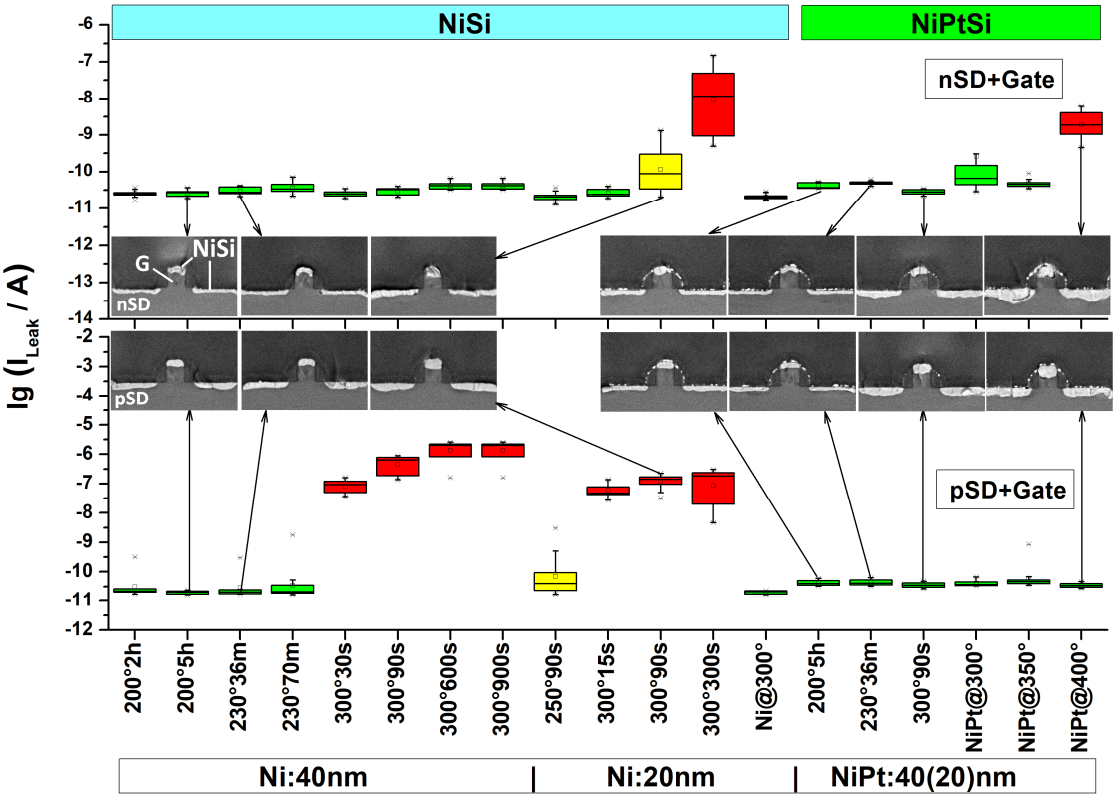

Fig.12: Leakage current I_{Leak} of nSD/p-well and pSD/n-well poly gate diodes versus NiSi and NiPtSi formations. I_{Leak} was measured with floating gate.

In result, low-ohmic NiSi layers formed by first anneals at 300°C and longer times show significant diode leakage current enhancement by shortening the SD/n-well junction towards the channel, in perpendicular direction, or on the SD-STI edge area. These defects could be suppressed by application of reduced first anneal temperatures such as 200°C and 230°C at the expense of higher silicide sheet resistances according to Fig. 6. However, the use of NiPt layers can significantly improve the leakage behavior of MOSFET devices.

Summary and Conclusions

The goal of this paper was to find out from several two-step silicidations of Ni or NiPt layers a suitable process for IHP's upcoming BiCMOS technologies, which results in low silicide sheet resistances for high cutoff frequencies of bipolar transistors without degradation of MOSFETs leakage currents.

An f_{max} increase for HBTs with an asymmetric base contact by lowering the NiSi or NiPtSi sheet resistance down to 4 Ω was demonstrated. A further reduction of the silicide resistance to 1.6 Ω associated with an f_{max} increase was shown for NiSi layers applying a two-step silicide scheme of 300°C and 450°C. However, such NiSi layers generate elevated leakage currents in MOSFETs by SD well spikes and mainly by pipes towards the channel. An acceptable leakage current reduction is possible for reduced first anneal temperatures such as 200°C and 230°C at the expense of increased silicide sheet resistances. The application of NiPtSi layers significantly suppresses the formation of all electrical active silicide defects especially the pipes towards the channel, even for the two-step silicidation schemes of 300°C and 450°C. For this silicide sequence the NiPtSi sheet resistance is only slightly increased compared to those of NiSi.

In summary, the two-step NiPtSi silicide process is a promising choice for upcoming IHP BiCMOS technologies both to enhance f_{max} of certain HBT constructions by low-ohmic silicide, and low MOSFET leakage current.

The NiPt silicide formation could be improved by suppressing the Ar defect band in the silicide which is formed by the Ar sputter clean. This Ar defect band possibly hinders the Pt diffusion through the silicide to the silicide silicon interface to more efficiently suppress silicide based defects.

Acknowledgments

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