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Impact of nickel silicide on SiGe BiCMOS devices

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Abstract

Nickel silicide (NiSi) can improve the RF performance of SiGe hetero bipolar transistors (HBT) compared to cobalt silicide (Heinemann *et al* 2016 *IEDM Tech. Dig.* 51–4). In this paper, the impact of different procedures to form NiSi on HBT and MOS devices of a 0.13 μm BiCMOS cobalt silicide technology is studied. The different NiSi formations are carried out by partly or fully Ni consumption (PC, FC) for low temperature furnace and low pressure anneals. Our investigations indicate, PC results in rough silicide surfaces and substrate interfaces, whereas FC leads to smooth surfaces and interfaces associated with lower resistivities. FC nickel silicidation at 300 °C and 450 °C exhibits an excessive NiSi growth on the STI edges of n doped source drain (N^+SD) regions, reducing the breakdown voltage to substrate or p well. An enhanced NiSi growth is found for all investigated silicide schemes on narrow P^+SD regions along polysilicon gates. The leakage current of these structures is caused by enlarged lateral silicidation towards the gates. The enhanced lateral NiSi growth could be suppressed by partly Ni silicidation with furnace anneals at 200 °C or 230 °C.

Keywords: nickel silicide, partly nickel consumption, fully nickel consumption

(Some figures may appear in colour only in the online journal)

1. Introduction

Since the 65 nm CMOS logic technology node the cobalt silicide is replaced by nickel silicide (NiSi), because it has a lower formation temperature and a lower silicon consumption [1]. However the NiSi comes along with new challenges. The higher resistive $NiSi_2$ phase formed above 750 °C has to be suppressed [2]. On heavily boron doped silicon the formation temperature of the unwanted $NiSi_2$ phase is reduced down to 500 °C in case of fully nickel consumption [3], resulting in elevated leakage currents in SD well junctions. The fully nickel consumption can induce an enlarged NiSi growth in narrow silicon lines associated with unwanted lower sheet resistances, often called the reverse line width effect. Solutions to suppress the $NiSi_2$ formation and to reduce the NiSi reverse line width effect, such as the introduction of NiPt, a partly Ni consumption silicidation combined with short low temperature anneals were proposed by Futase *et al* [3].

Only a few papers study the impact of NiSi on the SiGe hetero bipolar transistors (HBT) performance. Bae *et al* [4] demonstrated a 10% increase of the maximum oscillation frequency (f_{max}) from 35 to 38 GHz substituting titanium silicide by NiSi. Geynet *et al* [5] replaced cobalt silicide by NiSi among other measures of a low thermal budget HBT preparation to reduce the dopant diffusion. In result they demonstrated an increase of the transit frequency f_T from 340 to 410 GHz. Previously we have shown in a bipolar-only technology flow, that the use of NiSi instead of cobalt silicide can improve the f_{max} of npn SiGe HBTs up to 12% [6]. Now, the impact of NiSi both on HBTs and on MOS devices of a 0.13 μm BiCMOS technology is studied, which was originally developed with cobalt silicide.

In this paper, the influence of different NiSi formations on the silicide phases and morphology of the grown NiSi layers is studied in the first part. Secondly, the impact of different formed NiSi layers on the HBT performance is demonstrated. Their influence on the leakage behavior of source drain well diodes and on the SD line width effect of the NiSi sheet resistance (R_S) is investigated. These investigations were performed to determine a suitable NiSi process

Table 1. Studied nickel silicide schemes and Co reference.

Metal		Ni:15 nm		Ni:20 nm			Ni:40 nm						Co:10 nm
1.Anneal	*T*, *t*	450 °C 30 s	350 °C 30 s	300 °C 30 s	250 °C 90 s	300 °C 15 s	300 °C 90 s	230 °C 12 min	230 °C 36 min	230 °C 70 min	200 °C 1 h	200 °C 2 h	200 °C 5 h	Reference
	Tool	LP - low pressure anneal					Furnace anneal							RTP
Ni consumption		FC (fully Ni consumption)		PC (partly Ni consumption)		FC	PC (partly Ni consumption)							
2.Anneal		no					RTP: 450 °C, 30 s							RTP

for both HBT and MOS devices of the studied BiCMOS technology. In result, the favorite NiSi process consists of a two step formation with a furnace anneal, a selective etch and a final RTP anneal, where the Ni is partly converted to NiSi.

2. Experimental

200 mm p-type Si (001) bare wafers were used to study the NiSi phase formation and morphology by x-ray diffraction (XRD) and SEM. On patterned wafers applying a 0.13 μm BiCMOS technology the influence of Ni silicidation scheme on HBT parameters, on P^+ or N^+ diode breakdown voltage (BV) (island shaped and single SD areas), on gate diode leakage, and on R_S of narrow and wide SD lines was investigated.

The NiSi formation starts with a native oxide removal of the silicon areas by diluted hydrofluoric acid. Within a short queue time (minutes), the wafers were handled into a conventional Endura metallization tool (Applied Materials) to perform a degassing and an Ar sputter clean before the nickel layer was sputtered (DC magnetron) at room temperature which was finally covered by a 15 nm reactively sputtered TiN cap layer to suppress the Ni oxidation. The nickel silicidation contains a first low temperature anneal, a piranha etch of the TiN and not converted Ni and mostly a final anneal. In absence of an RTP tool for temperatures below 450 °C, an Endura heat chamber (low pressure at 10 Torr, 30 K s^{-1} ramp rate) was applied for the first silicide anneal between 250 °C and 450 °C, as well as an atmospheric furnace with nitrogen carrier gas (ASM A400, 1 K s^{-1} ramp rate) in the temperature range between 200 °C and 250 °C, respectively. The investigated NiSi formation schemes with the cobalt reference are summarized in table 1.

XRD measurements for the NiSi phase determination were performed with a 9 kW Smart-Lab diffractometer from Rigaku using CuKα radiation.

3. Results and discussion

3.1. NiSi formation—texture and morphology

Figure 1 shows the NiSi phase formation as a function of temperature by an *in situ* XRD measurement (details in [7]). The phase formations from Ni to Ni_2Si and NiSi are clearly visible, only the low $NiSi_2$ intensity is not noticeable. The (111)-oriented Ni is observed up to 250 °C. The Ni transforms into Ni_2Si in a temperature range between 230 °C and 330 °C, and above 330 °C up to 770 °C the targeted NiSi phase is present. For a two-step nickel silicidation scheme, the formation of the nickel rich Ni_2Si phase is targeted for the first anneal.

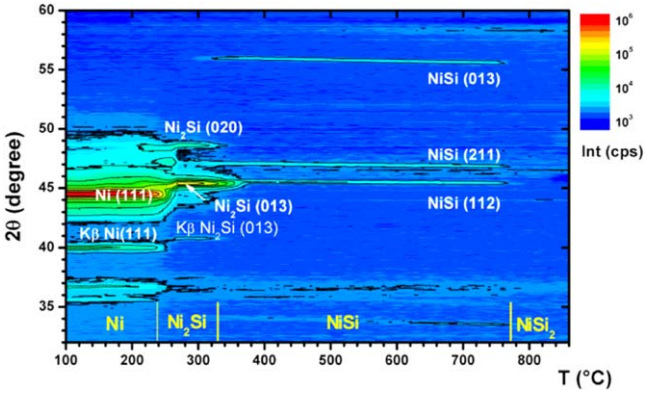

Figure 1. 2Θ to temperature plot of an *in situ* XRD measurement in 10 K intervals of 40 nm Ni.

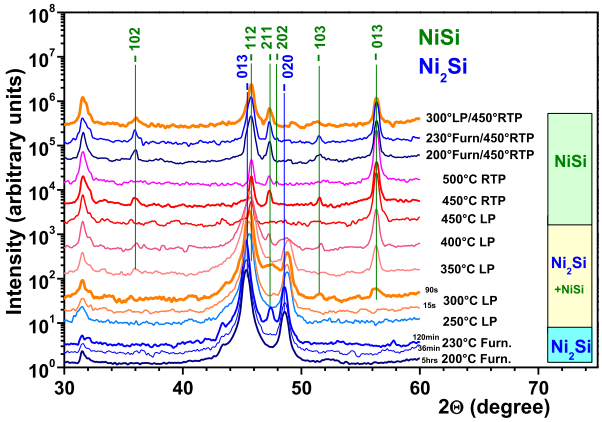

Figure 2. Specular ω–2Θ scans for Ni samples annealed at different temperatures with low pressure tool (LP), furnace, RTP and two-step combinations and after TiN etch.

Therefore, the nickel phase formations for the low pressure and furnace anneals were investigated in a temperature range of 200 °C–500 °C and plotted in figure 2.

Here, a clear dependence of the nickel phases on the temperature is shown. At a furnace anneal at 200 °C only Ni_2Si phase is present. Between 230 °C and 400 °C a mixture of Ni_2Si and NiSi phases exists, and pure NiSi is formed above 450 °C as well as for two-step formations. It is interesting to note, that even at a low temperature of 230 °C (furnace 120 min) the NiSi phase is present. The pressure and the ramp rates of the two studied anneals have no significant influence on the nickel phase formation.

The morphology of NiSi layers formed by partly and fully Ni consumption on undoped Si is shown in figure 3. The

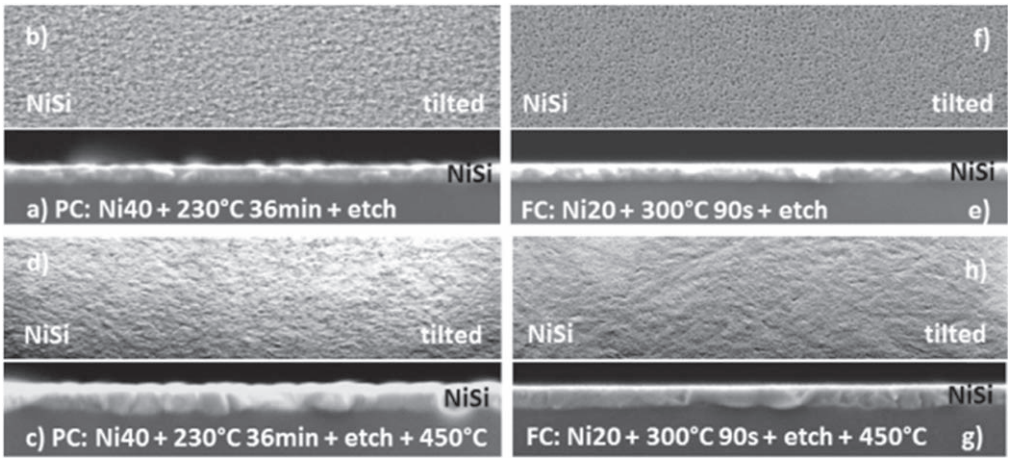

Figure 3. NiSi by partly Ni consumption post 1.anneal/etch (a), (b), post 2.anneal (c), (d) and by fully Ni consumption post 1.anneal/etch (e), (f) and post 2.anneal (g), (h).

PC NiSi exhibits a rough surface after a furnace anneal and etch (figures 3(a), (b)). This rough surface remains even after the second sinter anneal (figures 3(c), (d)). The FC NiSi sample shows a rather smooth surface after the first anneal and etch (figures 3(e), (f)).

This smooth surface remains even after the second anneal in figures 3(g) and (h). The FC NiSi has also a smoother silicide-Si interface (figure 3(g)) than the PC NiSi in figure 3(c), which corresponds to a finer NiSi grain structure. This difference in surface roughness of FC or PC formed NiSi does not depend on the LP or furnace anneal and was also observed on SD areas.

On SD areas FC samples show minimum resistivities of about 14 $\mu\Omega$ cm, whereas PC samples of the same NiSi thickness have 16 $\mu\Omega$ cm, respectively.

3.2. Resistance of narrow and wide silicide SD lines

It is reported that NiSi shows a reverse line width effect, e.g. R_S decreases by downscaling the line width [8, 9]. We investigated this effect by two types of SD lines: one wide line of 1.5 μm width and 10 narrow lines each of 0.15 μm width. Both line types have a length of 200 μm. The R_S results of the narrow and wide N^+SD/P^+SD lines for the investigated silicide schemes are shown in figure 4.

On N^+SD areas (figure 4(a)), the $CoSi_2$ reference shows a R_S difference between narrow and wide lines (ΔR_S) of 0.7 Ω. The largest ΔR_S of 1.8 Ω was found for the FC-NiSi formation at 450 °C. A reduction of the first NiSi formation temperature increases the narrow line R_S. This is due to a retarded consumption of the surrounding nickel layer of the narrow line in case of fully Ni consumptions (15 and 20 nm Ni, see table 1).

The Ni-20 nm 300 °C 90 s sample exhibits a low ΔR_S of 0.4 Ω, but at the expense of a strong NiSi growth downwards the STI edge (inserted image), which can cause leakage issues, which is discussed below.

It is interesting to note, that in case of the furnace anneals at 230 °C the ΔR_S of wide to narrow N^+SD lines changes from −0.8 Ω to +0.5 Ω if the time is increased from 12 min to 70 min, and at 200 °C the ΔR_S is changed from −1.6 Ω to 0 Ω for times of 1 h and 5 h, respectively. The same behavior was observed from Lauwers *et al* for As doped SD lines [8]. They argue that initially the NiSi formation is slower in narrow N^+SD lines. In conclusion, the R_S of narrow and wide N^+SD lines is equalized for furnace anneals at 200 °C and 230 °C targeting R_S values of 6.4 Ω.

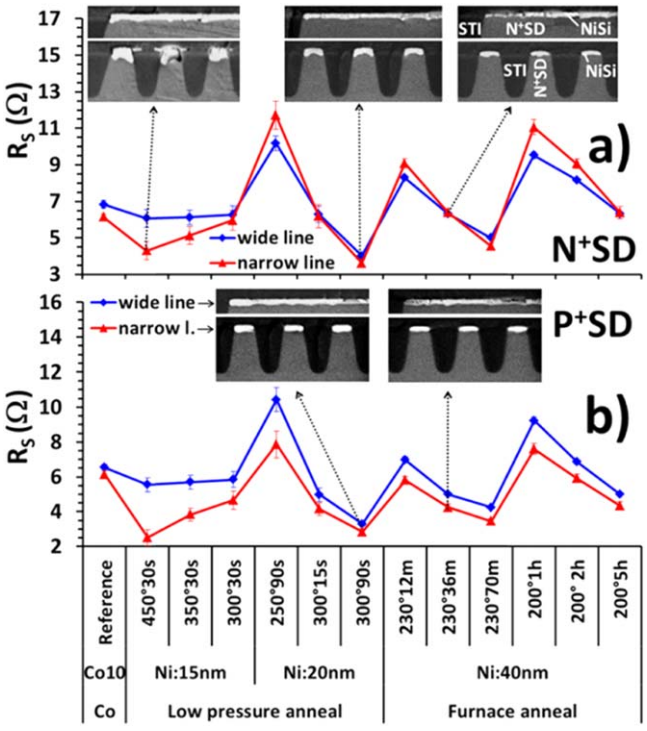

Figure 4. Sheet resistance R_S of narrow (150 nm) and wide (1.5 μm) silicide SD lines for (a) N^+SD and (b) P^+SD areas.

On P^+SD areas (figure 4(b)) all silicides show larger R_S for wide lines compared to the narrow ones. The lowest ΔR_S of 0.4 Ω are observed for $CoSi_2$ and NiSi formed at 300 °C 90 s of 20 nm Ni. The highest ΔR_S of 3 Ω was found for the 450 °C NiSi split. The ΔR_S can be reduced by lowering the first anneal temperature. The SEM inserts indicate that the

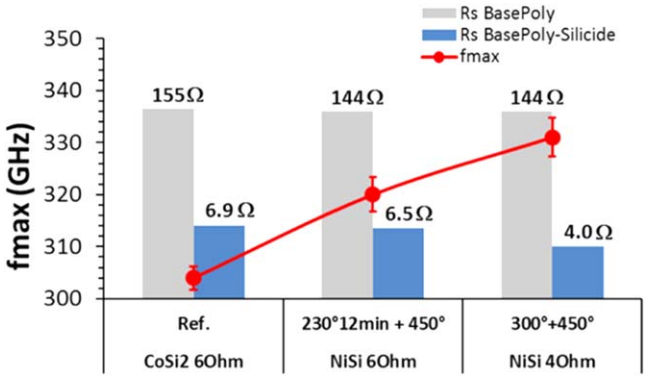

Figure 5. f_{max} (line) and base polysilicon R_S without (gray) and with silicide (blue) for three silicide layers. The corresponding transit frequencies f_T are 247, 249 and 251 GHz.

narrow P^+SD lines consist of homogeneous NiSi layers without enhanced growth at the SD-STI edge. The ΔR_S of P^+SD for the furnace anneals is only marginally reduced down to +0.8 Ω. This means, the initial NiSi formation on narrow P^+SD lines is not as slow as on N^+SD ones.

With respect to the NiSi R_S line width effect the furnace anneals at low temperatures and a partly Ni consumption are the favorite silicidation processes, because they allow to adjust small R_S differences of narrow and wide SD lines.

3.3. Impact of NiSi on HBT parameters

The silicide impact on the maximum oscillation frequency f_{max} of SiGe HBTs is studied in this section. Figure 5 shows the sheet resistance of the base polysilicon (with and without silicidation) and the f_{max} of a npn SiGe HBT for the cobalt and two NiSi.

The base polysilicon R_S (Rs BasePoly) drops from 155 Ω for $CoSi_2$ to 144 Ω for the NiSi layers. This decrease is associated with a reduced dopant deactivation due to the lower NiSi formation temperatures and the absence of a contact anneal.

The f_{max} is increased from 304 GHz for $CoSi_2$ to 320 GHz for the NiSi 6 Ω layer, which is attributed to the reduced Rs BasePoly and the contact resistance between NiSi and base polysilicon (not shown).

A further f_{max} increase to 331 GHz is achieved by the low ohmic 4 Ω NiSi. All in all these results show an improvement of HBT RF performance by the introduction of NiSi. In the next sections the impact of the cobalt and NiSi formation on diode leakage currents is investigated.

3.4. NiSi impact on SD diode BV

The BV of SD well diodes with island shaped SD areas or one single SD area can help to evaluate silicide related issues at the bulk silicide interface and the SD-STI edge. Figure 6(a) shows this BV of N^+ islands diodes for the investigated silicide splits. Two of them have either reduced BV of about 9 V (Ni:15 nm at 450 °C) or a large BV scattering down to 7 V (Ni:20 nm at 300 °C 90 s). In case of the P^+ islands

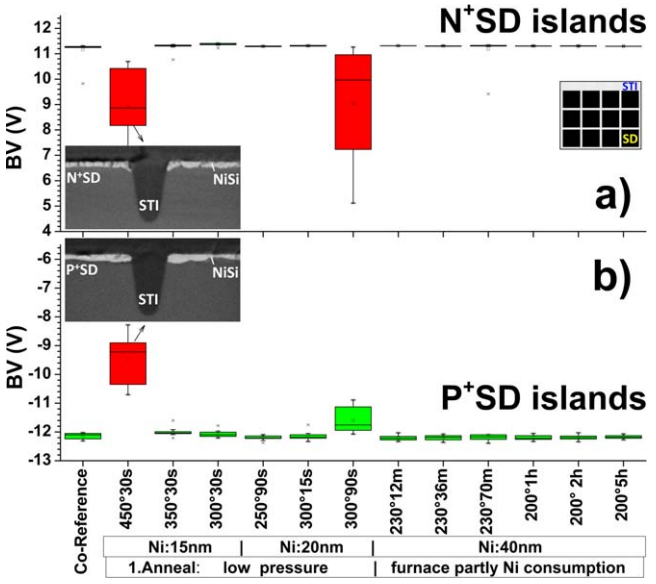

Figure 6. Breakdown voltage of (a) N^+P well and (b) P^+N well diodes consisting of SD islands (11 400 diodes) with a SD perimeter, a total SD area and a perimeter/area ratio of 7.4 × 10^4 μm, 3.7 × 10^4 μm^2 and 2.5 μm^{-1}, respectively.

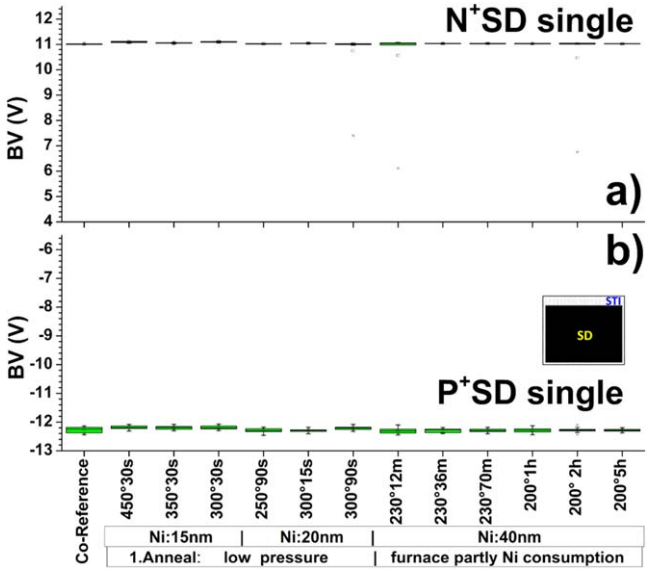

Figure 7. BV of (a) N^+P-well and (b) P^+N-well diodes consisting of one single SD area with a SD perimeter, area and a perimeter/area ratio of 850 μm, 3.0 × 10^4 μm^2 and 0.02 μm^{-1}, respectively.

diodes (figure 6(b)), only the 450 °C-NiSi variant has a pronounced lower mean BV of about −9.5 V.

The BV of SD well diodes having only one single SD area are plotted in figure 7. Both N^+SD and P^+SD diodes show for all NiSi splits the same BV as the cobalt reference. Only 1 or 2 edge chips of the N^+SD diodes have BV lower 8 V, which might be attributed to patterning irregularities at the wafer edge.

The major geometric difference of both diode types consists in the larger perimeter/area ratio (about a factor of 100) of island compared to single area ones. Because the

single area diodes do not show any significant silicide impact on the BV, it can be concluded that the BV issues in figure 6 are due to SD-STI edge effects.

In case of the N^+SD islands diodes, an excessive NiSi down growth along the STI edge occurs for the fully consumed Ni splits at 450 °C 30 s and 300 °C 90 s (SEM inserts figures 4(a) and 6(a)).

This enlarged NiSi thickness possibly combined with defects at the STI-edge can increase the recombination and therefore reduce the BV at constant forced current for the reverse biased N^+P island diodes.

To overcome these BV issues of island shaped SD diodes it is necessary to prevent an excessive Ni diffusion and the resulting NiSi formation. This could be achieved by a reduction of temperature and/or time (partly Ni consumption) of the first NiSi anneal. It is shown in figure 6, that the NiSi formation could be adjusted in that way, that no silicide related BV issues occur.

3.5. NiSi impact on gate SD diode leakage current

MOS like diodes with gate polysilicon lines are suitable for the determination of silicide related leakage currents generated at the silicide bottom to SD interface or by the lateral silicidation towards the gate.

Figure 8 presents the leakage currents of such P^+ gate and N^+ gate diodes for the investigated silicide formations. In case of the N^+ gate diodes (figure 8(a)), only the 450 °C NiSi layer shows a high leakage current of about 5×10^{-8} A.

The NiSi formed at 300 °C 90 s has a larger leakage current scattering, whereas the insert exhibits a thin even NiSi layer on N^+SD, which looks quite similar to the cobalt silicide reference (inserts). The layers of all other silicidation schemes do not show any increased leakage currents of the N^+ gate diode.

In case of the P^+ gate diodes a large number of elevated leakage currents are presented in figure 8(b) with respect to the cobalt reference. Mainly the samples of the low pressure anneal group at temperatures equal and above 300 °C show high leakage currents larger than 1×10^{-9} A. The insert of the Ni-20 nm 300 °C 90 s sample shows an excessive NiSi growth on the P^+SD area, which looks like the $NiSi_2$ pyramide growth reported by Futase *et al* [3]. The NiSi layers formed by a PC furnace silicidation show mean leakages below 1×10^{-10} A with only a few outliers. Only the leakage current of the 230 °C 12 min sample shows an increased scattering across the wafer. The inserts of these samples indicate an enlarged NiSi growth on P^+SD. This indicates that the $NiSi_2$ formation on P^+SD is not suppressed by a partly Ni consumed silicidation at low temperatures as demonstrated by Futase [10] applying NiPt instead of Ni.

A careful view on the inserts of the P^+ gate diodes shows in case of the NiSi formed at 300 °C 90 s a lateral silicide growth under the gate spacer, whereas for the furnace samples the silicide growth immediately stops at the spacer. This enhanced lateral silicidation is responsible for the pn leakages. Even the insert (Ni:20 nm 300 °C 90 s) of the N^+ gate diode indicates an enhanced lateral nickel silicidation. The

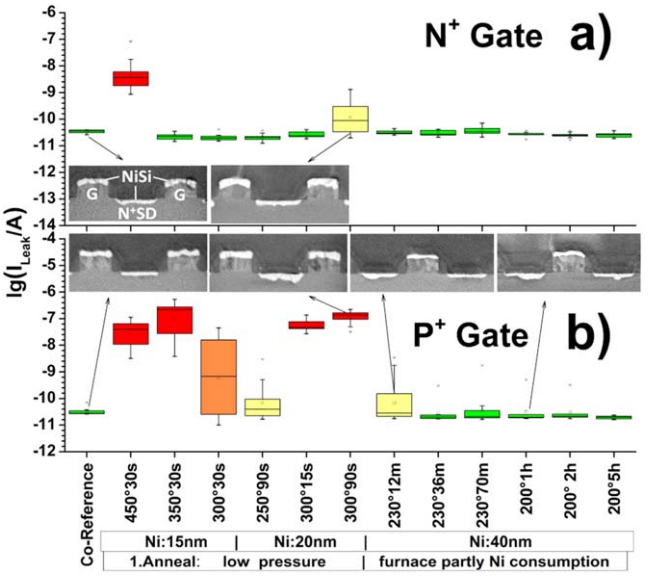

Figure 8. Leakage currents between SD and well (floating gate) for the silicides on N^+ gate polysilicon (a) and P^+ gate polysilicon (b) diodes with SEM inserts.

lateral silicidation as a leakage root cause is confirmed by P^+ gate diodes with relaxed halo and extension implantations, where the pn junctions are shifted towards the gate. They have much lower leakage currents. Even the leakage current differences of the two samples Ni:20 nm at 300 °C 15 s ($I_{Leak} > 1 \times 10^{-7}$ A) and Ni:40 nm 230 °C 36 min ($I_{Leak} < 1 \times 10^{-10}$ A) could be explained with the enhanced lateral silidation for the 300 °C anneal, because both PC silicidations form similar NiSi layers of 34 nm thicknesses and 5.0 Ω sheet resistance. A further NiSi thickness increase (Ni:40 nm 230 °C 70 min) does not affect the leakage current. The lateral silicidation is propagated by higher temperatures (diffusivity), and in case of the FC-silicidation by the additional Ni contribution from the spacers.

The results of this section show an excessive NiSi growth on heavily boron doped Si. The lateral nickel silicidation may influence the leakage behavior of P^+ gate diodes. This leakage behavior (lateral silicidation) can be tuned by the silicidation process. Best leakage performance is achieved by silicidations of partly Ni consumption at low temperature furnace anneals for the pn and np junctions of the investigated 0.13μ BiCMOS technology.

For an improved process stability and for steeper and shallower SD junctions, the excessive NiSi growth on P^+SD should be reduced by optimization of the second NiSi anneal (fast), by the adjustment of the crystalline morphology of narrow P^+SD lines between gate polysilicon, and by the application of NiPt instead of Ni.

4. Conclusions

It was found, that the NiSi phase formation only depends on the temperature and the time and not on the ramp rates of the

studied furnace and low pressure anneals. At a temperature of 200 °C only the nickel rich Ni_2Si phase was observed. Between 230 °C and 400 °C a mixture of Ni_2Si and NiSi phases exists, whereas above 450° only NiSi was found. The nickel silicidation scheme impacts the NiSi morphology. A partly Ni consumption results in relative rough NiSi surface and interface, whereas fully Ni consumed NiSi layers show smoother surfaces as well as substrate interfaces, finer grains, and lower resistivity.

The line width effect of the NiSi sheet resistance of SD areas can be controlled by the silicidation scheme, whereas similar R_S differences of wide and narrow lines as the cobalt reference are achieved for partly Ni consumption by furnace anneal. N^+SD and P^+SD island diodes show only for two nickel silicidations impacts on the diode BV, which are correlated with an enhanced NiSi thickness at SD-STI edge. Even these two NiSi formations have increased leakage currents of gate polysilicon N^+SD diodes. Gate P^+SD diodes exhibit an excessive NiSi growth on narrow heavily boron doped SD areas. The large leakage currents of these P^+ gate diodes are attributed to the lateral nickel silicidation towards the gates, which mainly occurs at elevated temperatures of the first silicide anneal (300 °C and above) in combination with a fully Ni consumption. A temperature reduction (200 °C or 230 °C) of the first anneal associated with a partly Ni consumption leads to acceptable leakages of the pn and np junctions of the investigated 0.13 μm BiCMOS technology.

For an improved process stability and for steeper and shallower SD junctions, the excessive NiSi growth on P^+SD should be suppressed by optimization of the second NiSi anneal (fast), by the adjustment of the crystalline morphology of narrow P^+SD lines between gate polysilicon, and by the application of NiPt instead of Ni.

Acknowledgments

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