Ge / SiGe Multi Quantum Well Fabrication by Using Reduced Pressure Chemical Vapor Deposition

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Abstract

In this paper we have deposited structures comprising a stack of 10 periods made of 15 nm-thick Ge multi quantum well (MQW) enclosed in 15 nm-thick $Si_{0.2}Ge_{0.8}$ barrier have been deposited on SiGe virtual substrates (VS) featuring different Ge contents in the 85% - 100% Ge range to investigate the influence of heteroepitaxial strain on the $Si_{0.2}Ge_{0.8}$ and Ge growth. With increasing Ge concentration of the VS, growth rate of the $Si_{0.2}Ge_{0.8}$ in the MQW increases. Si incorporation into the $Si_{0.2}Ge_{0.8}$ layer becomes also slightly higher. However, almost no influence of the growth rate is observed for Ge growth in the MQW. We argue that the increased tensile strain promotes the Si reaction at the surface. In the case of the $Si_{0.2}Ge_{0.8}$ growth on Ge, we observe a smeared interface due to the Ge segregation during the growth. Furthermore, we observe that this interface width increases with increasing Ge concentration of VS. We attribute this observation to the increased segregation of Ge driven by the increased strain energy accumulated in the in the $Si_{0.2}Ge_{0.8}$ layers. We also observed that the MQW layer "filters-out" threading dislocations formed in the VS.

Keywords

Ge, SiGe, Epitaxy, Chemical vapor deposition, Strain, Dislocation

1. Introduction

Group-IV heteroepitaxy has become widely established for various semiconductor device fabrications [1-6]. In order to realize the group-IV heteroepitaxy, it is of paramount importance to correctly manage the lattice strain due to the lattice mismatch possibly existing between epilayer and substrate. (In the case of Ge growth on Si, lattice mismatch is 4.2% [7]). During the initial stage of the Ge growth on Si, the heteroepitaxial strain induces local elastic deformation at the heterointerface interface. After exceeding a critical thickness, of few-nm only in the Ge/Si case, plastic relaxation occurs. The lattice mismatch is thus accommodated by inserting high density of misfit dislocations (MD) and threading dislocations (TD) [8]. In the case of SiGe growth on Si or Ge surface, critical thickness is larger compared to that of the Ge growth on Si because of a reduced lattice mismatch [9, 10]. Therefore, strain management during the growth is even more important for the heteroepitaxial growth of SiGe, because of the initial pseudomorphic growth the relaxation of SiGe will not occur until reaching much thicker thickness compared to that of the Ge growth on Si.

The group-IV heteroepitaxy processes with severe control of the strain are now commonly applied for device performance improvement. For example, Si:C and SiGe heteroepitaxial growth are widely used for CMOS technologies to boost carrier mobility in channel region by strain engineering [11-14]. SiGe with graded Ge concentration layer is used for base epitaxy of heterobipolar transistors to accelerate carrier in the base region [15-19]. The group-IV heteroepitaxial growth is also applicable to extend functionality of integrated circuit. In order to further extend functionality of the CMOS technologies according to a “More than Moore” approach, monolithic integration of Ge photodiodes and infra-red sensors are of also of major interest [20-22].

Introducing high quality SiGe / Ge superlattice (SL) structure has a potential to realize high efficient Ge multi quantum well (MQW) cascade laser [23-27]. In order to fabricate the SiGe / Ge MQW cascade laser, high quality and precisely controlled SiGe / Ge SL layer fabrication process is required. To realize the high crystal quality and precisely controlled SiGe / Ge MQW structures, influence of strain on the Ge and SiGe growth has to be investigated. In this study, we fabricated $Si_{0.2}Ge_{0.8}$ / Ge MQW structures on Ge and SiGe virtual substrate (VS) with different Ge content and discuss the influence of strain on $Si_{0.2}Ge_{0.8}$ and Ge growth. In this paper, influence of strain on the $Si_{0.2}Ge_{0.8}$ and Ge growth rate as well as steepness of the interface are also discussed in addition to data already published in [28].

2. Experimental

Epitaxial $Si_{0.2}Ge_{0.8}$ / Ge MQW fabrication is carried out by using a reduced pressure (RP) chemical vapor deposition (CVD) system. Si(100) substrates are used. H_2 is used as a carrier gas and SiH_4 and GeH_4 are used as growth precursor gases. For a Ge VS preparation, ~2 μm thick Ge is deposited by following procedure. After standard radio corporation of America (RCA) clean, the Si(100) wafer is loaded into the RPCVD reactor and baked at 1000^{o}C in RP H_2 to remove native SiO_2. After that the wafer is cooled down to 350^{o}C. During the cooling carrier gas is changed from H_2 to N_2 at 600^{o}C to form a hydrogen-free Si surface. After temperature stabilization, a Ge seed layer is deposited using N_2-GeH_4 gas mixture. Afterwards the wafer is heated up to 550^{o}C in H_2 environment and the deposition is continued by growing the main Ge layer part using H_2-GeH_4. To improve crystal quality of the 2 μm thick Ge, cyclic annealing at 800^{o}C is performed by interrupting the Ge deposition process at 800^{o}C for several times [29-31]. To fabricate SiGe VS with 95%, 90% and 85% Ge content, ~500 to ~600 nm thick SiGe layer deposition using H_2-SiH_4-GeH_4 gas system followed by postannealing at 850^{o}C is performed on a ~1.5 μm thick Ge layer deposited by the cyclic annealing process. By

this reverse graded buffer approach, high crystal quality of SiGe VS deposition is possible comparable to that of direct SiGe deposition on Si substrate [32]. After the VS fabrication, the wafers are unloaded from the RPCVD reactor and cleaned by HF dip and loaded into the RPCVD reactor again. Then the wafer is baked at 800^{o}C to remove native oxide. Afterwards 10 cycles of Ge and $Si_{0.2}Ge_{0.8}$ layers are deposited at 500^{o}C using H_2-GeH_4 and H_2-SiH_4-GeH_4 system, respectively. Target thickness of the Ge and the SiGe layers are 15 nm. The 10 cycles of the $Si_{0.2}Ge_{0.8}$ / Ge MQW deposition is performed on the VS with 85%, 90%, 95% and 100% Ge content with identical process condition to check influence of the strain on the $Si_{0.2}Ge_{0.8}$ and Ge growth.

X-ray diffraction (XRD) is used for periodicity and degree of relaxation measurements. Cross section transmission electron microscope (TEM) is used for crystallinity and profile analysis. Energy dispersive X-ray spectrometry (EDX) and X-ray photoelectron spectroscopy (XPS) with monochromated Al Kα (1486.7 eV) are used for Si composition analysis of the deposited Ge / SiGe SL. Threading dislocation density (TDD) is measured by combination of Secco defect etching and angle view scanning electron microscope (SEM) measurement.

3. Results and Discussion

In Fig. 1a and 1b, $Si_{0.2}Ge_{0.8}$ and Ge thicknesses in the $Si_{0.2}Ge_{0.8}$ / Ge MQW deposited on VSs with 85%, 90%, 95% and 100% Ge content are shown. In the case of the $Si_{0.2}Ge_{0.8}$ layer (Fig. 1a), the thickness on a $Si_{0.15}Ge_{0.85}$ VS is ~17 nm. The $Si_{0.2}Ge_{0.8}$ layer thickness increases with increasing Ge concentration of VS from 85% to 100%. This result indicate that growth rate of the $Si_{0.2}Ge_{0.8}$ layer is increased by increasing tensile strain. On the other hand, in the case of Ge layer in the MQW (Fig. 1b), there is almost no influence of Ge concentration of the VS on the Ge layer thickness. Based on these results, it seems that enhancement of surface reaction of SiH_4 occurs on higher tensile strained SiGe surface.

In Fig. 2, Si concentration in the SiGe layer in the MQW measured by TEM-EDX and intensity ratio of Si 2p and Ge 3d measured by XPS is shown. Because the escape depth of photoelectron by XPS measurement is below 10 nm and top SiGe layer thickness is 17 nm to 18 nm (as shown in Fig. 1a), only photoelectrons from top SiGe layer are visible and the photoelectron intensity from the Ge layer underneath is negligible. By the TEM-EDX analysis, Si concentration in the SiGe layer in MQW on $Si_{0.15}Ge_{0.85}$ VS is ~18%, and tends to increase slightly by increasing the Ge concentration in the VS. The increase is very small, but the increase of Si concentration is also supported by XPS analysis. Therefore, it seems that the increase of the Si incorporation with increasing Ge concentration in the VS (i.e. increasing tensile strain in the growing $Si_{0.2}Ge_{0.8}$ layer) is reliable. Based on the results of Fig. 1a, b and Fig. 2, possible explanation of the slight increase of growth rate for the $Si_{0.2}Ge_{0.8}$ layer (Fig. 1a) but not for the Ge layer (Fig. 1b) could be that there is an increased reaction of SiH_4 on higher tensile strained $Si_{0.2}Ge_{0.8}$ due to higher surface energy. At 500^{o}C, SiH_4 reaction is in the surface reaction limited regime, but GeH_4 reaction is in the mass transport limited regime. Therefore, the reaction of the SiH_4 is increased by higher strain, but the reaction of the GeH_4 is less sensitive for surface energy of the Ge surface because the reaction is mainly limited by the mass transport.

In Fig. 3, cross section STEM (Fig. 3a and 3b) and EDX (Fig. 3c and 3d) of 10 cycles of $Si_{0.2}Ge_{0.8}$ / Ge MQW are shown. Fig. 3a and 3c depict samples with MQW grown on Ge VS and Fig 3b and 3d with MQW grown on $Si_{0.15}Ge_{0.85}$ VS. For both Fig. 3a and 3b, no defects are observed in STEM images, indicating good crystal quality of the MQW. In both EDX images (Fig. 3c and 3d), steep profiles are observed at the interface of Ge on $Si_{0.2}Ge_{0.8}$ layer, however the interface of $Si_{0.2}Ge_{0.8}$ on Ge is smeared. The smeared interface could be caused by Ge segregation into $Si_{0.2}Ge_{0.8}$ [33], to the lower surface energy density of Ge as compared to Si.

Next, influence of strain on the interface steepness is discussed. Because the resolution of

the TEM images is influenced by the TEM lamella thickness, relation between the interface thickness measured by TEM and the TEM sample lamella thickness are summarized in Fig. 4. The interface thickness is determined as the thickness of transition area of Ge concentration between Ge and $Si_{0.2}Ge_{0.8}$. As shown in Fig 4, with increasing the TEM sample lamella thickness, slight increase of the interface thickness is observed for both interfaces, Ge on $Si_{0.2}Ge_{0.8}$ and $Si_{0.2}Ge_{0.8}$ on Ge. This trend is observed for both samples of Ge VS and $Si_{0.15}Ge_{0.85}$ VS. The slight increase is caused by blurred resolution of the TEM image. However, relative constant interface thickness is obtained for TEM lamella thickness between 0.35 T / lambda and 0.5 T / lambda. The estimated interface steepness using the TEM lamella between 0.35 T / lambda and 0.5 T / lambda is summarized in Table 1. In the case of Ge growth on $Si_{0.2}Ge_{0.8}$, only slight increase of the interface steepness (1.5 nm to 1.8 nm) is observed by increasing Ge concentration of the VS from 85% to 100%. On the other hand, in the case of $Si_{0.2}Ge_{0.8}$ growth on Ge, relative large change (6.4 nm to 7.4 nm) of the interface steepness is observed by changing $Si_{0.15}Ge_{0.85}$ VS to Ge VS. A possible reason could be, that higher tensile strain in the $Si_{0.2}Ge_{0.8}$ layer on Ge VS causes higher Ge segregation.

In Fig. 5a and Fig. 5b, XRD RSM of the 10 cycles of the $Si_{0.2}Ge_{0.8}$ / Ge MQW deposited on the Ge VS and the $Si_{0.15}Ge_{0.85}$ VS are shown. In the case of the $Si_{0.2}Ge_{0.8}$ / Ge MQW grown on Ge VS (Fig. 5a), 0.18% of tensile strain is observed in the Ge VS due to thermal expansion coefficient difference between Ge and Si substrate. Subpeaks of SL from $Si_{0.2}Ge_{0.8}$ / Ge MQW are also observed, indicating a constant vertical periodicity of the $Si_{0.2}Ge_{0.8}$ / Ge MQW. The SL periodicity is evaluated to be 31.4 nm. Q_x of the SL subpeaks are shifted to the left side of the Ge VS peak, thus indicating a partial plastic relaxation by MD formation. On the other hand, in the case of the $Si_{0.2}Ge_{0.8}$ / Ge MQW deposited on $Si_{0.15}Ge_{0.85}$ VS (Fig. 5b), position of the Ge VS peak indicates 0.18% of tensile strain again. Position of $Si_{0.15}Ge_{0.85}$ VS peak shows 0.29% of tensile strain, due to partial relaxation from the Ge VS. Subpeaks of SL from the $Si_{0.2}Ge_{0.8}$ /

Ge MQW are also observed. Estimated periodicity of the SL is 30.9 nm. The Q_x position of the SL peaks is same as $Si_{0.15}Ge_{0.85}$ VS peak, indicating the $Si_{0.2}Ge_{0.8}$/Ge MQW layer is pseudomorphically grown on the $Si_{0.15}Ge_{0.85}$ VS.

In Fig.6, improvement of TDD by the $Si_{0.2}Ge_{0.8}$ / Ge MQW deposition on Ge or SiGe VS with various Ge content is summarized. In the case of the $Si_{0.2}Ge_{0.8}$ / Ge MQW deposition on $Si_{0.15}Ge_{0.85}$ VS, the TDD is the same level as that of the $Si_{0.15}Ge_{0.85}$ VS. With increasing Ge concentration of the SiGe VS, improvement of the TDD is observed by the 10 cycles of $Si_{0.2}Ge_{0.8}$ / Ge MQW deposition. Approximately, a 50% reduction of the TDD is observed for the Ge VS sample. It is not possible to achieve a TDD reduction of the same extend by adding the same thickness (300 nm) of simple Ge layer on the ~2 µm thick Ge VS without annealing steps [29, 31, 34]. We attribute the the decrease of TDD by the $Si_{0.2}Ge_{0.8}$ / Ge MQW deposition on the Ge VS might be the same mechanism as reverse graded buffer. The TD network seems to go downwards by tensile strained SiGe growth on Ge [32]. However, further investigations are required to clarify the detailed mechanism behind this observed effect.

Summary and Conclusion

Ten cycles of 15 nm thick $Si_{0.2}Ge_{0.8}$/15 nm thick Ge MQW are fabricated on SiGe virtual substrate with 85% - 100% Ge content to discuss the influence of strain on SiGe and Ge growth. In the case of $Si_{0.2}Ge_{0.8}$ growth on Ge MQW layer, smeared interface is observed due to segregation of Ge atom. On the Ge VS, slightly higher Ge segregation into the $Si_{0.2}Ge_{0.8}$ is observed compared to that on SiGe VS with 85% Ge content due to higher tensile strain in the $Si_{0.2}Ge_{0.8}$ layer. Small increase of growth rate and Si concentration of the $Si_{0.2}Ge_{0.8}$ layer is observed by increasing Ge content of the SiGe VS from 85% to 100%. With increasing Ge content in the VS, higher reduction of the TDD is observed by depositing the 10 cycles of $Si_{0.2}G_{0.8}$/Ge MQW.

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Figure captions

Fig. 1. Thickness of a) $Si_{0.2}Ge_{0.8}$ and b) Ge of MQW deposited on SiGe VS with different Ge concentration. Thickness of the $Si_{0.2}Ge_{0.8}$ and Ge layers are measured by cross section TEM.

Fig. 2. Si concentration measured by EDX and intensity ratio of Si2p and Ge3d in $Si_{0.2}Ge_{0.8}$ layer of $Si_{0.2}Ge_{0.8}$ / Ge superlattice grown on Ge or SiGe virtual substrate with different Ge content. Target thickness of $Si_{0.2}Ge_{0.8}$ and Ge layers are 15 nm and top layer of the MQW is $Si_{0.2}Ge_{0.8}$.

Fig. 3. a) Cross section bright field HAADF STEM images of 10 cycles of $Si_{0.2}Ge_{0.8}$ / Ge MQW deposited on a) Ge VS and b) $Si_{0.15}Ge_{0.85}$, respectively. c) and d) show EDX mapping image of the $Si_{0.2}Ge_{0.8}$ / Ge MQW on Ge VS and $Si_{0.15}Ge_{0.85}$ VS, respectively.

Fig. 4. a) Interface steepness of $Si_{0.2}Ge_{0.8}$ on Ge and Ge on $Si_{0.2}Ge_{0.8}$ as function of Tem lamella thickness.

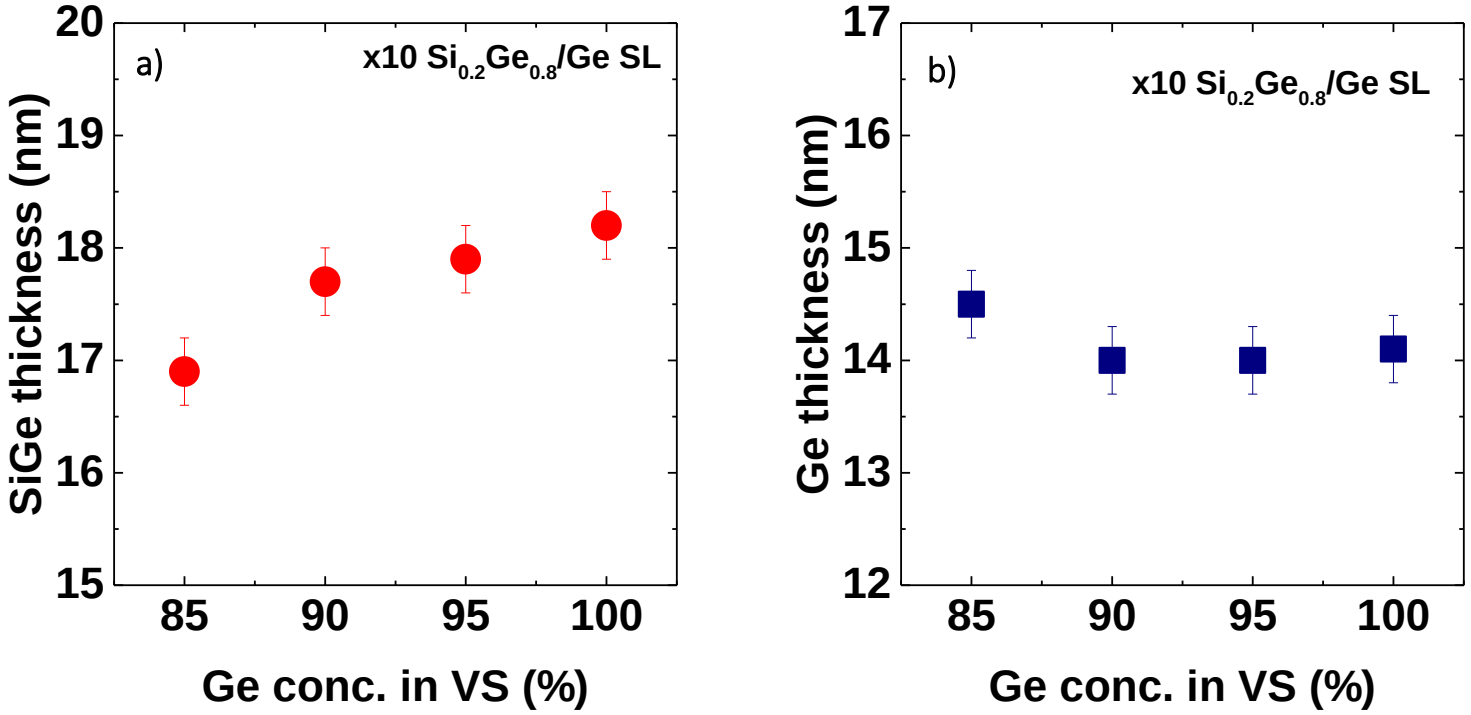
Fig. 5. XRD RSM images of 10 cycles of $Si_{0.2}Ge_{0.8}$ / Ge MQW deposited on a) Ge VS and b) $Si_{0.15}Ge_{0.85}$.

Fig. 6. TDD ratio before and after 10 cycles of $Si_{0.2}Ge_{0.8}$ / Ge MQW deposited on Ge and SiGe VS of various Ge concentrations.

Table

Table 1. Summary of steepness of interface between $Si_{0.2}Ge_{0.8}$ and Ge of MQW measured by TEM.

Virtual substrate	Interface thickness: Ge on $Si_{0.2}Ge_{0.8}$ (nm)	Interface thickness: $Si_{0.2}Ge_{0.8}$ on Ge (nm)
Ge	1.8	7.4
$Si_{0.15}Ge_{0.85}$	1.5	6.4



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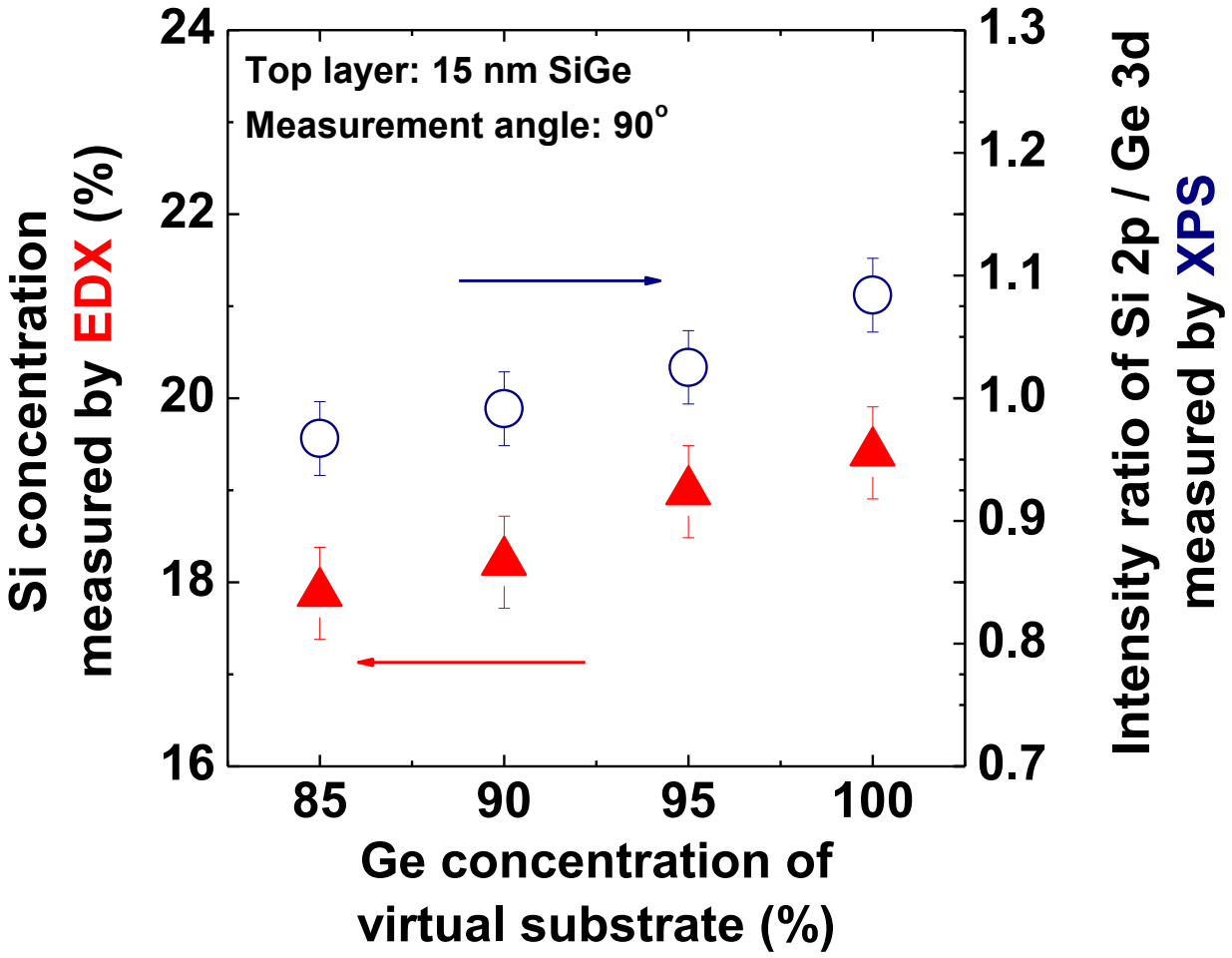

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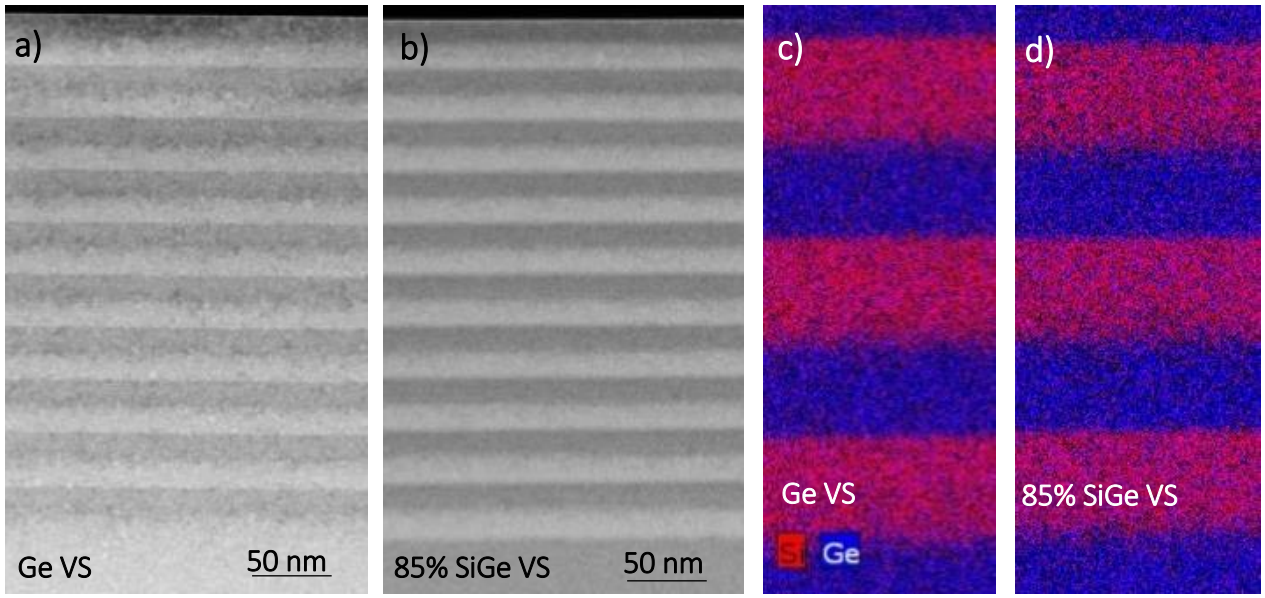

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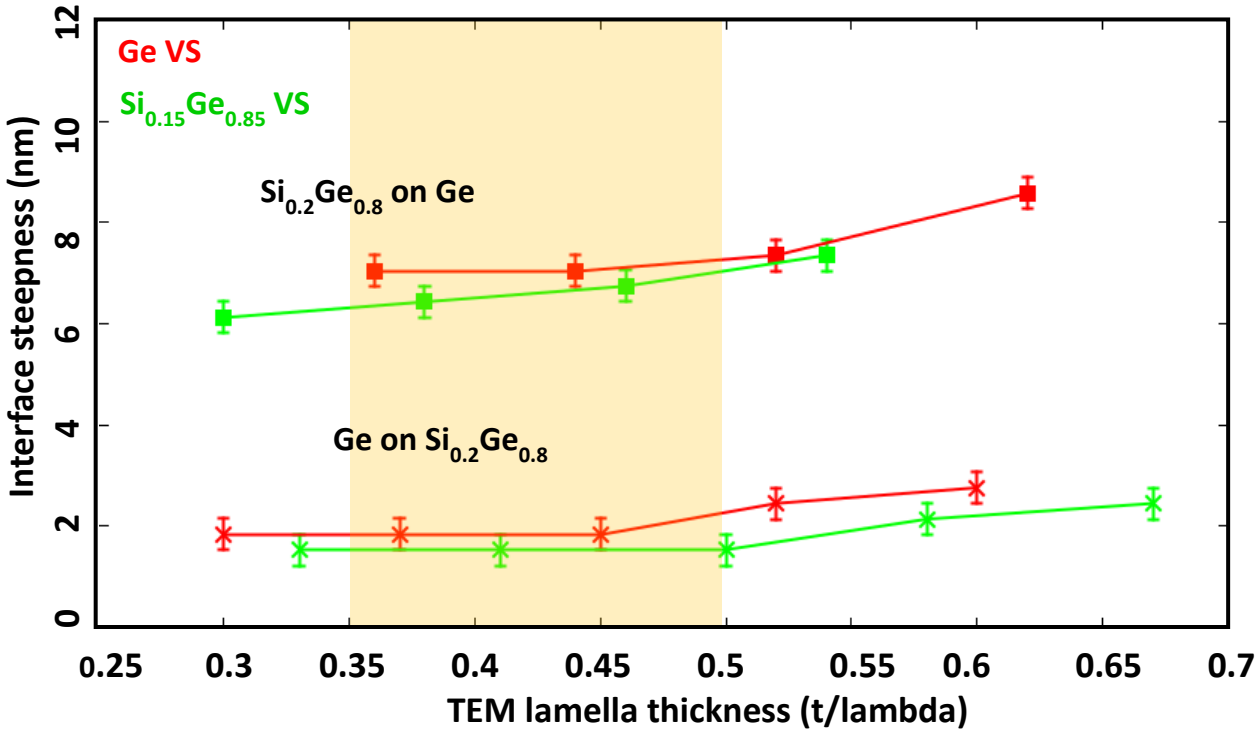

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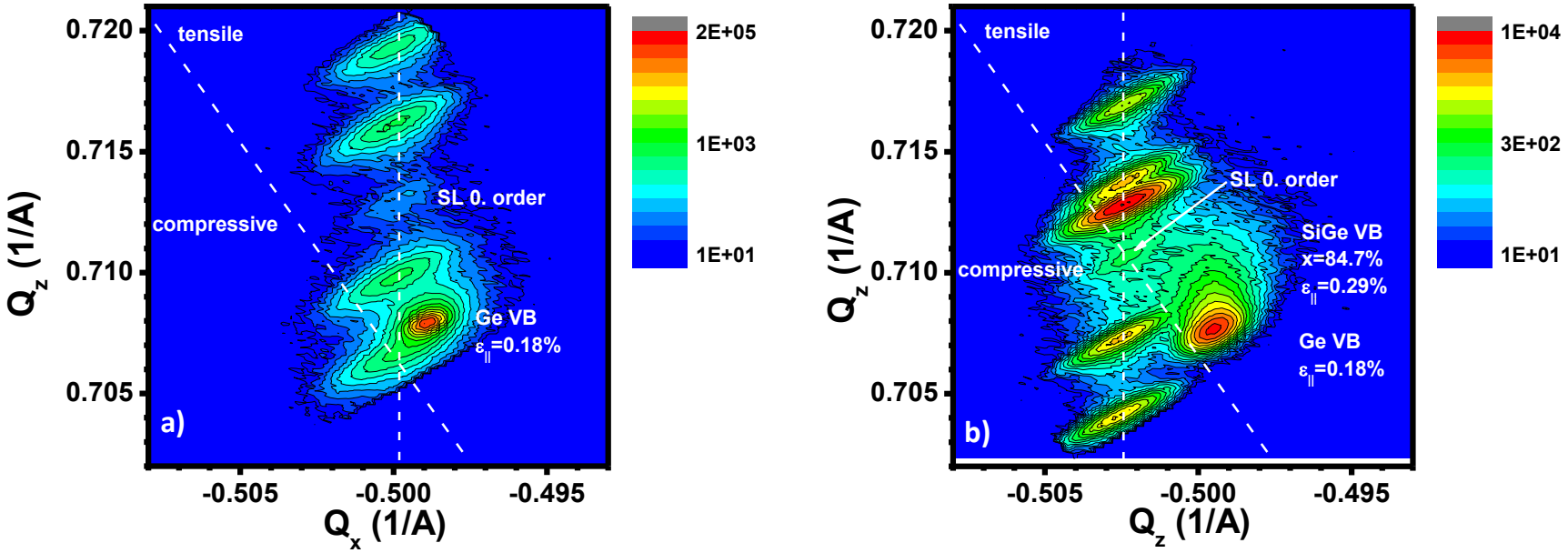

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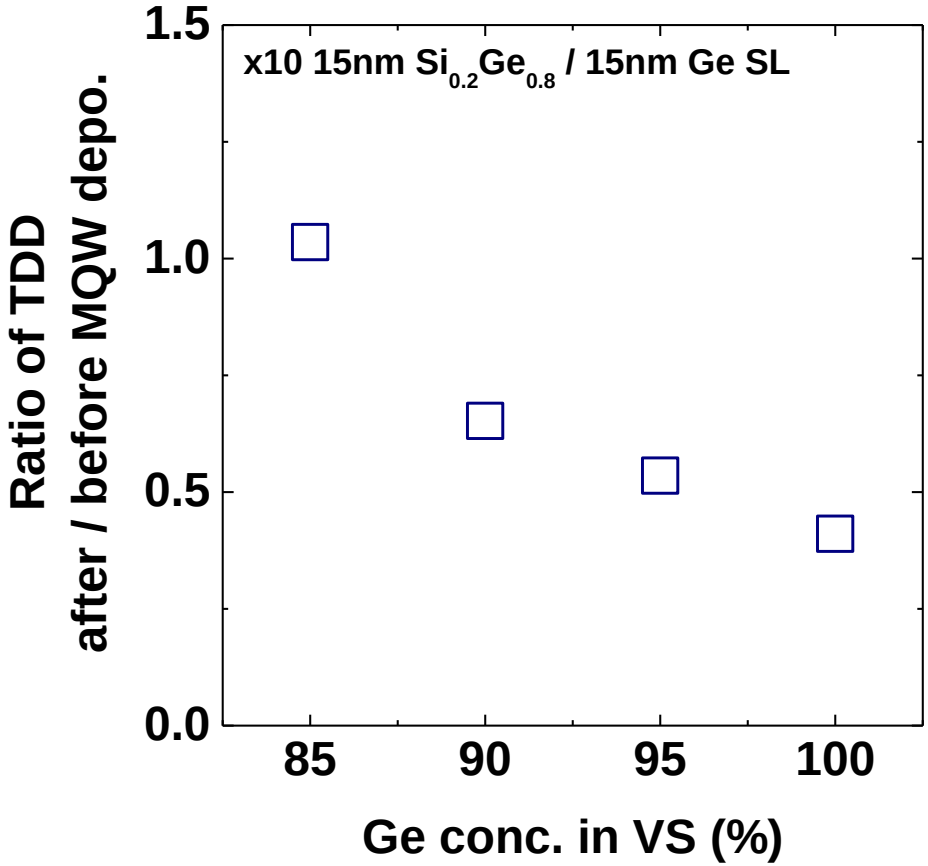

Fig. 6. Y. Yamamoto et al.