

180 GBd Electronic-Plasmonic IC Transmitter

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Abstract: A monolithically integrated plasmonic SiGe-BiCMOS electronic transmitter operating at 180 GBd is demonstrated. Such compact high-speed electronic-photonic integrated circuit (EPIC) transmitters are key components for future high-performance computing (HPC) and data center interconnects (DCI). © 2021 OCIS Codes: 130.4110, 130.3120

1. Introduction

Co-integration of electronic and photonic systems will be required in future communication systems for high performance computing (HPC) and data center interconnects (DCIs). Monolithic integration is one of the most viable paths towards this goal as it not only reduces manufacturing costs, but also provides the shortest path for electrical signals, and thus enables operation at highest speed with lowest energy consumption.

Thus far, the highest-symbol-rate transmitters have involved discrete assemblies [1-5] or side-by-side integrations of electronic and photonic components [6]. The symbol rate is often constrained by the limited bandwidth offered by photonics. Not so with plasmonic modulators—plasmonics has emerged as a technology that offers highest bandwidth, compact footprint, ultra-low energy consumption [7, 8] and has already demonstrated operation at 400 Gb/s/lane [1, 9] and beyond. However, these prior demonstrations have relied on electronic circuits connected through PCB and/or wire bonds. Such integration methods will ultimately face frequency limitations and power consumption challenges, which will at some point prohibit widespread deployment for HPC and DCI.

In 2020 a BiCMOS electronic–plasmonic transmitter based on an electronic-photonic/plasmonic integrated circuit (EPIC) demonstrated data transmission of up to 120 Gb/s OOK with a bit error ratio (BER) of $1.74 \cdot 10^{-2}$ [10].

In this work, we demonstrate 180 Gb/s OOK—the fastest symbol rate in EPIC transmitters, improving the state-of-the-art by a factor of 1.5. Reception below the hard decision forward error correction (HD-FEC) limit of $3.8 \cdot 10^{-3}$ is shown. Furthermore, at 100 GBd the device operates without digital equalization with a BER below the HD-FEC limit. The results show that future real-time implementations with low-complexity signal processing can become practical. The plasmonic modulator requires an area of 0.0017 mm² and can be integrated into the back-end of line of the chip.

2. The Plasmonic 180 GBd 4:1 MUX-Driver-Transmitter

The EPIC transmitter assembly shown in Figure 1(a) consists of a 1.5x3 mm² SiGe BiCMOS chip with monolithically integrated plasmonic modulators, mounted on a 5x7 cm² PCB. The electronic layer stack was fabricated by IHP in a modified SG13G2-process. The electro-optic layer was fabricated by ETH with electron beam lithography-based processes. More details on the process can be found in [10]. As active electro-optical material BAHX was used, a crosslinkable variant of the recently reported high-performance BAH13 material [11, 12], which was poled electrostatically and crosslinked [13].

The assembly is interfaced with RF connectors, ribbon cables, optical fibers and a passive heat sink. A magnified image of the output stage is given in Figure 1(e).

The operation of the EPIC transmitter is as follows. The data is generated by on-chip PRBS generators, multiplexed in two stages, see Figure 1(b), and amplified to $V_p = 0.5$ V. The data signal is consequently encoded onto laser light in the C-band, which is coupled using conventional grating couplers and single-mode fibers. The 15 μm long plasmonic modulator, see Figure 1(c), utilizes a dual-drive design [7], effectively doubling the drive voltage, and

shows a high modulation efficiency where a V_p of 2 V is required for complete extinction. This value is measured in a reference modulator that was on the same chip, but not part of the circuit.

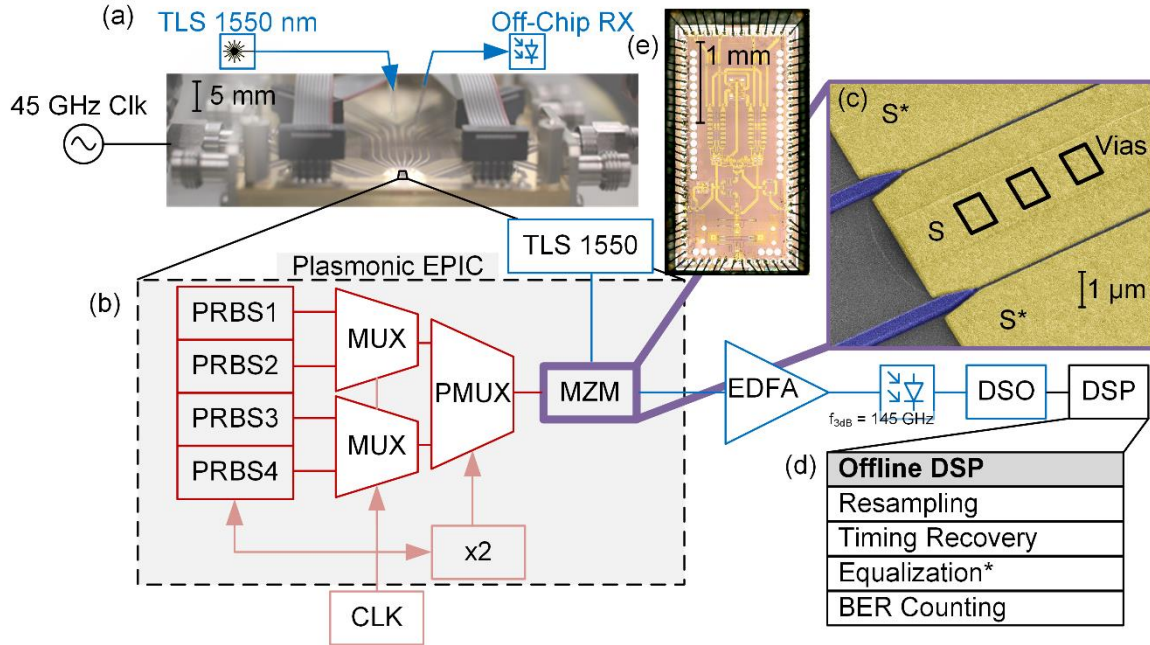


Figure 1: (a) The physical setup with the transmitter EPIC on a PCB routing the clock and low-speed connections. (b) A schematic illustration of the characterization setup and (c) an inset with a colorized SEM of the plasmonic dual-drive MZM. The schematic (b) is drawn to represent the 180 Gb/s experiment, i.e. $4 \times \text{CLK}$. The multiplexer circuit inherently triggers at rising and falling edge, the second stage relies on a phase-locked-loop-based on-chip frequency doubler. The chip contained additional circuitry to run at $2 \times \text{CLK}$ without the frequency doubler, which is not shown here for simplicity. The DSP chain (d), whereby digital equalization was not performed in all experiments. (e) The optical microscope image shows the complete EPIC with wirebonds.

3. Experimental Performance

The setup shown in Figure 1 was used to generate data at 180 GBd and 100 GBd, and to transmit the data through an optical link. The signal is mapped back to baseband in a pre-amplified direct-detection receiver. The optical receiver consists of an erbium-doped fiber amplifier (EDFA), a 145 GHz photodiode and a 113 GHz real time oscilloscope (DSO), sampling at 256 GSa/s followed by offline digital signal processing (DSP), Figure 1(d). For the experiments shown in Figure 2(a)-(c), the laser power in the input fiber was 12 dBm and the wavelength was set close to 1544 nm. The operating temperature was measured to be 120°C , as determined from a reference sample. The optical insertion loss amounted to 25 dB (fiber-to-fiber) in the current experiments. For the results in (a), (c) & (d), a nonlinear feed-forward-equalizer (NLE) was applied.

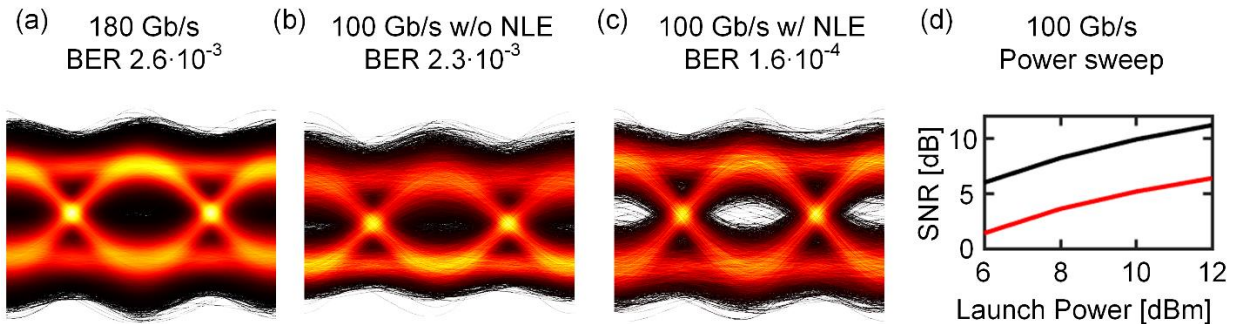


Figure 2: Eye diagrams for (a) 180 GBd and (b), (c) 100 GBd NRZ. In (a) the 180 Gb/s OOK signal is shown after DSP. In (b) and (c) the same signal is shown, once before, once after digital equalization. The 100 Gb/s signal is already below the HD-FEC limit before equalization. In (d) the launched laser power in the input fiber is varied and the SNR is plotted before (red) and after (black) equalization.

The signals seen in Figure 2(a)-(c) are all below the HD-FEC limit. The input power sweep, see Figure 2(d), reveals the relation between signal-to-noise ratio (SNR) and laser power in the input fiber.

4. Conclusion

This work demonstrates a monolithic and most compact EPIC transmitter platform for symbol rates in the order of 200 GBd. The demonstrated high quality of the signal leaves room for future encoding of higher-order modulation such as PAM-4, optical multiplexing as well as low-complexity receiver electronics, further expanding the link capacity. The plasmonic post-processing is not limited to the BiCMOS platform. The same cointegration is possible for high-speed III-V, or low power CMOS, where the ultralow capacitance of plasmonics enable >500 GHz bandwidth [14] and attojoule/bit [8] communication, respectively. The presented plasmonic EPIC transmitter is a scalable solution for future HPC and DCI optical interconnects.

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